Got Jitter? Diagnosing Power Integrity and Signal Integrity Problems
Agenda

• Power integrity (PI) overview
• Challenges in preserving power integrity
• Tektronix TPR power rail probe solution

3 demonstrations to highlight key challenges in PI:
1. High impedance probe coupling challenges
2. Measuring ripple on sensitive voltage rails
3. Maintaining target impedance in a PDN
What is Power Integrity?

THIS IS NOT JUST ABOUT KEEPING VOLTAGES WITHIN LIMITS!

- Power Integrity (PI) is simply the assurance that power applied to a circuit or a device is appropriate for the desired performance of the circuit or the device.
- Its purpose is to maintain the quality of power from generation to consumption.
- Achieving an acceptable power integrity implies the noise levels are within the defined tolerance levels.
Embedded systems these days involve…

- Processors, GPUs, SoCs, FPGAs
- SerDes – High-speed data
- Lots of power rails
- Efficiency and heat management
- Point of load (POL) power regulation, and digital power management (DPM)

Power Integrity gets affected by the system noise

- Noise sources on power rails (frequencies can be quite high)
- Cross talk from data signals, coupling from clocks, power supply switching noise (and harmonics)

What happens if power rails are noisy?

- Too much Jitter → bit errors
- Loss of data

Critical to ensure enough power is applied to a circuit as required for the expected performance
High Level Power Integrity Technical Requirements

<table>
<thead>
<tr>
<th>Example Applications</th>
<th>High Speed/Low Speed Applications (e.g. Servers &amp; Mobile Devices)</th>
<th>Others (e.g. Power supplies, DC-DC, LVDC buses)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Ripple / Noise Voltage</strong></td>
<td>&lt;10 mV riding on 0.3 V – 3 V</td>
<td>≥ 10 mV riding on 5-48 V</td>
</tr>
<tr>
<td><strong>Transients (edge)</strong></td>
<td>&gt;2 GHz</td>
<td>&lt;1 GHz or lower due to switching edges</td>
</tr>
<tr>
<td><strong>Requirements</strong></td>
<td>10s of uV resolution at high BW</td>
<td>High DC offset voltage and dynamic range</td>
</tr>
<tr>
<td><strong>Measurements</strong></td>
<td>Ripple on fast transitions</td>
<td>Ripple Measurements</td>
</tr>
<tr>
<td></td>
<td>Cross talk (isolate noise from Jitter)</td>
<td></td>
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</tbody>
</table>
3 Major Performance Challenges...

Signal Integrity Issues
- Attenuation
- Reflection
- Dispersion
- Interference
- Cross Talk

Power Integrity Issues
- Voltage Drop
- Switching Noise
- Cross Talk

EMI Issues
- Near Field Coupling
- Radiated Emissions

Problems to be Solved

WHERE ARE THE CUSTOMERS STUCK?

1. The Measurement System/Method
   - Overall PDN Impedance

2. Signal Integrity vs Power Integrity

3. Device Response across Frequencies

4. DC-DC Power Conversion
   - Ripple, Transients, Power Sequencing, Jitter

5. AC-DC Power Conversion
   - Power Quality, Switching Ripple, Switching Loss, Magnetics, Harmonics, SOA, Efficiency
   - Frequency Response Analysis and PSRR

Determine Impedance profile of the PDN components
Power Integrity Coupling Requirements

Issue with AC Coupling:
- You lose the low frequency events like voltage droop and creep

Issue with AC+DC Coupling:
- Different offsets on different voltages as required by most applications.
- Not enough resolution
- Issues with baseline noise
- Issues with noise on high attenuation probes

Figure 11. Example of a device that is scaling the input voltage needed as the frequency is increased. The ~2 Hz frequency component between steps will be missed with many AC coupling filters
# Power-Rail Probes

## SPECIFICATIONS AND THEIR VALUE PROPOSITION

<table>
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<tr>
<th>Specifications</th>
<th>TPR1000</th>
<th>TPR4000</th>
<th>Value Proposition</th>
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<tbody>
<tr>
<td>Bandwidth</td>
<td>1 GHz</td>
<td>4 GHz</td>
<td>Higher Bandwidth to capture more signal noise content</td>
</tr>
<tr>
<td>Offset Voltage Range</td>
<td>±60V</td>
<td></td>
<td>Larger offset to cover wide range of DC power rails</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>±1V</td>
<td></td>
<td>Larger dynamic range to account for any current droops</td>
</tr>
<tr>
<td>Input Resistance</td>
<td>50KΩ DC, 50Ω AC</td>
<td></td>
<td>Higher input impedance to reduce oscilloscope loading effect</td>
</tr>
<tr>
<td>Input Coupling</td>
<td>DC, LF Reject</td>
<td></td>
<td>Allow higher offset (larger rails) while zooming-in on small ripple</td>
</tr>
<tr>
<td>Accuracy</td>
<td>1mV</td>
<td></td>
<td>Tighter resolution to see smallest ripple, meet specifications</td>
</tr>
<tr>
<td>System Noise (With 6 Series Scopes)</td>
<td>&lt;300µV Peak-To-Peak (With 20MHz Bandwidth Limit)</td>
<td>&lt;1.3mV Peak-To-Peak (At Full Bandwidth of Scope)</td>
<td>Lower system noise means less confusion about the noise of the oscilloscope and probe (system noise) with the noise and ripple of the DC supply being measured → Designer can focus only their designs instead of guessing or over-design</td>
</tr>
<tr>
<td>Attenuation</td>
<td>1.25x</td>
<td></td>
<td>Less, or no, attenuation to send DC rail to oscilloscope “as-is”</td>
</tr>
<tr>
<td>Connectivity &amp; Accessories</td>
<td>New Browser, Solder-In &amp; Snap-On</td>
<td></td>
<td>Modular &amp; flexible connectivity options to cover most needs</td>
</tr>
</tbody>
</table>
Power Rail Coupling Demo

DC supply connected to a System on chip or (SOC)

MMCX Connection

TPR4000: 4 GHz Power Rail Probe

MSO64: 25 GS/s, low noise, up to 16-bit resolution

Source: www.beaglebone.org
Switching Ripple and Noise

SO WHERE’S THE ‘SWITCHING’ HAPPENING?

**Ripple**: Charge/Discharge of storage elements; Switching frequency of the SMPS

**Noise**: Can come from anywhere; parasitic inductances, and high charge/discharge of digital coupling

The VRM uses three components to do its job: MOSFETs, inductors (also called chokes), and capacitors. These components introduce the AC elements into the otherwise DC based PDN system

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https://www.technog.com/2019/05/smps-block-diagram.html
Ripple on Ripple Demo

Solder point near a DDR3 memory module (1.5V rail)

TPP1000: 1 GHz, 10x Passive Probe

MSO64: 25 GS/s, low noise, up to 16-bit resolution

TPR4000: 4 GHz Power Rail Probe

Source: www.beaglebone.org
Connectivity Matters!

BECAUSE MAKING CONNECTIONS IS TOUGH!

To reduce ringing and get full BW, we need:
Low Inductance, and Low Capacitance

Need super high signal integrity – no compromises?
• Micro RF connectors - MMCX
  ◦ Need to be planned
  ◦ Take up space

Need semi-permanent connections for decent signal integrity with no planning?
• Micro Coax & Flex Solder-in adapters
  ◦ Need to be soldered-in
  ◦ Not as good as MMCX

Need to debug, quick and dirty checks?
• Browsers and adapters!
Target Impedance

- Target impedance represents the upper limit on PDN impedance that should be maintained in a system such that the power supply noise doesn’t exceed a maximum value.
  - Impedance = f(R, C, and L), and varies over a frequency range.
- Lowering impedance requires a target impedance, and determining where the ‘anti-resonance’ occurs.
  - Anti-resonance is the condition for which the reactance vanishes and the impedance of an electrical circuit is very high, approaching infinity.
- Designers include capacitors when the anti-resonance impedances are above the target impedance (Z).
  - The capacitors will lower the impedance at that particular frequency without affecting the PDN’s performance.
  - The addition of capacitors raise the cost of the product.
  - If the antis resonance is lower than the target impedance then no action is required.

Source: https://www.signalintegrityjournal.com/articles/1083-target-impedance-is-not-enough#:~:text=In%20a%20PDN%20designed%20to,below%201.57%C3%97%20target%20impedance
Decoupling Caps

• Two Main Goals of the Decoupling Caps
  ◦ Charge Supply → provide the required charge to a switching current load within a short period of time
  ◦ Filtering → The noise due to the switching of the transistors will be shunted to ground

• Implemented to reduce the output impedance of a PDN
• Used to keep the power rail transient voltages within allowable limits
• The impedance of a de-cap reaches the minimum impedance at the frequency $\omega = \frac{1}{\sqrt{LC}}$ (resonant frequency)
• At high frequencies, the de-cap does not act as a resistance, but rather as an inductor, and its impedance grows with frequency (parasitic inductance)

Source: [https://commons.wikimedia.org/wiki/File:MLCC-Imp-versus-Frequenz.engl.png](https://commons.wikimedia.org/wiki/File:MLCC-Imp-versus-Frequenz.engl.png)
Important Measurements

1. Control Loop Response (using Bode Plot)
   - Understand Noise, perturbation, load variation
   - Is the control loop working correctly?
   - Is my design stable?

2. Power Supply Rejection Ratio (PSRR)
   - Understand the Input Voltage variation
   - Does a bad input voltage affect my output voltage?
   - Maximize the min value of the PSRR

3. Impedance
   - Impedance values across a specific frequency bands
Tektronix Method – Impedance

Measurement System

- 4/5/6 Series MSO Scope
- AFG (from the scope or external)
- Direct SMA or BNC
- Power Supply (Picotest)
- Active Splitter (Picotest)
- Common-mode Transformer (Picotest)

1Source of power supply can be a DC power supply unit or USB connector
2It is recommended to use DC block at CH2 of the oscilloscope, if there is a DC offset in the signal.
Impedance Demo

Ideal operating range of the device

Impedance Demo

Peak 1: 455.8 μΩ @ 165 Hz
Peak 2: 354.9 μΩ @ 670 Hz
Peak 3: 352 μΩ @ 8.75 kHz

Ideal operating range of the device
Thank you! Questions?