Tektronix®

Testing at the Edge of Innovation

DesignCon 2025 I BOOTH #819

Experience our Demos

Streamline PCIe Gen 6/7 Validation Testing

Automate Test at 64 GT/s for PCI Express 6.0 CEM Tx & Rx

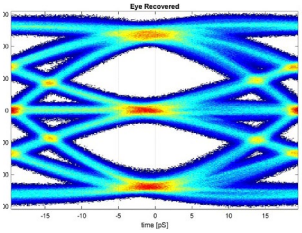
- Enable upcoming spec release for 64.0 GT/s data transfer rate for faster processing to meet rapidly growing AI/ML needs
- Simplify complicated calibration and measurement of PAM-4 signaling
- Test full compliance with backward compatibility to PCIe Gen 5.0, 4.0, and 3.0, Base and CEM

Explore Pathfinding of 128 GT/s Measurements for PCIe 7.0 Base Specification

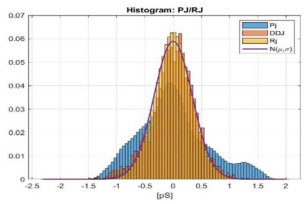
- Analyze signal integrity of PAM-4 signaling at 128 GT/s, measurements of eye diagram, signal-to-noise distortion ratio (SNDR), and ratio level mismatch (RLM)
- Characterize and compensate noise of measurement system for improved measurement accuracy

Simplify DDR5 and USB4v2 to Accelerate Compliance Testing

Streamline USB4v2 Validation at 40 Gb/s



- Acquire and analyze in parallel improving speed and scope utilization
- Enhance accuracy through low intrinsic jitter
- Leverage latest industry-standard disaggregated architecture

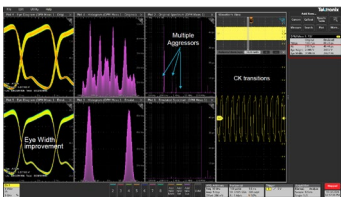


Empower Engineers with a Unified DDR5 DRAM Tx/Rx Test Workflow

- Streamline testing processes by offering a cohesive experience with a unified Tx/Rx workflow
- Enable precise troubleshooting and quick issue resolution with flexible debugging capabilities

Optimize Power & Signal Integrity for GenAI Data Centers

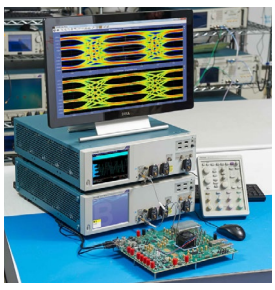
Achieve Energy Efficiency with Improved PI/SI Measurements



- Evaluate power supply reliability (transients, noise, sequencing)
- **NEW!** Characterize power supply induced jitter (PSIJ) for reliable PDN's
- **NEW!** Isolated Current Probe (TICP Series) for Dynamic Current Evaluation

Enable Networking for AI/HPC Interconnects

Accurately Test 800G PHY Transmitter Conformance



- Analyze signal integrity of PAM-4 signaling at 112 Gb/s, measurements of eye diagram, signal-to-noise distortion ratio (SNDR), and jitter (J3u, Jrms, EOJ)
- Quickly recover a clock on a PAM-4 signal; no external trigger source or hardware clock recovery required

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Elektro-Automatik

Scale High-Power Battery Testing

Adapt to Any Power Test Application with Flexible Platforms

- Easily test multiple high-power battery modules simultaneously using multiple channels for load or power source
- Access a full range of voltage test parameters from low to high with a single device
- Characterize batteries at >1 kHz programming and measurement speeds
- Pre-charge, polarity check and external contactor control

Scan this QR Code to Sign Up for a Demo

Come Hear Tek Experts

The Case of the Closing Eyes: 200G/Lane AI HW Dogfight, it's Impact on You & Ethernet, NVLink, OIF, PCIe

Tuesday, January 28 I 4:45 PM – 6:00 PM PST
Ballroom E

Multiple Pulses-Based Decision Feedback Equalizer (MPDFE) for PAM4

Wednesday, January 29 I 11:15 AM - 12:00 PM PST
Ballroom F

PCI Express 7.0 PHY Electrical Pathfinding Updates

Wednesday, January 29 I 2:15 PM - 3:00 PM PST
Great America Ballroom 3

The Expanded Role of SI/PI in Next Gen AI Data Center Development

Thursday, January 30 I 11:15 AM - 12:00 PM PST
Chiphead Theater

200Gbps Lanes Equalization Methods & Required Fixture Bandwidth, S-parameter Bandwidth & Acquired Signal Bandwidth

Thursday, January 30 I 12:15 PM – 1:00 PM PST
Ballroom C

Arbitrary Waveform Generator Assisted Digitalization of Physical Channels with Fractional Sampling Rate for SerDes High-Speed Evaluation

Thursday, January 30 I 12:35 PM - 12:45 PM PST
Chiphead Theater

Unbaking the Cake: The New Science of Compensating for Instrument Noise in Serial Data Measurements

Thursday, January 30 I 4:00 PM – 5:15 PM PST
Ballroom C