Tektronix®

Gain Powerful Design Insights

We Can Help You Solve Your Measurement Challenges

DesignCon 2024 I BOOTH #827

Experience our Demos

PCI Express® 6.0 Tx Automated Test Solution at 64 GT/s

- Simplify calibration and measurement of PAM-4 signaling
- Test full compliance with backward compatibility to PCIe® Gen 5.0, 4.0, and 3.0, Base & CEM

FEATURING: MARVELL

Pathfinding 128 GT/s Measurements for PCIe 7.0 Base Specification

- Analyze signal integrity of PAM-4 signaling at 128 GT/s, measurements of eye diagram, signal-to-noise distortion ratio (SNDR), and ratio level mismatch (RLM)

FEATURING: SYNOPSYS® Anritsu Advancing beyond

PCIe 6.0 Optical Test Feasibility

- Explore the viability of a PCIe 6.0 x8 link over optical fiber at 64 GT/s through testing enabled by Alphawave Semi's PCIe Subsystem PiCORE Controller IP + PipeCORE PHY and the Nubis XT1600 high-density and low-latency Linear Optical Engine

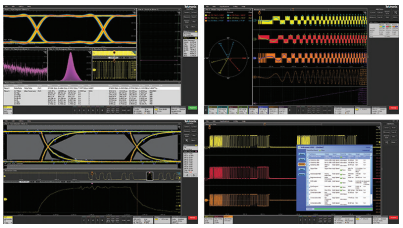
FEATURING: nubis COMMUNICATIONS ALPHAWAVE SEMI



Quickly Validate and Gain Insight into the Latest DDR5 and LPDDR5-5X Designs

- Leverage powerful de-embedding to make the measurement where it matters – at the DRAM

FEATURING: AMD



Multi-Domain Troubleshooting & Validation – Streamlined Signal Integrity Test

- Optimize system designs with exceptional signal integrity on the 6 Series B MSO
- Seamlessly correlate time and frequency domain signals for multi-domain troubleshooting



Embedded Power Design Solutions for Every Bench with the NEW 4 Series B MSO

- Compute power measurement results 2x faster with the 3.0 GHz processor
- Gain powerful insights with automated measurements for switching power supplies, SiC/GaN WBG test
- Examine small signal details at higher resolution

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Come Hear our Experts

Panel – The Case of the Closing Eyes
Tuesday, January 30 | 4:45 PM - 6:00 PM PST | Ballroom E
Learn More

Sponsored Session: PCI Express 6.0 CEM Pathfinding Updates
Wednesday, January 31 | 9:00 AM - 9:45 AM PST | Great America Ballroom 3
Learn More

Panel – PCI Express® & PAM4: Pathway to 128 GT/s & Interoperability at 64 GT/s
Wednesday, January 31 | 4:00 PM - 5:15 PM PST | Ballroom C
Learn More

Panel – The Impact of Data Center & AI Growth on SI/PI Engineers
Wednesday, January 31 | 4:00 PM - 5:15 PM PST | Ballroom B
Learn More

Technical Session: Multiple Linear Fit Pulse Responses for PAM4 Measurements
Thursday, February 1 | 8:00 AM - 8:45 AM PST | Ballroom A
Learn More

Technical Session: Lowering the Jitter & Noise Floor of PAM4 Measurements
Thursday, February 1 | 11:15 AM - 12:00 PM PST | Ballroom C
Learn More

Technical Session: PAM-4 Signals Testing Considerations: Learnings from PCIe® & Ethernet/OIF-CEI for 100+ Gb/s per Lane
Thursday, February 1 | 12:15 PM – 1:00 PM PST | Ballroom B
Learn More

Get information about all of our demos by scanning the QR codes below:

DDR Test Solutions for Memory

PCIe Validation and Debug

6 Series B MSO Mixed Signal Oscilloscope

4 Series B MSO Mixed Signal Oscilloscope

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