Tektronix®

DesignCon 2023

BOOTH #727

Gain Powerful Design Insights

Let us show you – in real time – practical applications to solve current and emerging test challenges.

- **Dive deep into DDR5 and LPDDR5/5X.** Explore the Tektronix memory solutions (leveraging powerful analysis tools) on AMD's advanced server platform. By using Tektronix' P7700 series high impedance probes, along with Nexus XH series interposers, design and validation engineers can capture DDR waveforms with high signal fidelity. From there, the TekExpress DDR compliance software can be easily used to quickly automate, measure, and validate DDR5 and LPDDR5X designs.
- **See unique probing connections for power and signal integrity.** With more demanding high-speed components per board, analyzing Power Rails and Power Distribution Networks for channel-to-channel interference is a critical piece in design validation. This is especially true while under load in various operating conditions. Using the unique capabilities of the 6 Series B MSO Oscilloscope with application-specific probes, design and validation engineers can accurately correlate voltage, current, and EMI signals to quickly identify sources of error and propose corrections.
- **Watch a demonstration of a complete electrical solution for full compliance testing or system debugging for the recent IEEE 802.3ck,** for previous 50G/per lane standards, and for PCIe® all the way up to Gen 6 using the Tektronix DPO70000SX Real Time Oscilloscope.
- **Learn a new approach for modeling complex PAM4 SerDes receiver equalizers** using Conditional Generative Adversarial Networks (cGAN). Tektronix DPO70000SX Oscilloscope captures data with no knowledge of the receiver equalizer structures. The model can generate Bit-Error-Rate (BER) contour as well as eye-diagram outputs that are indistinguishable from ground truth measurements produced by the Tektronix PAMJET Signal Analysis software.

NEW Margin Tester for Fast PCIe Link Health Evaluation

Join us as we demo the industry-first PCIe Link Health Evaluation solution from Tektronix: the TMT4 Margin Tester. This new product category enables design, validation, and failure analysis teams to assess the link health of the PCIe Gen 3 and Gen 4 devices in just minutes – not hours or days like legacy test solutions.

NEW Automated PCIe 6.0 Base Tx/Rx Testing at 64 GT/s

Industry first automated testing solution for PCI Express 6.0 Base transmitter and receiver testing at 64 GT/s. Wizard-based user interface simplifies calibration and measurement complexities of PAM-4 signaling. Supports backward compatibility of full compliance testing for mainstream generation - PCIe 5.0 / 4.0, Base and CEM.

Click on link or Scan QR Code to request a demo

REQUEST DEMO

Presentations Featuring Tektronix Experts

TUTORIAL

Tuesday, Jan. 31

9:00AM – 11:30AM

Ballroom E

Measuring PSNR/PSRR/PSMR to Meet QSFP/OSFP High-Speed Requirements

Speakers: Pavel Zivny, Domain Expert; Tony Ambrose, Application Engineer; et al.

In this tutorial, we focus on PSRR, PSMR, and PSNR which are all measures of how power rail noise appears at the output of voltage regulators, RF amplifiers, and digital channel jitter. PSNR on 400/800G transceivers will be a focus. The test solution using the P2124A, the first water cooled testing probe for PSNR noise immunity applications is explored. Live demonstrations of PSRR testing of power supplies using Tektronix oscilloscopes, PSMR using Signal View software, and PSNR using a 112Gb/s PAM4 application will be presented.

PANEL

Tuesday, Jan. 31

4:45PM – 6:00PM

Ballroom GH

The Case of the Closing Eyes: Bridging FEC to Signal Integrity

Panelists: Chris Loberg, GM Mainstream Scopes; Pavel Zivny, Domain Expert; et al.

Forward Error Correction (FEC) is a key enabler for high-speed communications designs. This panel of experts will discuss the role FEC plays and how it can be impacted by signal integrity challenges; and what to do with a testing architecture designed to help find a bridge between FEC and Signal Integrity. Join this session for a lively debate on the topic.

PANEL

Tuesday, Jan. 31

4:45PM – 6:00PM

Ballroom F

PCIe 6.0: Challenges of Achieving 64GT/s with PAM4 in Lossy, HVM Channels

Panelist: David Bouse, PCI Express Technology Lead; et al.

This panel will focus on the latest evolution of PCI Express Technology, revision 6.0 of the PCIe spec, which uses PAM4 rather than NRZ signaling of previous PCIe revisions. PCI Express technology's advances to 64GT/s has enabled system designers to achieve much needed and desired improvements in data throughput aiding advances in the deployment of artificial intelligence inference engines and co-processors in the data center.

TECHNICAL SESSION

Wednesday, Feb. 1

8:00AM – 8:45AM

Ballroom F

Towards 106 GBaud: Analysis of Latest 53 GBaud DUTs Informs the Improvements of Methodology

Speakers: Pavel Zivny, Domain Expert; Maria Agoston, Principal Engineer

With the understanding of the behavior of the devices with the settings of the current standard, we'll run experiments with the different proposed changes, such as measurement bandwidth filters current and proposed for 106 GBaud, and proposed equalizations – all scaled to the symbol rate of our existing commercial devices. We will analyze in detail the part that only a few optical standards explicitly mention although it impacts both electrical and optical signals' measurements alike: the end of measurement filter compliance.

TECHNICAL SESSION

Thursday, Feb. 2

11:15AM – 12:00PM

Ballroom G

Data-Driven PAM4 SerDes Modeling & Generative Adversarial Network

Speakers: Wenzheng Sun, Software Design Engineer; Muhammad Saad Chughtai, Software Design Engineer; et al.

This paper will describe a novel method to model complex PAM4 SerDes using cGAN. Modeling is based on deep learning using data from test instrument captures or chip internal measurements. No knowledge of the SerDes equalizer structures such as CTLE or DFE is required to generate the model.