TEKTRONIX
INNOVATION FORUM
2023
Engineering the Future

Understanding USB4 v2.0 and the Challenges of PAM3 Signaling for Physical Layer Testing

Nitin Jhanwar

Agenda

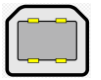
- USB History
- Comparison with USB4 Gen2, Gen3 and Gen4
- PAM3 Signaling
- Test Descriptions
- Tektronix Offering
- Unique debugging capability : PAMJET

USB Evolution

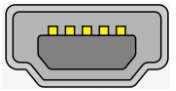
USB Standard

Standard	Year	Data Rate	Connectors
USB 1.0	1996	12 Mbps (FS)	Standard A/B, Mini A/B, Micro A/B
USB 2.0	2000	480 Mbps	Standard A/B, Mini A/B, Micro A/B
USB 3.0	2008	5Gbps	Standard A/B, Micro-A/B/AB, Powered B
USB 3.1	2013	10 Gbps	Type – C
USB 3.2	2017	20 Gbps	Type – C
USB4 V1	2019	40 Gbps	Type – C
USB4 V2	2022	80 Gbps	Type - C

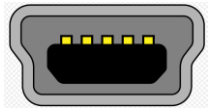
Type - A



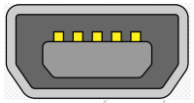
Type - B



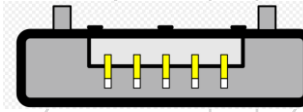
Mini - A



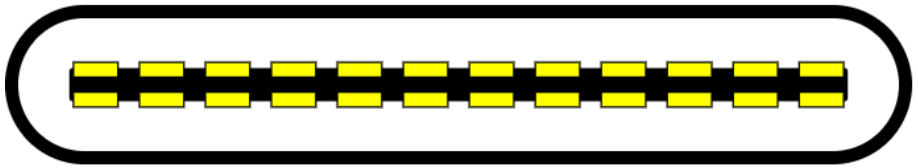
Mini - B



Mini - AB



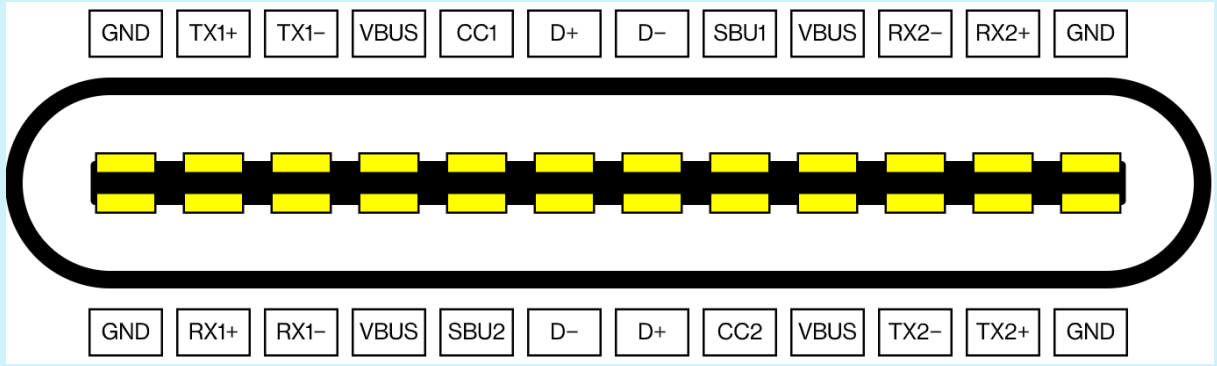
Micro - A



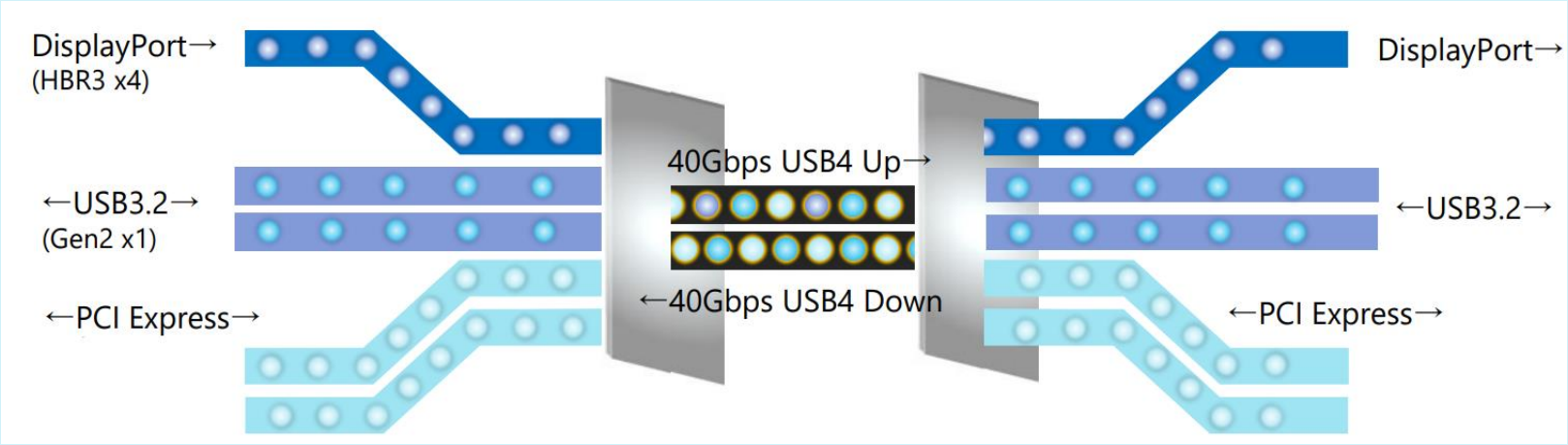
Type - C

Type – C Connector

Symmetrical



Multiple protocol into a single physical layer



USB V1

USB4 Ver 1

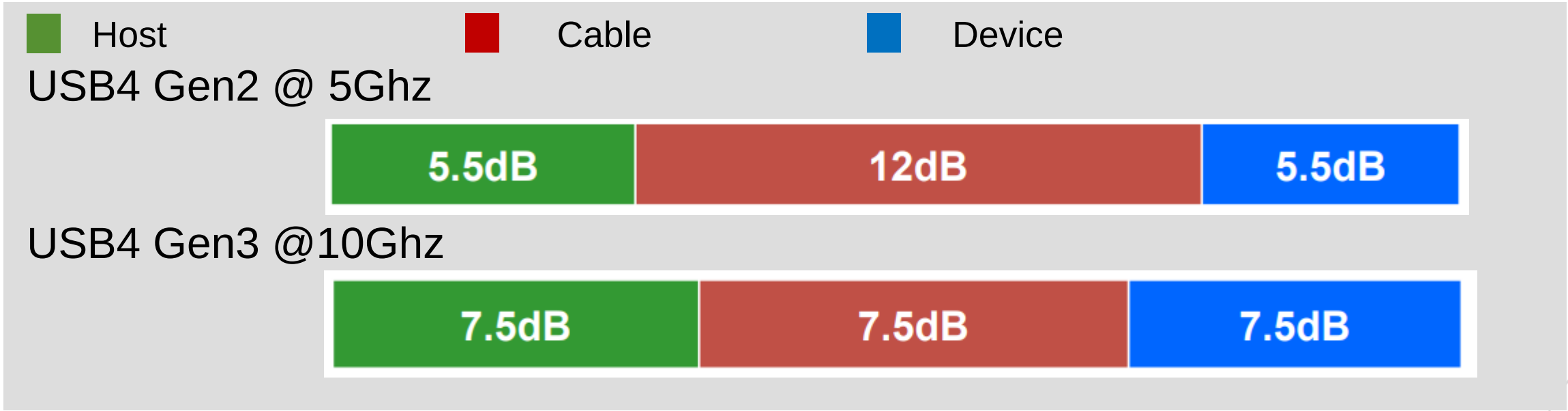
Gen2 : 10GBPS (64B/66B)
Gen3 : 20 GBPS (128B/132B)

Key Features

- 20Gbps x2 lanes (40Gbps data transfer rate)
- Sideband signals using USB Type-C cable and connector
- Specification Derived from Thunderbolt – 4
- Introduced Preset Calibration to USB testing

USB4 Ver 1

Loss Targets : Gen2 – 23db @5Ghz Gen3 : 22.5db @10Ghz



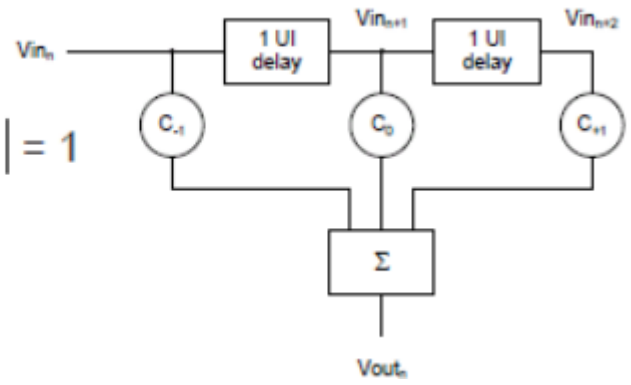
The above host/device loss targets include losses from the die to the receptacle connector, including package, AC capacitor, and substrate Wiring, ESD protection devices included

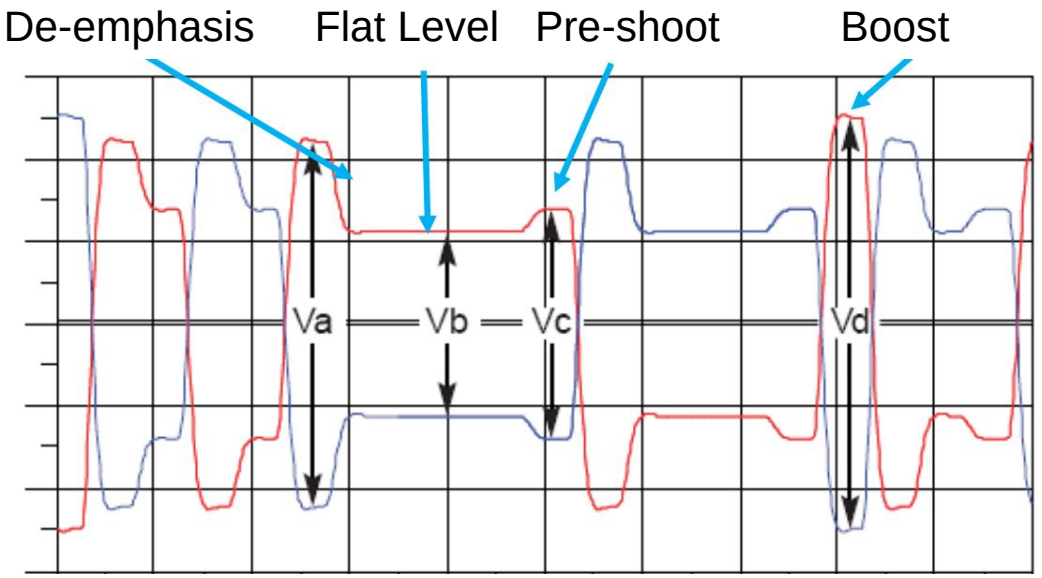
USB4 Ver 1 Transmitter Equalization

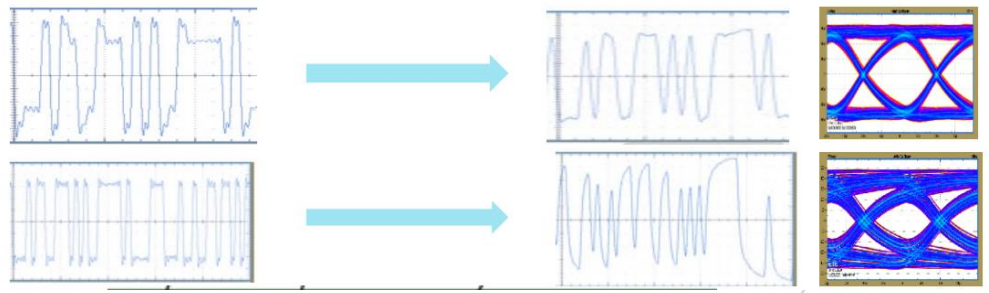
16 Presets

Preset Number	Pre-shoot [dB]	De-emphasis [dB]	Informative Filter Coefficients		
			C_{-1}	C_0	C_1
0	0	0	0	1	0
1	0	−1.9	0	0.90	−0.10
2	0	−3.6	0	0.83	−0.17
3	0	−5.0	0	0.78	−0.22
4	0	−8.4	0	0.69	−0.31
5	0.9	0	−0.05	0.95	0
6	1.1	−1.9	−0.05	0.86	−0.09
7	1.4	−3.8	−0.05	0.79	−0.16
8	1.7	−5.8	−0.05	0.73	−0.22
9	2.1	−8.0	−0.05	0.68	−0.27
10	1.7	0	−0.09	0.91	0
11	2.2	−2.2	−0.09	0.82	−0.09
12	2.5	−3.6	−0.09	0.77	−0.14
13	3.4	−6.7	−0.09	0.69	−0.22
14	3.8	−3.8	−0.13	0.74	−0.13
15	1.7	−1.7	−0.05	0.55	−0.05

$$|C_{-1}| + |C_0| + |C_{+1}| = 1$$



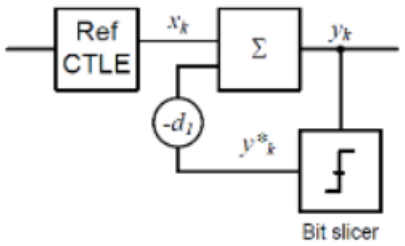


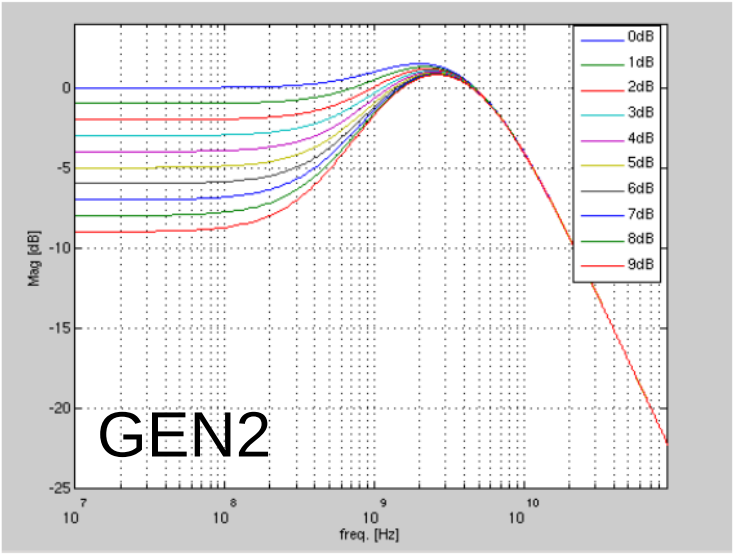


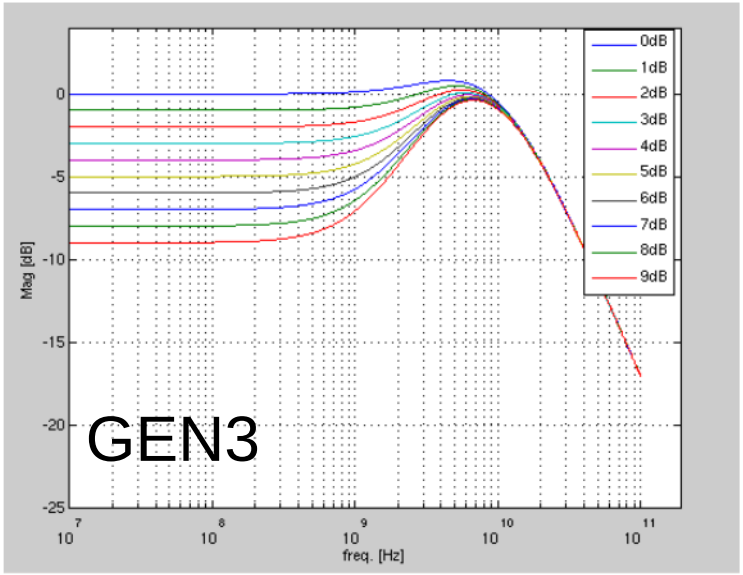
USB4 Ver 1 CTLE and DFE

CTLE Parameter	Gen2	Gen3
fp1	1.5 GHz	5GHz
fp2	5 GHz	10 GHz
Adc	0-9db	0-9db

$$H(s) = 1.41 \cdot \omega_{p2} \cdot \frac{S + \frac{A_{dc}\omega_{p1}}{1.41}}{(S + \omega_{p1})(S + \omega_{p2})}$$





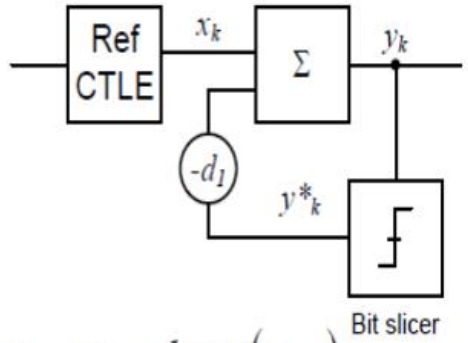


USB4 Ver 1 DFE

DFE: weighted, delayed by 1 bit and added to original waveform

Benefits:

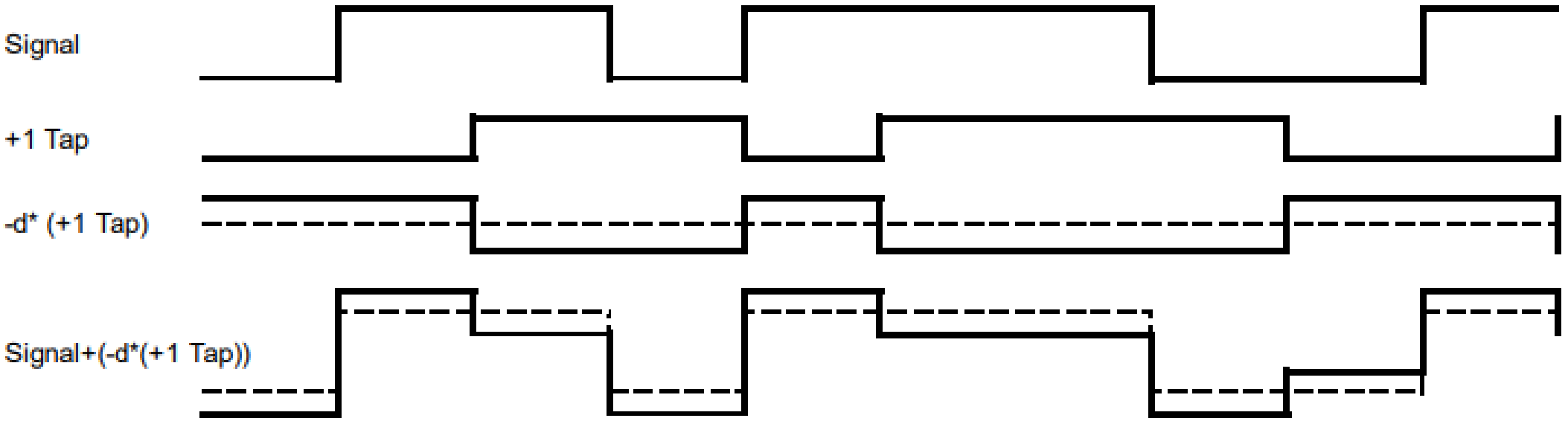
1. Boost during transition and suppression during non-transition.
2. Derivation of the coefficient that opens the eye to the maximum using the method of least squares (does not exceed 50mV) ▪
3. Cancels inter-symbol interference without amplifying the noise that other equalizers suffer from



$$y_k = x_k - d_1 \operatorname{sgn}(y_{k-1})$$

$$0 \le d_1 \operatorname{sgn}(y_{k-1}) \le 50mV$$

USB4 Ver 1 DFE

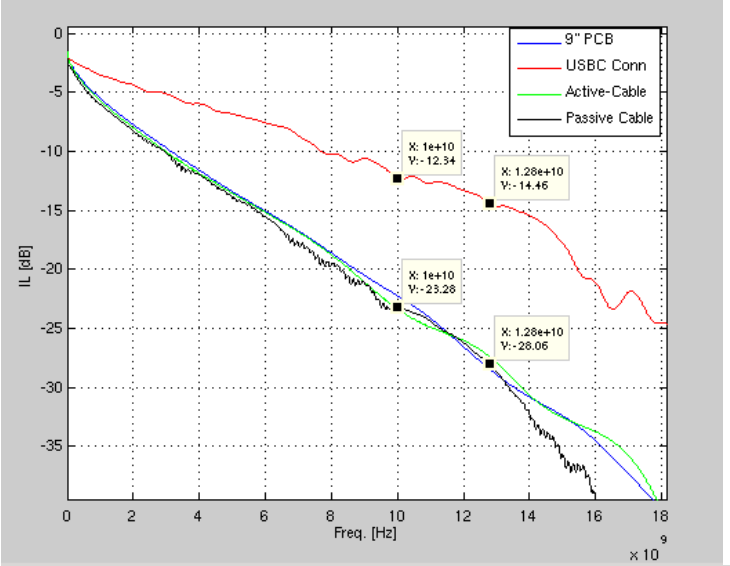


USB V2

USB4V2 Introduction

Goal : Double USB4 link speed with the existing ecosystem constraints

Signaling	NRZ	PAM -3	PAM -4
Baud Rate	40GB	25.6 GB	20 GB
Level Separation	1	0.5	0.33
Information	Symbol carries 1 bit	Symbol carries 1.57 bit	Symbol Carries 2 bit
IL	49 db	28.06db	23.28db



NRZ : IL too high

PAM-4 : Level separation doesn't allow uncoded BER of 10e-8

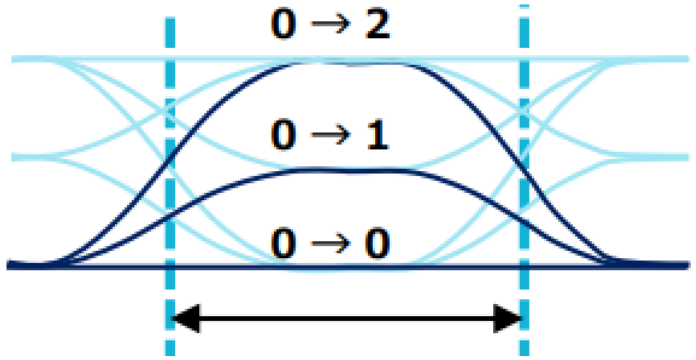
USB4V2 vs USB4V1

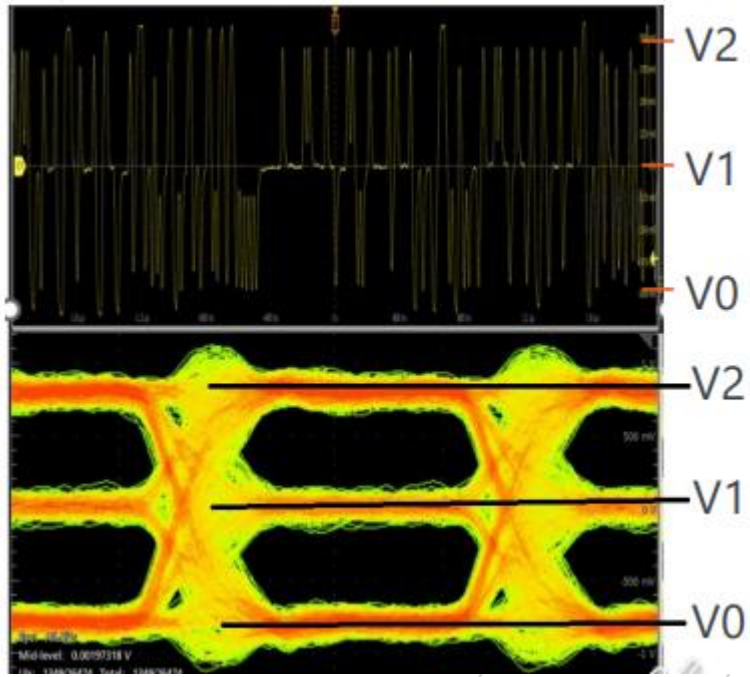
	Gen2	Gen3	Gen4
Data Transmission	NRZ		PAM-3 (3-level Pulse Amplitude Modulation)
Data Rate	10 Gbps	20 Gbps	25.6 Gbaud
Bits/UI	1	1	1.57(maps 7trits to 11 bits)
Data Transfer Rate/Lane	10Gbps	20Gbps	40 Gbps
Loss Target	5.5db	7.5db	9.5db
Test Signal	PRBS		PRTS7
Presets	16		41

PAM-3 Modulation

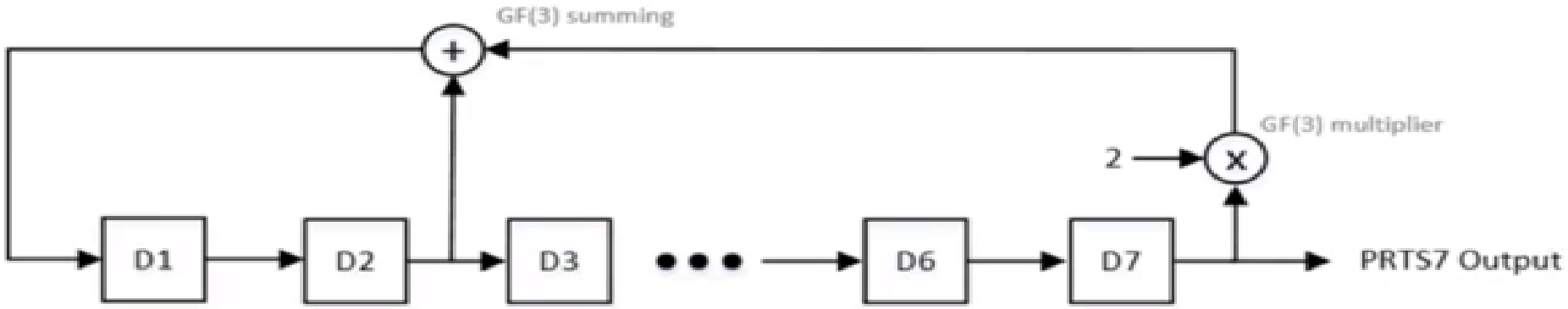
- 3-level Signaling
- Transmits 1.57 bits per UI
- Bandwidth requirement is 2/3rd of NRZ for same throughput of data
- 3 possible transitions instead of 2
- 7 Symbols transmit 11 bits

Level	Voltage
V2	max 250mV, min 175mV
V1	0 V
V0	min - 250mV, max - 175mV





PRTS7 Pattern



1. Pattern with 2186 (3^7 -1)Symbols (Note: PRBS7 is 2^7 -1)
2. Best Emulates Real Traffic
3. PRTS7 is generated by the equation $G(x)=1+X^2+2X^7$

Tx Design Considerations

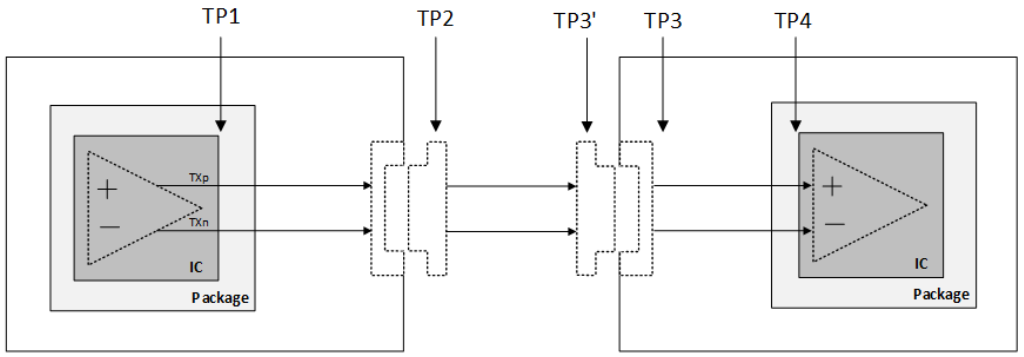
COMPLIANCE TEST POINTS

TP1: at the pins of the transmitter device

TP2: at the test interface on a test access fixture near end

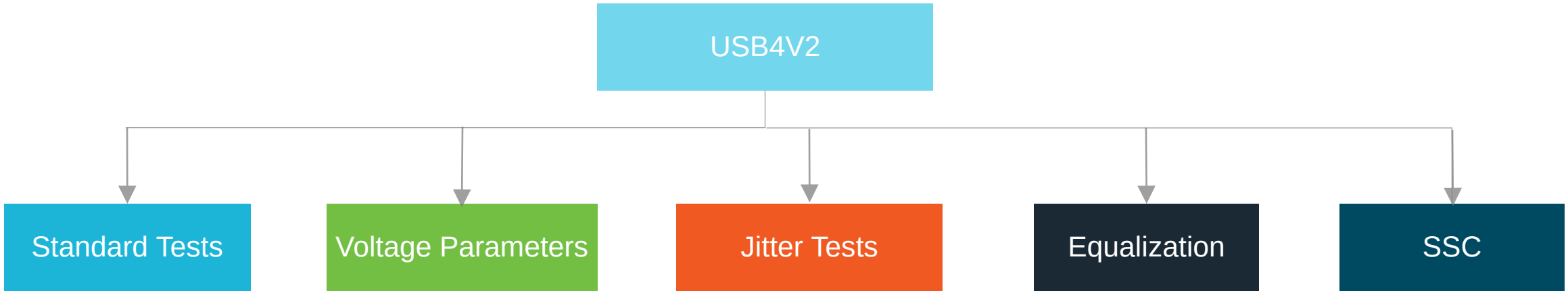
TP3: at the test interface on a test access fixture far end

TP4: at the pins of a receiving device



Tx Design Considerations

MEASUREMENTS



1. *UI*
2. *Lane to Lane Skew*
3. *Tx SNDR*
4. *TX ISI Margin*

1. *TX swing*
2. *Tx Pulse Peak*
3. *Tx Level Mismatch*
4. *Common Mode Noise*
5. *Tx Swing when Disabled*

1. *Uncorrelated Jitter (UJ)*
2. *Uncorrelated DJ (UDJ)*
3. *UDJ@RT pass band(UDJ_LF)*
4. *ODD_EVEN (DCD)*

1. *TX FFE*

1. *SSC Rate*
2. *SSC Down Spread*
3. *SSC slew rate*
4. *SSC Phase Deviation*

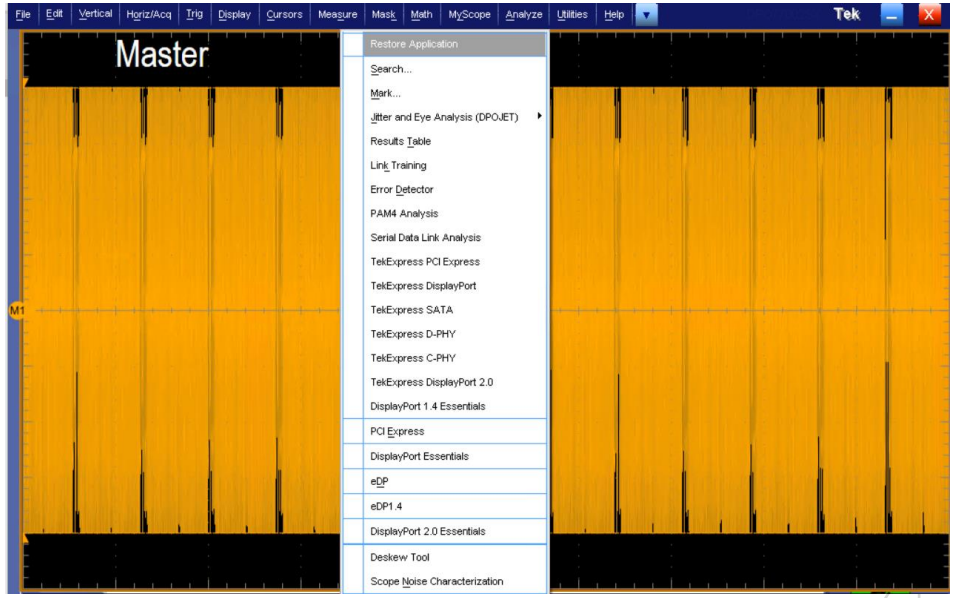
PAMJET: Tektronix PAM Tool

Unique Debugging Solution

PAMJET

HOW TO DEBUG COMPLIANCE FAILURE

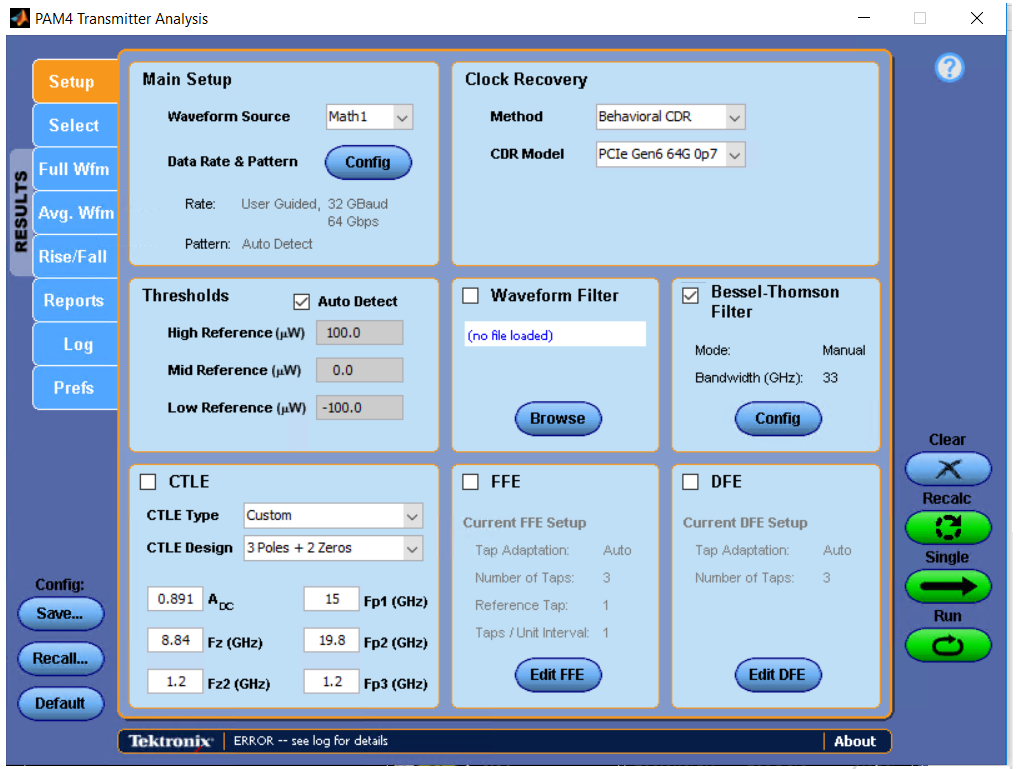
- PAMJET - Tektronix general purpose PAM signal analysis tool
- Includes the standard specific modules e.g. USB4V2
- Comprehensive Measurements for
  - Jitter Analysis
  - Eye Analysis
  - Amplitude Analysis
  - Timing Analysis
  - Period / Frequency



PAMJET

USB4V2 PLUGIN

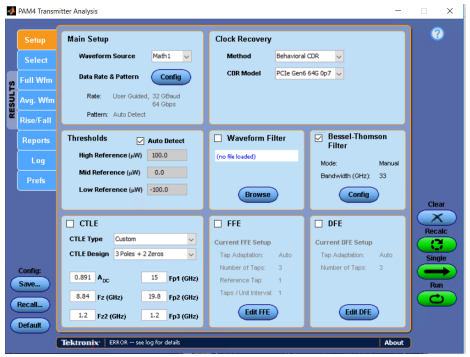
- Quickly analyze measurements before performing automated testing
- Vary measurement parameters and monitor behavior
- Add different plots to get deep insight into DUT characteristics
- Generate reports for reference



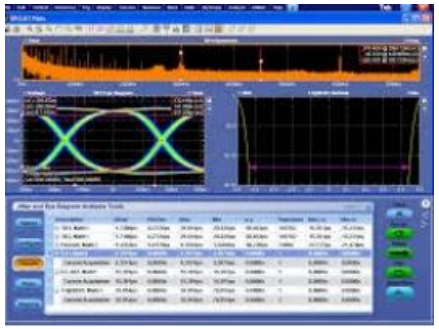
Tektronix USB4 Solution

USB4 Complete Solution

DEBUG



PAMJET



DPOJET

SDLA

COMPLIANCE

THANK YOU

Nitin Jhanwar

Nitin.Jhanwar@tektronix.com

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