TEKTRONIX
INNOVATION FORUM
2023
Engineering the Future

Addressing New DisplayPort v2.1 Testing Challenges

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DisplayPort 2.1

INTRO AND AGENDA

Topics:

- DisplayPort 2.1 (DP2.1) Overview
  - What does DP2.1 offer over previous versions?
- Compliance Testing
  - What are the requirements for DP2.1 certification?
- Testing Challenges
  - What is the main challenge with respect to compliance testing and certification?
- Overcoming Compliance Test Challenges
  - How can challenges be addressed and what improvement is possible?

DisplayPort 2.1

OBJECTIVES FOR THIS SESSION

Objectives:

- High-level understanding of DP2.1
  - DP2.1 revision basics
  - Differences from previous versions of DP
- Compliance Testing Requirements/Challenges
- Addressing DP2.1 compliance testing challenges

DisplayPort 2.1 Overview

DisplayPort 2.1 Overview

WHAT'S NEW?

Three new data rates

- UHBR10: 10Gbps
- UHBR135: 13.5Gbps
- UHBR20: 20Gbps

DP 2.1 enables up to 3X increase in data bandwidth performance

- DP2.1 will use 128b/132b encoding

DP 2.1 improves USB4 Tunneling performance

- DSC (Display Stream Compression) support mandatory.
  - USB4 Tunneling architecture is designed to combine multiple protocols onto a single physical interface
  - Exemptions exist for some devices (table 2-165 of DP2.1 spec)

DP 2.1 supports Standard DP, Type-C, and Mini DP connectors

DisplayPort 2.1 Overview

HOW DOES DP2.1 COMPARE TO PREVIOUS VERSIONS?

Parameter	DP 1.4a	DP 2.1	Comments
Data Rate (per lane)	8.1 Gbps (HBR3)	10 Gbps (UHBR10) 13.5 Gbps (UHBR135) 20 Gbps (UHBR20)	Backward compatible to all earlier DP versions
Encoding	8b/10b	128b/132	
DSC	Optional	Mandatory	
Max Resolution	5K@60fps 24bpp	10K@60fps 24bpp	fps: frames per second bpp: bits per pixel
Max Resolution (w/ DSC)	8K@60fps 30bpp	16K@60fps 30bpp	
Max payload (4 lanes)	25.92 Gbps	77.56 Gbps	~3X improvement

DisplayPort 2.1 Compliance Testing

DisplayPort 2.1 Compliance Testing

COMPLIANCE TEST POINTS

TP1: at the pins of the transmitter device

TP2: at the test interface on a test access fixture near end

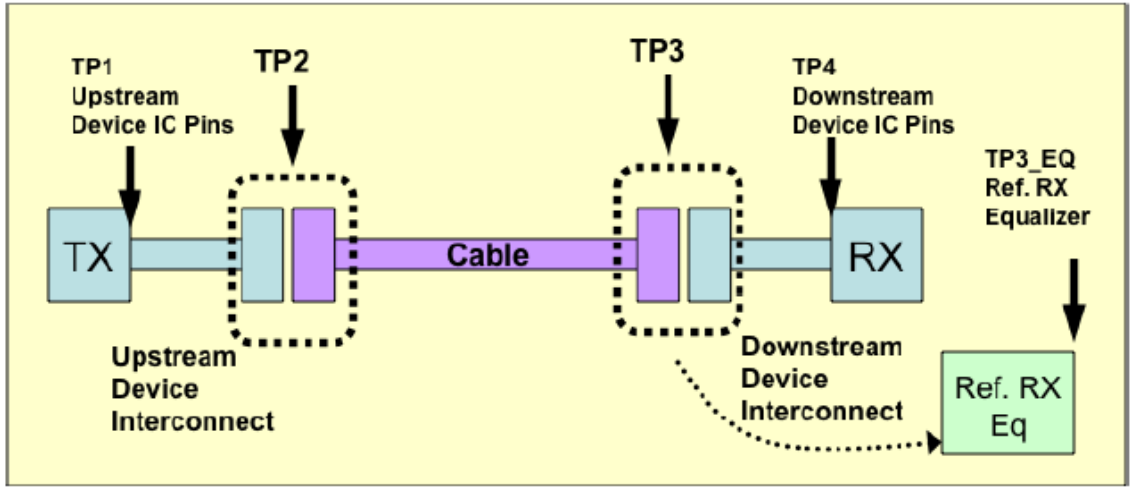
TP3: at the test interface on a test access fixture far end

TP3_EQ: TP3 with equalizer applied

TP4: at the pins of a receiving device

NORMATIVE test points

INFORMATIVE test points



DisplayPort 2.1 Compliance Testing

REQUIRED TESTS

UHBR10, UHBR 13.5 and UHBR 20		
Measurements	**TP2**	**TP3EQ**
Preset Optimization	☑	☑
Eye Height	☑	☑
Eye Width	☑	☑
Total Jitter (TJ)	☑	☑
Random Jitter (RJ)	☑	☑
Uncorrelated Deterministic Jitter (UDJ)	☑	☑
Low Frequency UDJ (LFUDJ)	☑	☑
Data Dependent Jitter (DDJ)	☑	☑
Uncorrelated Jitter (UJ)	☑	☑
SSC Phase Deviation	☑	
SSC Down Spread Rate	☑	
SSC Down Spread Range	☑	
SSC Slew Rate	☑	
Unit Interval (UI)	☑	
Bit Rate	☑	
Electrical Idle	☑	
AC Common Mode	☑	

DisplayPort 2.1 Testing Challenges

DisplayPort 2.1 Challenges

OBSTACLES TO COMPLIANCE TESTING

Challenges	Impact
Signal Integrity challenges (Data Rate changing from 8Gbps to 20Gbps)	Noise, crosstalk, and other signaling issues require low-noise acquisition
De-Embedding of Test Cables required in DP2.1 Testing • Test fixture De-embed is optional	Specialized HW/SW and expertise are required
Increased complexity in compliance test requirements: RBR, HBR, HBR2, HBR3, **UHBR10, UHBR135 & UHBR20** • TX preset calibration (16 Presets) • Optimal CTLE scan (10 CTLE's)	Test times are increased, costs for test lab certification also increase

DisplayPort 2.1 Challenges

PRESET AND CTLE_DFE TESTS FOR TP3_EQ

Preset and CTLE_DFE testing now required at TP3_EQ for UHBR10, UHBR13.5 and UHBR20

- Referred to as “Preset and CTLE-DFE Declaration”
- Only TP2 preset testing required previously
  - The preset that results in the lowest value of DDJ is used for all TP2 tests
- Adds acquisition/analysis time
  - 16 presets for all supported UHBR bandwidths
- CTLE and DFE selection also required
  - 10 CTLE’s for all supported UHBR bandwidths
- Preset and CTLE_DFE combination that provides the maximum eye area (EH x EW) is used for all TP3_EQ Eye and Jitter tests

DisplayPort 2.1 Challenges

PRESET AND CTLE_DFE TESTS FOR TP3_EQ

Test Time Example

- Single lane, Single Bandwidth for previous DP1.4a HBR3 Compliance Testing : ~ 1 hr
- Addition of Preset and CTLE_DFE tests at TP3_EQ increases test times ~2x-2.5x
- Well over a full day of testing would be required to complete all normative testing

Overcoming DisplayPort 2.1 Testing Challenges

DisplayPort 2.1 Challenges

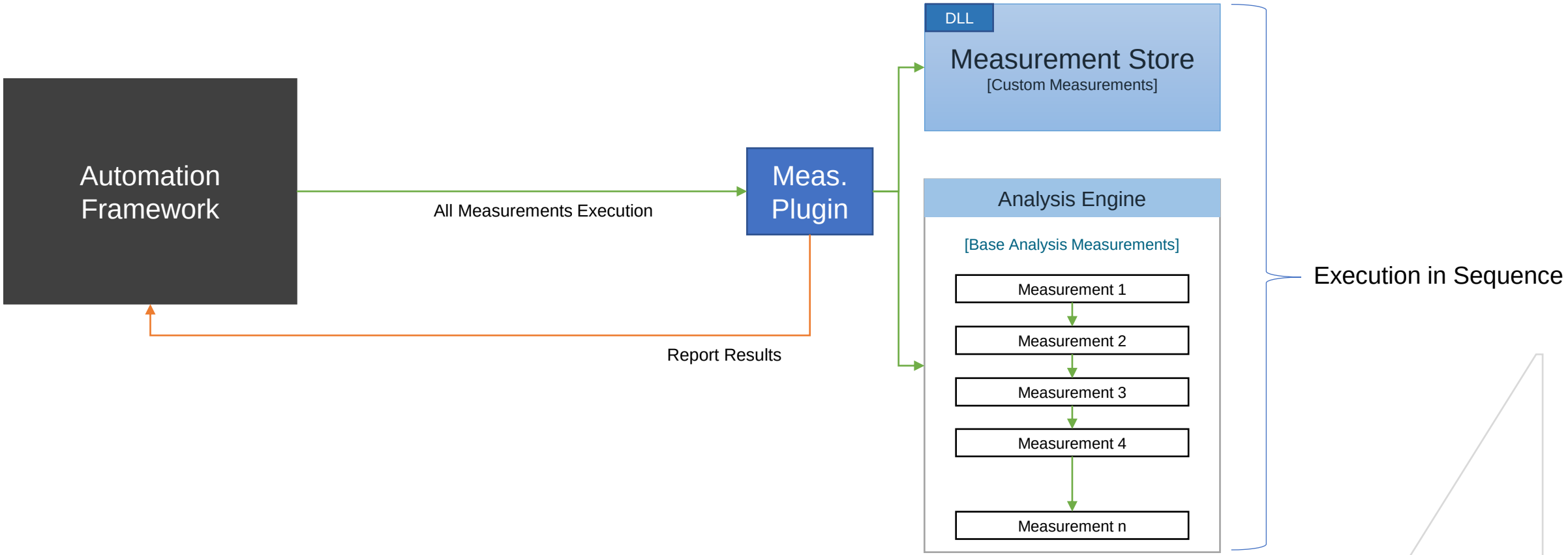
HOW CAN TEST TIMES BE IMPROVED?

SW Analysis

- Test times strongly tied to SW analysis
- Current solutions have a very linear analysis methods
  - Single instance of analysis SW, processing single waveform data sequentially

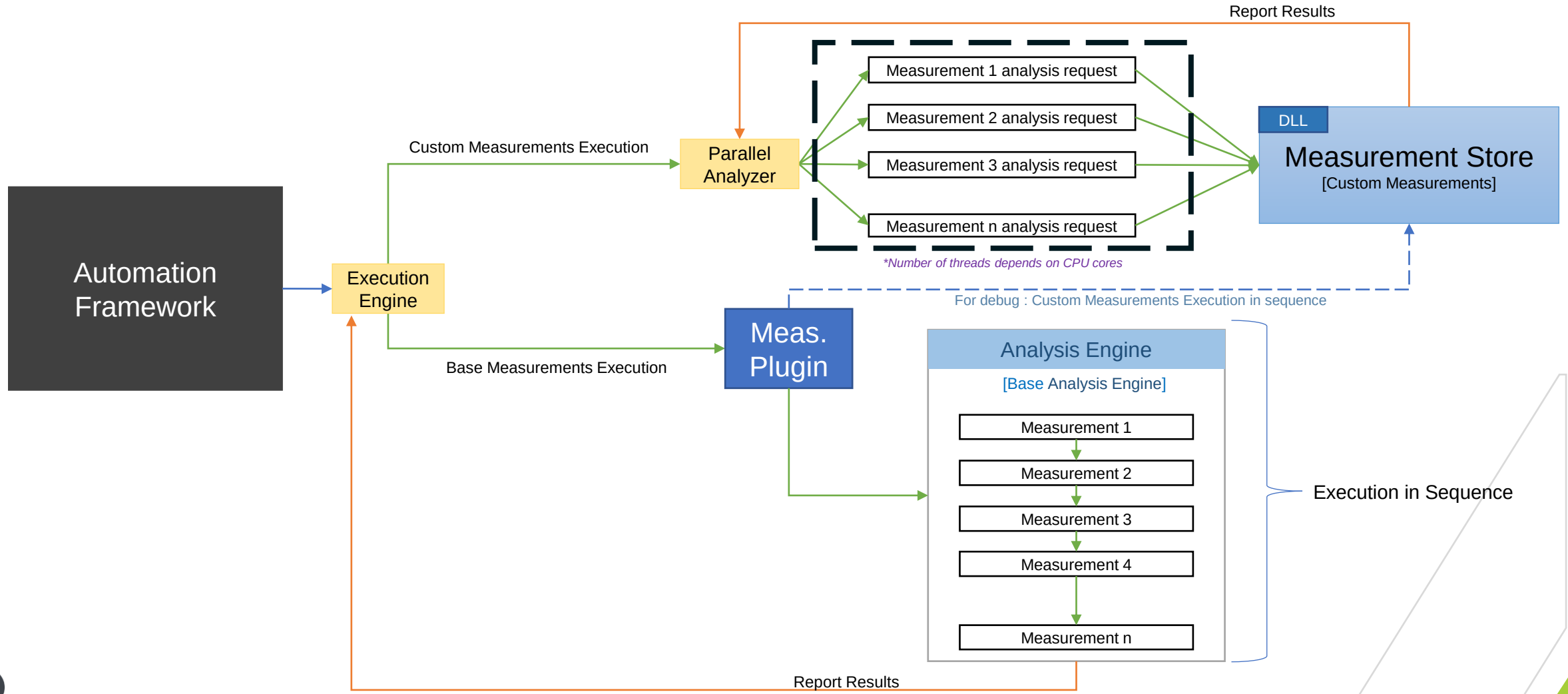
DisplayPort 2.1 Challenges

CURRENT EXECUTION ARCHITECTURE



DisplayPort 2.1 Challenges

PROPOSED EXECUTION ARCHITECTURE



DisplayPort 2.1 Challenges

PROPOSED EXECUTION ARCHITECTURE

Experimental Results…

- Based on internal and external prototype testing
  - Collaboration with several customers
- Test Time Improvements
  - Current results show **~ 3x improvement** over previous automation/execution architecture
  - Repeatable across multiple DP2.1 DUT's

Availability…

- Beta available now, under NDA
- Contact your Tektronix Account Manager for details

Summary

DisplayPort 2.1

SUMMARY

DisplayPort 2.1 (DP2.1) Overview

- Basic additions and Differences from Previous versions

Compliance Testing

- Requirements for DP2.1 certification

Testing Challenges

- Among all challenges, test times have greatest overall impact

Overcoming Compliance Test Challenges

- Solution proposal and results
- Prototype/Beta availability

THANK YOU

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