TEKTRONIX
INNOVATION FORUM
2022
Accelerating Progress

MIPI Interfaces, D-PHY, C-PHY and M-PHY: Debug and Validation

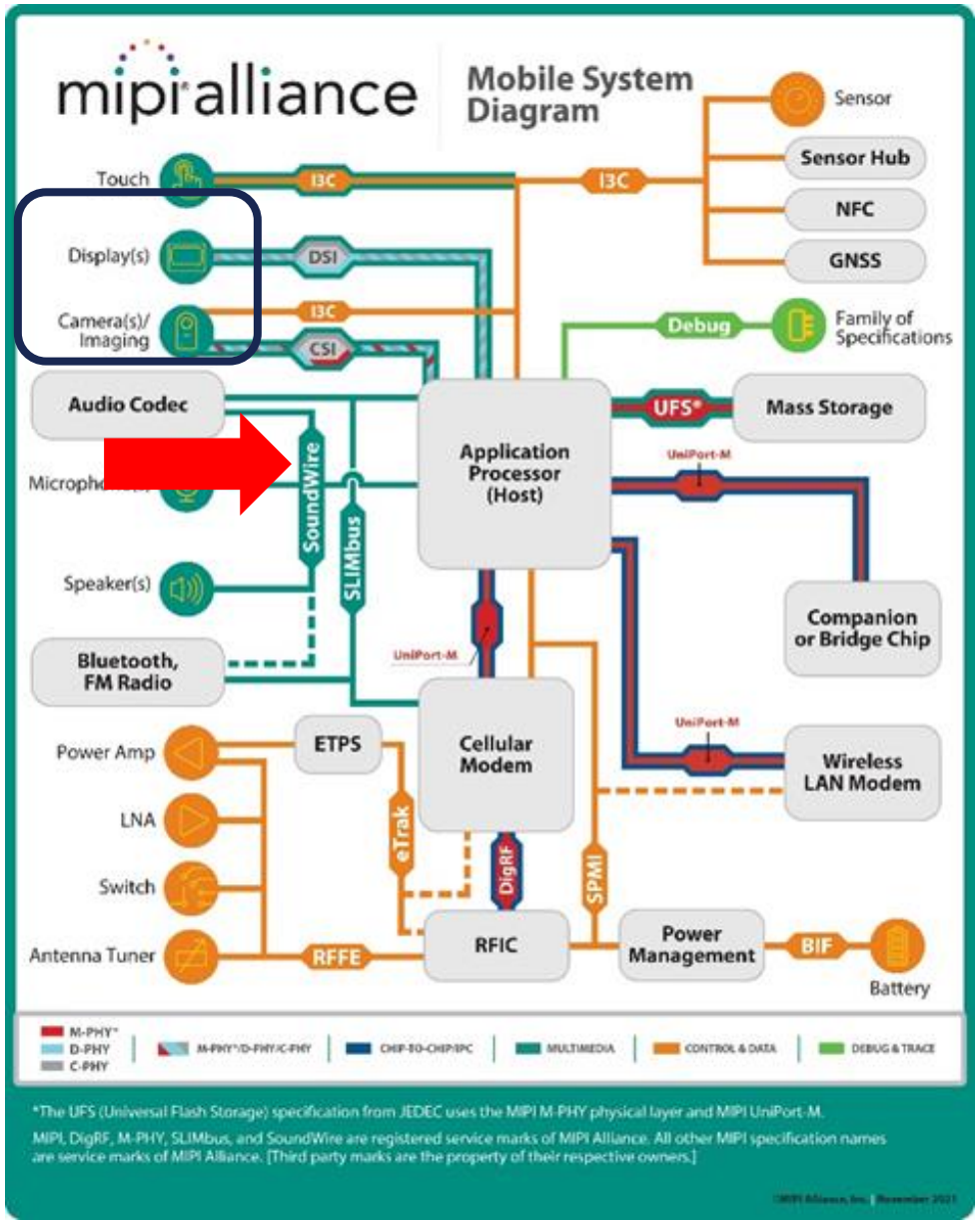
Ravi Malladi, Product Manager-MIPI
Gajendra K Patro, PL Solutions Engineer

What are MIPI D-PHY, C-PHY, and M-PHY?

MIPI : Consortium that develops the interfaces in mobile devices

D-PHY – Physical layer connecting the display or camera to the application processor in mobile / portable devices
C-PHY – Physical layer connecting the camera to the application Processor
M-PHY – Physical layer Inter-chip/ Processor communication

Feature	M-PHY v4.1	D-PHY v2.1	C-PHY v2.0
No of lanes	1(+)	4	3
Clock	-	1	-
Max. Data Rate	11.6Gbps	4.5Gbps	8Gsps
No of tests	46	64	43
Eye Diagram	√	√	√
De-embed	√	Yes>2.5Gbps	√
Equalization	√	x	√



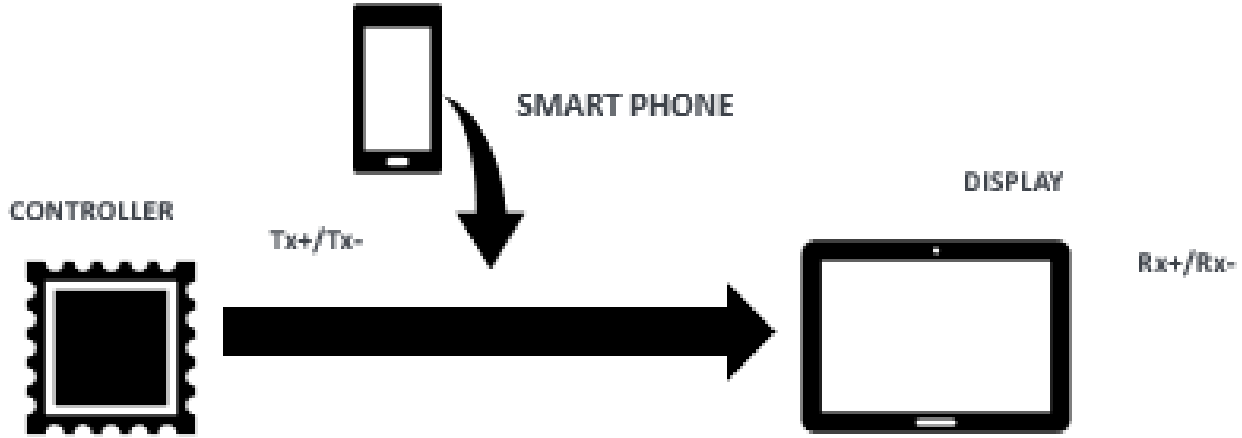
Source: MIPI Alliance

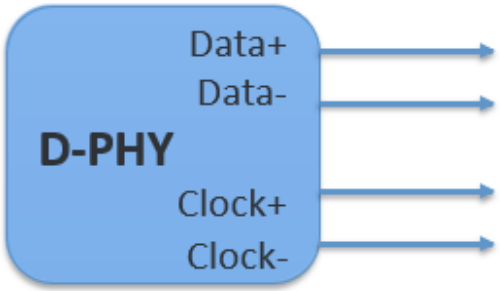
D-PHY

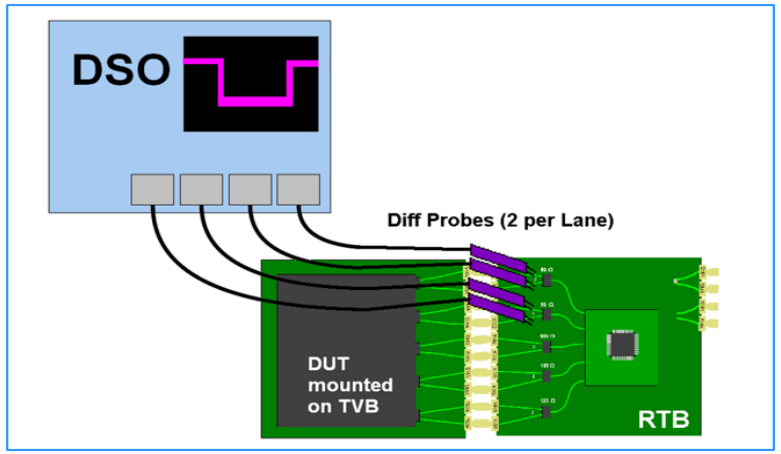
Technology Overview of D-PHY Signaling

ELECTRICAL SIGNALING OVERVIEW

- Data & Clock Lane
  - Data+, Data- & Clock+, Clock-
    - Minimum 4 wires for Single ended connections
    - Minimum 3 wires for Differential Clock (Continues)
- Lane operating modes
  - High Speed Mode(HS)
    - Terminated
    - Low swing, Differential signal
    - Non-Return to Zero (NRZ) coding
    - Data transmission
  - Low Power Mode(LP)
    - Non-Terminated
    - Single-ended transmission.



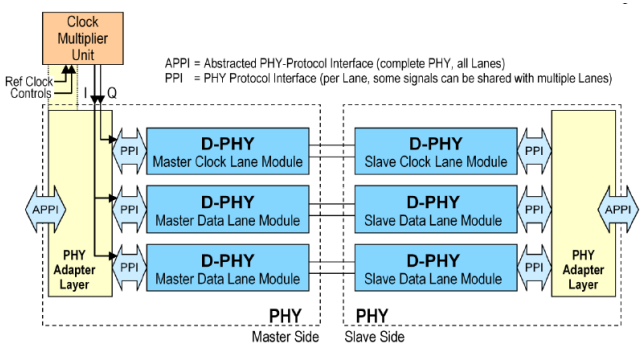




Technology Overview of D-PHY Signaling

D-PHY SPECIFICATIONS DESCRIBES PHY FOR ELECTRICAL AND INTERCONNECTS, ESPECIALLY SUITED FOR CAMERA OR DISPLAY DATA

- Source synchronous Master/Slave interface
- Two operating modes
  - Low Power (LP) – high voltage, unterminated
  - High Speed (HS) – LVDS signalling, with termination at both ends
- A link has a clock lane and at least one data lane
  - Differential signalling during HS mode
  - Single Ended signalling during LP mode
  - Max data rates up to 2.5Gbps with DDR clocking



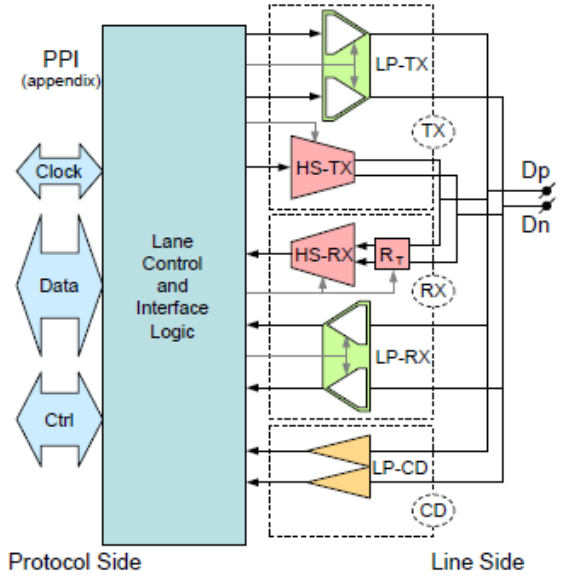


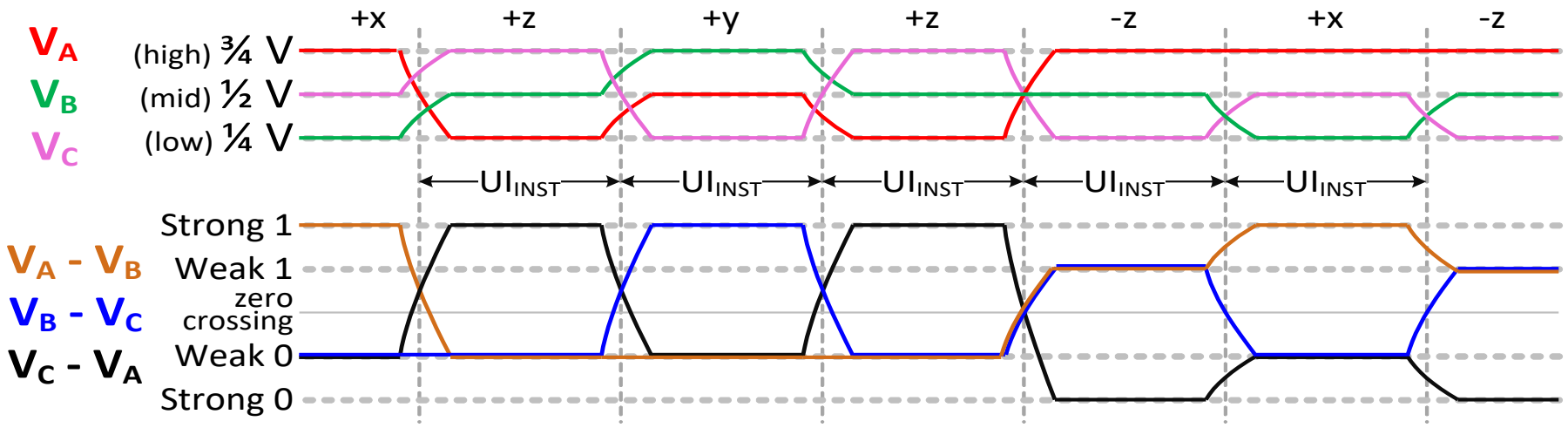
Figure 1 Universal Lane Module Functions

Images in the slide are copyright of MIPI.org

C-PHY

C-PHY Signaling

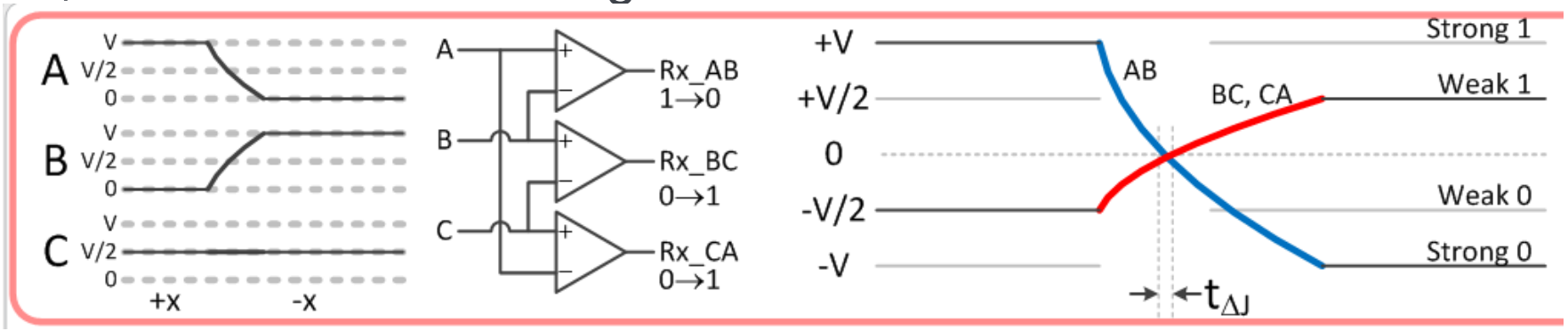
- The transmitter uses 3-level signaling. V_{HIGH} , V_{MID} & V_{LOW}
- 3-level Signal transmitted over 3 wires as V_A, V_B, and V_C
- Level on any wire is different from the other two.
- The 3-wire Trio is called a Lane. (Signals are V_A, V_B, and V_C)
- Receiver sees three voltages as differential V_{AB}, V_{BC}, and V_{CA}
- Receivers detect only positive or negative, not the weak or strong level.



C-PHY Signal Levels

- VA, VB, VC
  - HS Line Voltage { High, Low, Mid }
  - { V, 0, V/2 }

- VAB, VBC, VCA – Differential Signals



Source: MIPI Workgroup Proceedings

M-PHY

M-PHY HS Gears, PWM Gears & SYS

High Speed

High Speed Gears	Rate A Series (Mbps)	Rate B Series (Mbps)
HS-G1	1248	1457.6
HS-G2	2496	2915.2
HS-G3	4992	5830.4
HS-G4	9.984	11.648
HS-G5	**19.968**	**23.3472**

PWM (TYPE I)

PWM Gears	Min (Mbps)	Max(Mbps)
PWM-G0	0.01	3
PWM-G1	3	9
PWM-G2	6	18
PWM-G3	12	36
PWM-G4	24	72
PWM-G5	48	144
PWM-G6	96	288
PWM-G7	192	576

UFS4.x Ref-Clock

- 19.2 MHz
- 26M
- 38 MHz
- 52 MHZ

SYS (TYPE II)

Transmission Rate : integer division of the shared reference clock frequency

- 26 MHz
- 38.4MHZ
- 52MHZ

M-PHY Multi Lane

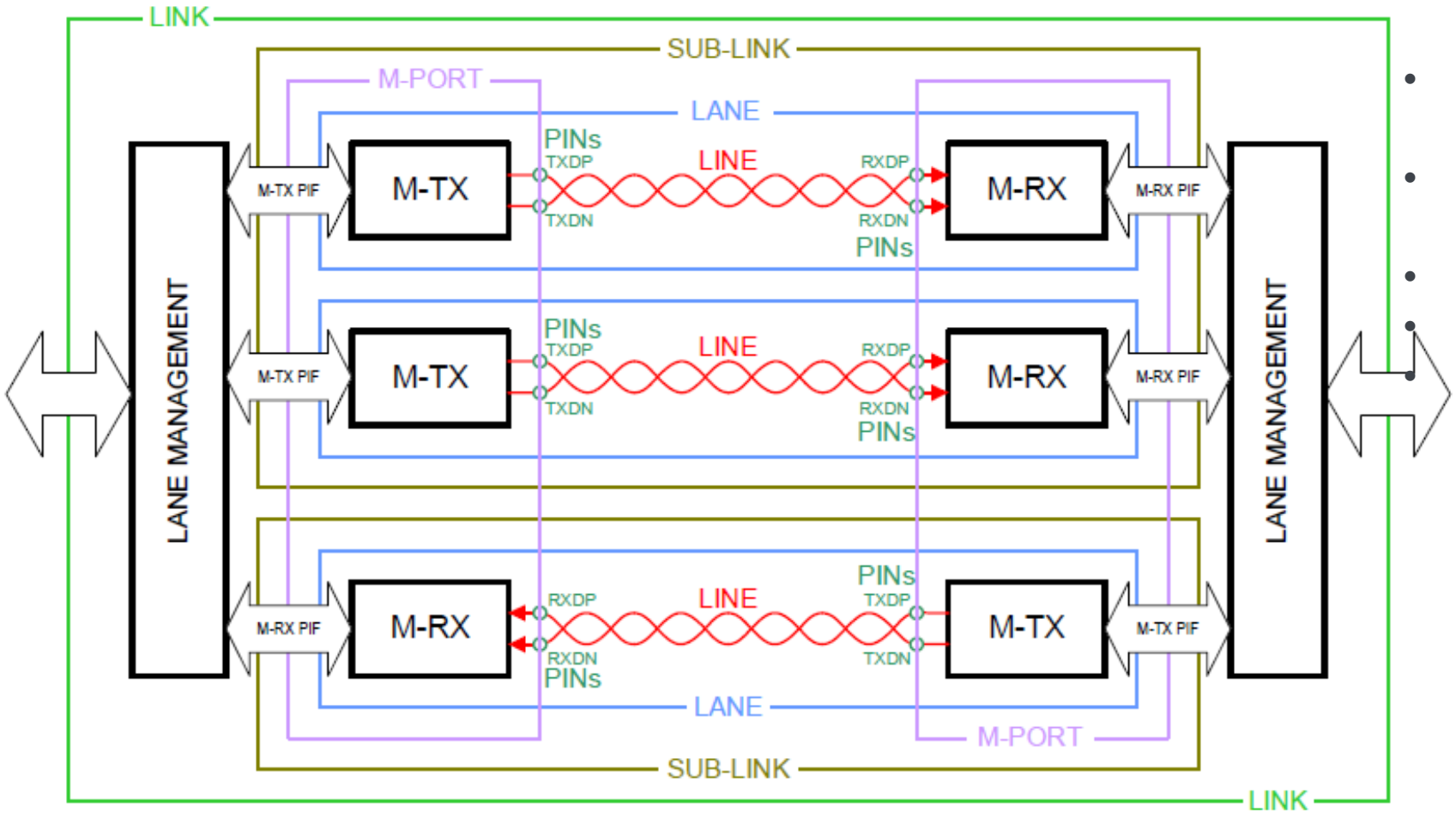
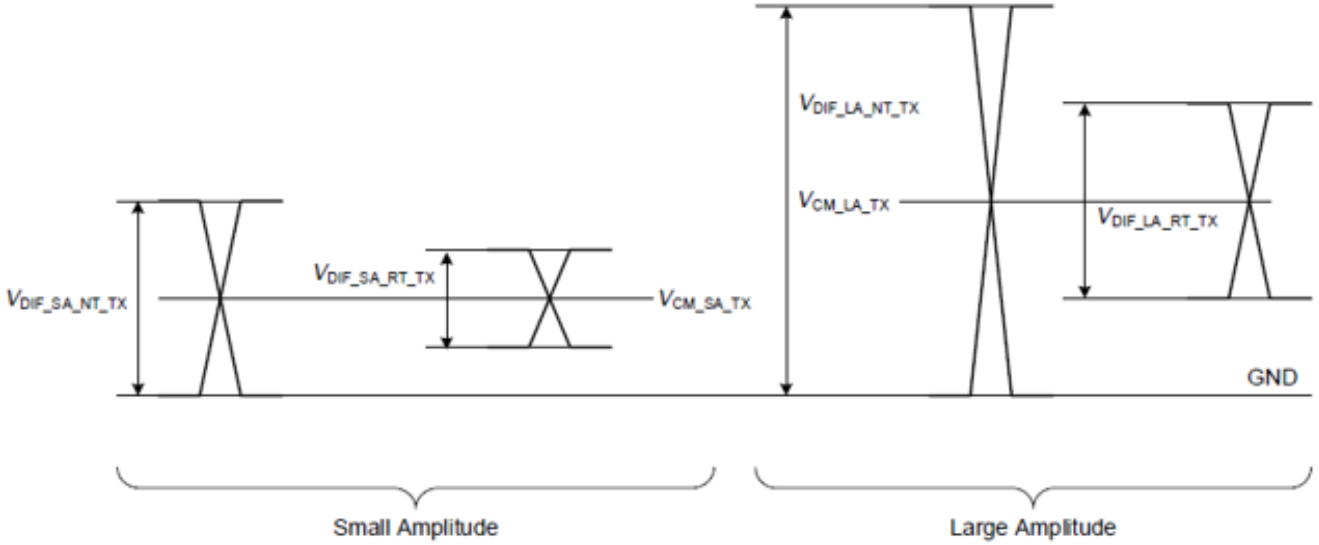


Figure 1 M-PHY Lane Example

- Sub-Link - Manage one or more lanes
- Every “LANE” can have Multiple “LINE” configuration.
- LINK-Connects M-PHY Transmitter to an M-PHY Receiver.
- Lane-Operation defined in the Protocol.

M-PHY Signaling



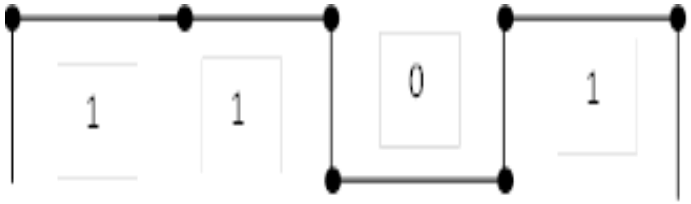
- Burst or Continuous signaling.
- In High-Speed mode each Lane is terminated on both sides.
- The Link includes a High-Speed signaling mode for fast-data traffic and a low-power signaling mode for control purposes.

M-TX Signal Levels

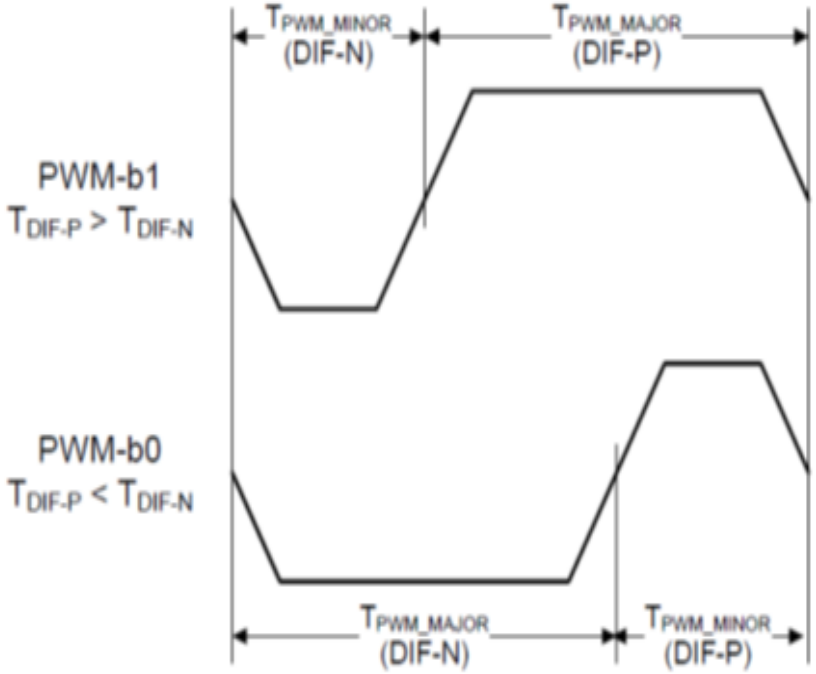
$V_{DIF\_DC\_LA\_RT\_TX}$	240	300	mV	Large Amplitude differential TX DC voltage when the M-TX is terminated[8]. Defined for R_{REF_RT}[1] and test pattern[2]. See
$V_{DIF\_AC\_LA\_RT\_TX}$[3]	220	310	mV	Large Amplitude differential TX AC voltage when the M-TX is terminated[8]. Defined for R_{REF_RT}[1] and CRPAT4. See

M-PHY Signaling Modes

- NRZ - High Speed (HS) Mode



- PWM - Low Speed (LS) Mode



- TYPE I Device
  - PWM (LS Mode)
- TYPE II Device
  - SYS which is NRZ (LS Mode)
- UFS Clock
  - Clock

Encoding Setup

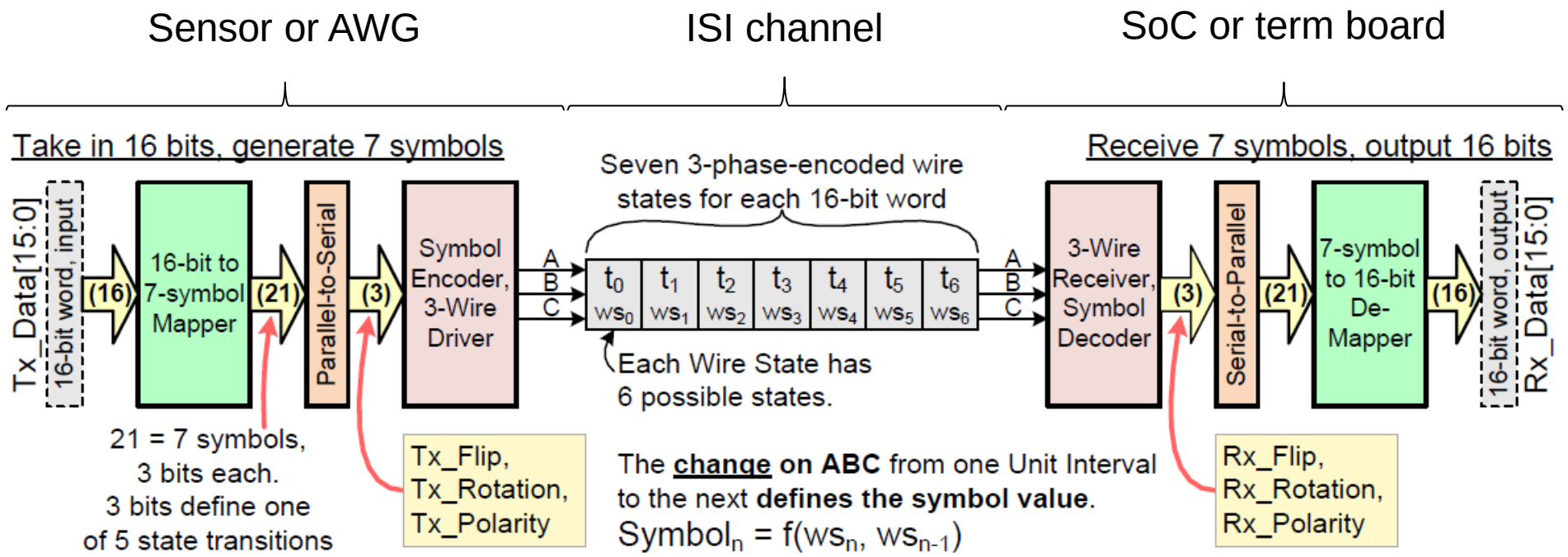


Figure 3 End-to-End Transmission of Data, 16-bit Word Conversion to Channel States

M-PHY Measurements

LIST OF CTS MEASUREMENTS FOR TRANSMITTER TESTING: HS, PWM, UFS AND SYS

	Group 1 HS-TX	Test Names	
1	Group 1 HS-TX REQUIREMENTS	Test 1.1.1-HSTX Unit Interval and Frequency Offset	New
2	Group 1 HS-TX REQUIREMENTS	Test 1.1.2-HSTX Common-Mode AC Power Spectral Magnitude Limit 1	
3	Group 1 HS-TX REQUIREMENTS	Test 1.1.3-HSTX PREPARE Length	
4	Group 1 HS-TX REQUIREMENTS	Test 1.1.4-HSTX Common Mode DC Output Voltage Amplitude	
5	Group 1 HS-TX REQUIREMENTS	Test 1.1.5-HSTX Differential DC Output Voltage Amplitude	
6	Group 1 HS-TX REQUIREMENTS	Test 1.1.6-HSTX G1 and G2 Differential AC Eye	
7	Group 1 HS-TX REQUIREMENTS	Test 1.1.7-HSTX G3, G4, and G5 Differential AC Eye	New
8	Group 1 HS-TX REQUIREMENTS	Test 1.1.8-HSTX 20-80% Rise and Fall Times	
9	Group 1 HS-TX REQUIREMENTS	Test 1.1.9-HSTX Lane-to-Lane	New
10	Group 1 HS-TX REQUIREMENTS	Test 1.1.10-HS-TX Slew Rate Control Range	
11	Group 1 HS-TX REQUIREMENTS	Test 1.1.11-HS-TX Slew Rate Monotonicity	
12	Group 1 HS-TX REQUIREMENTS	Test 1.1.12-HS-TX Slew Rate Resolution	
13	Group 1 HS-TX REQUIREMENTS	Test 1.1.13-HS-TX Intra-Lane Output Skew	New
14	Group 1 HS-TX REQUIREMENTS	Test 1.1.14-HS-TX Transmitter Pulse Width	New
15	Group 1 HS-TX REQUIREMENTS	Test 1.1.15-HS-TX Total Jitter	New
16	Group 1 HS-TX REQUIREMENTS	Test 1.1.16-HS-TX Short-Term Total Jitter	New
17	Group 1 HS-TX REQUIREMENTS	Test 1.1.17-HS-TX Deterministic Jitter	New
18	Group 1 HS-TX REQUIREMENTS	Test 1.1.18-HS-TX Short term Deterministic Jitter	New
19	Group 1 HS-TX REQUIREMENTS	BER Eye Contour	New

M-PHY Measurements

LIST OF CTS MEASUREMENTS FOR TRANSMITTER TESTING: HS, PWM AND UFS

	Group 2 PWM-TX	Test Names
1	Group 2 PWM-TX REQUIREMENTS	Test 1.2.1 PWM-TX Transmit Bit Duration (TPWM_TX)
2	Group 2 PWM-TX REQUIREMENTS	Test 1.2.2 PWM-TX Transmit Ratio (kPWM_TX)
3	Group 2 PWM-TX REQUIREMENTS	Test 1.2.3 PWM-TX PREPARE Length (TPWM_PREPARE)
4	Group 2 PWM-TX REQUIREMENTS	Test 1.2.4 PWM-TX Common Mode DC Output Voltage (VCM_TX)
5	Group 2 PWM-TX REQUIREMENTS	Test 1.2.5 PWM-TX Differential DC Output Voltage Amplitude (VDIF_DC_TX)
6	Group 2 PWM-TX REQUIREMENTS	Test 1.2.6 PWM-TX Minimum Differential AC Eye Opening (TEYE_TX) (OBSOLETE)
7	Group 2 PWM-TX REQUIREMENTS	Test 1.2.7 PWM-TX Maximum Differential AC Output Voltage Amplitude (VDIF_AC_TX)
8	Group 2 PWM-TX REQUIREMENTS	Test 1.2.8 PWM-TX 20/80% Rise and Fall Times (TR_PWM_TX and TF_PWM_TX)

	Group USF4-Ref-Clock	Test Names	New
1	USF4-Ref-Clock-Measurement	Frequency	
2	USF4-Ref-Clock-Measurement	Frequency Error	
3	USF4-Ref-Clock-Measurement	Input High Voltage	
4	USF4-Ref-Clock-Measurement	Input Low Voltage	
5	USF4-Ref-Clock-Measurement	Input Clock Rise Time	
6	USF4-Ref-Clock-Measurement	Input Clock Fall Time	
7	USF4-Ref-Clock-Measurement	Duty Cycle	
8	USF4-Ref-Clock-Measurement	Random Jitter	
9	USF4-Ref-Clock-Measurement	Deterministic Jitter	

M-PHY Measurements

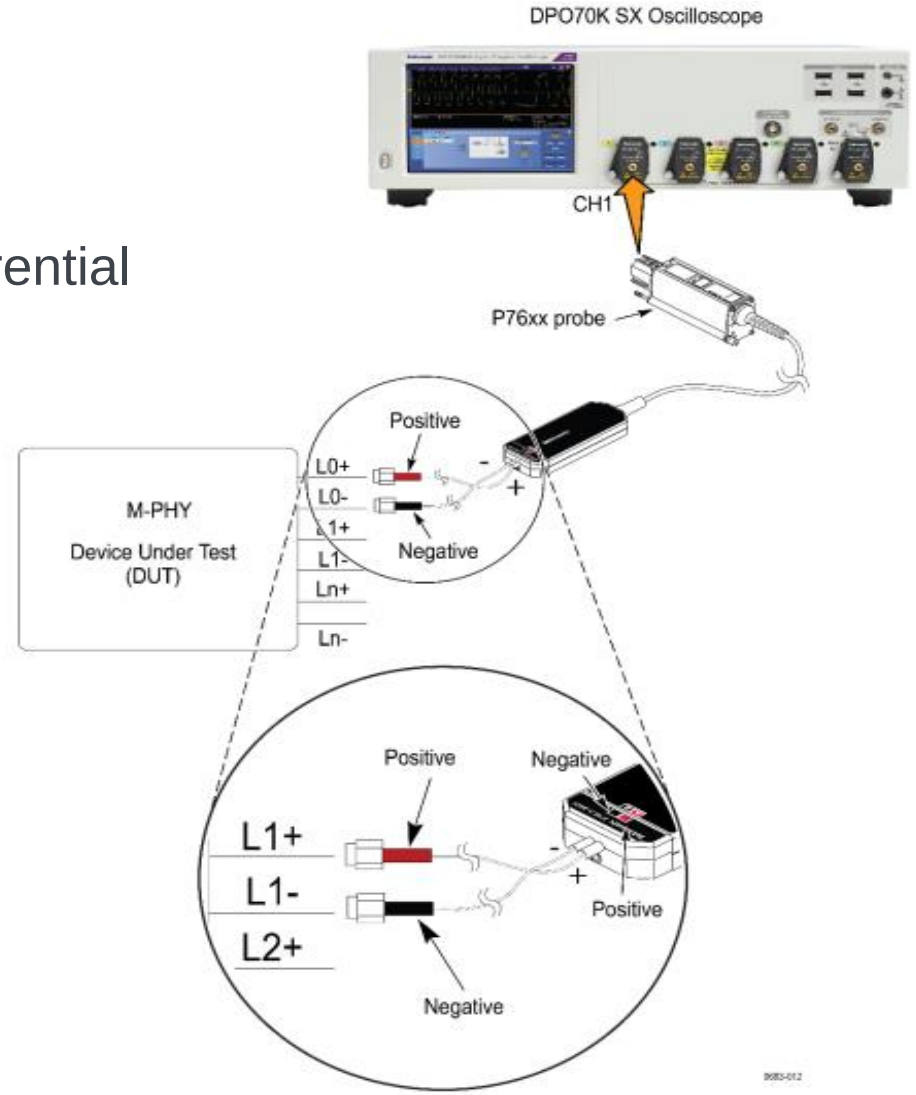
LIST OF CTS MEASUREMENTS FOR TRANSMITTER TESTING: HS, PWM AND UFS

	Group -SYS (System clock) measurements	Test Names
1	SYS (System clock) measurements	Test 1.3.1 – SYS-TX Unit Interval and Frequency Offset
2	SYS (System clock) measurements	Test 1.3.2 – SYS-TX RefClk Frequency
3	SYS (System clock) measurements	Test 1.3.3 – SYS-TX PREPARE Length
4	SYS (System clock) measurements	Test 1.3.4 – SYS-TX Common Mode DC Output Voltage Amplitude
5	SYS (System clock) measurements	Test 1.3.5 – SYS-TX-Differential DC Output Voltage Amplitude test
6	SYS (System clock) measurements	Test 1.3.7 – SYS-TX Maximum Differential AC Output Voltage Amplitude
7	SYS (System clock) measurements	Test 1.3.8 – SYS-TX 20/80% Rise and Fall Times
8	SYS (System clock) measurements	Test 1.3.9 – SYS-TX Lane-to-Lane Skew

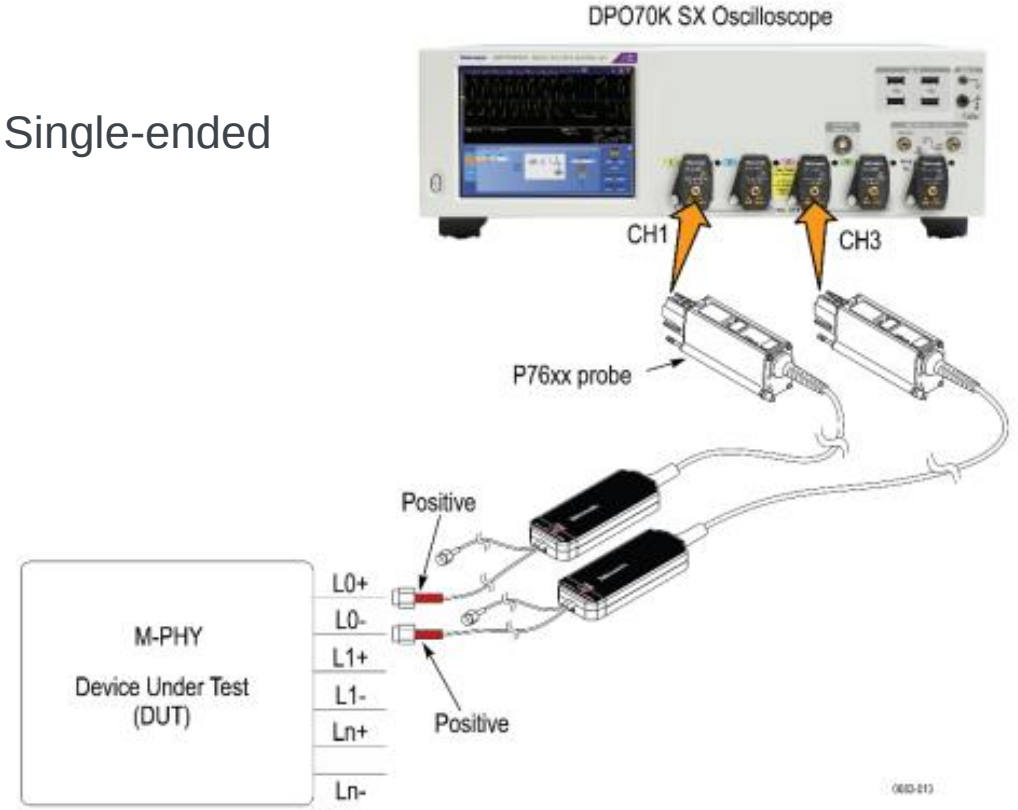
M-PHY Measurements

M-PHY CONNECTION DIAGRAM FOR HS MEASUREMENTS

Differential



Single-ended



Elements of Tx Validation/Debug

ESSENTIALS OF MIPI TESTING

	D-PHY v2.1	C-PHY v2.0	M-PHY Gear 5
Test Methodology	1.Waveform / Pattern / Region 2.Measurement Procedure/ Post Processing Algo		
Test Equipment: Oscilloscopes, Probes and accessories and Fixtures	1. Scope: BW* > 13GHz 2. Probes: BW>13GHz 3. Fixtures 4.Softwares(Conformance +Decode)	1. Scope: BW*>20GHz 2. Probes: 20GHz and above 3. Fixtures 4.Softwares(Conformance+Decode)	1. Scope: BW > 33GHz 2. Probes: BW> 33GHz 3.Softwares(Conformance)
Test Modes/Test Points	• Escape Mode(LP) • Burst Mode(HS) • LP-HS Transition • Channel (Long/Short/Standard)	• Escape Mode(LP) • Burst Mode(HS) • LP-HS Transition • Protocol verification (Preamble/Sync etc.) • Channel (Long/Short/Standard)	• CRPAT(HS) • HS Continuous / Burst • PWM/ SYS • Reference channels S4p files/ filter files

*Works on Lower bandwidth for sub rates

Tx Validation Challenges

D-PHY V2.1

- Variable Data rate up to 4.5Gb/s
  - 80 Mbps to 4.5Gbps
- Eye diagram and jitter measurements
  - Tx Equalization by de-emphasis
- Spread-spectrum clocking
- Embed channel insertion loss
- LP Mode
  - Slew rate measurements
  - Bus Turn Around (BTA) test
    - User intervention to enable mode and measure

Tx Validation Challenges

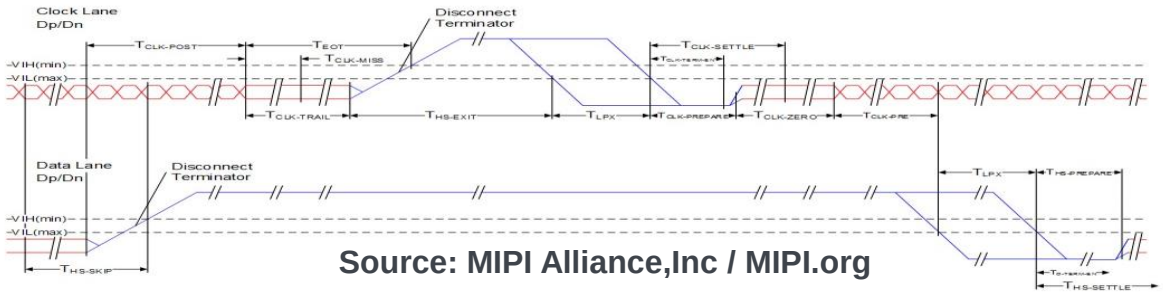
C-PHY V2.0

- Data rate up to 8.0Gs/s
  - 80 Msps to 8.0 Gsps with support for intermediate Symbol rates
- Eye diagram and jitter measurements
  - Tx Equalization and De-embed Channel
- Embed channel insertion loss (Long/Short and Standard)
- Protocol based measurements (Preamble and Sync)
- LP Mode
  - Slew rate measurements
  - Bus Turn Around (BTA) test
    - User intervention to enable mode and measure

Tx Validation Challenges *(cont.)*

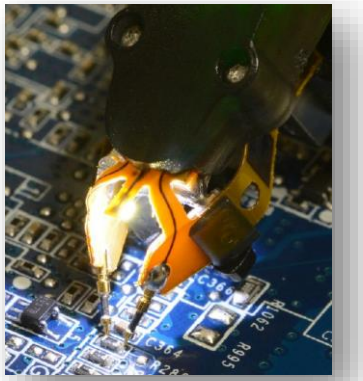
COMMON CHALLENGES IN D-PHY AND C-PHY

- Dynamic switching of terminations between LP and HS mode



Source: MIPI Alliance,Inc / MIPI.org

- Waveform post processing to discern the LP-HS transitions
- Burst Mode timing measurements
- Measurements on clock and data lanes-D-PHY and Data lane for C-PHY
  - Voltage and Timing parameters
- Probing
  - HS & LP transmission without loading the bus
  - Access to tight test locations

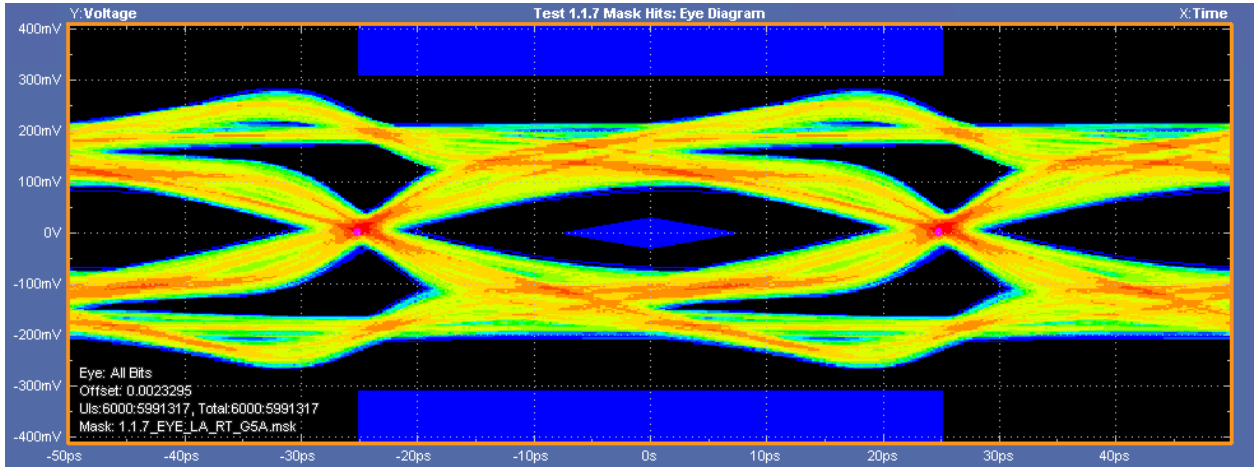


Tx Validation Challenges

M-PHY GEAR 5

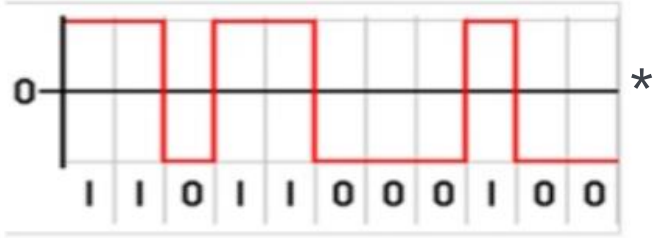
- Data rate up to 23.34 Gbps
  - 1.248 Gbps to ~23.34 Gbps
- Eye diagram and jitter measurements
  - Receiver Equalization using CTLE and DFE
- Embed channel insertion loss
- LP & HS Mode
  - LP: PWM / SYS modes

HS Gear 5 Eye Diagram



High-Speed Gears

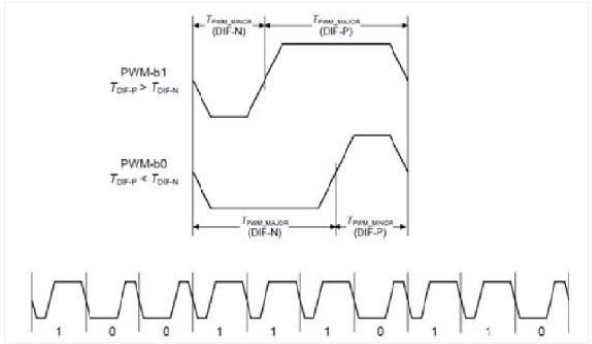
- Non-Return-to-Zero(NRZ)
- Small and large amplitude modes



*

Low-Speed Gears

- Pulse-Width-Modulation (PWM)
- Self-Clocking



*

Probing

- Users want to remove probe distortion from their measurements through de-embedding
  - P7700 is the ***industry's first*** probe and tips to be characterized with S-parameters
    - S-parameters file saved in each probe and tip
    - Uploaded to scope when probe or tip is attached
    - Others only calibrate to the probe body and use a nominal filter for the tip
  - P7700 automates the de-embedding of the probe with a one click connection to the scope
    - Others require multi-step manual process to achieve the same level of calibration

P7700

P77STFLXA

Eye Diagram Measurements in D-PHY v2.1 and C-PHY v2.0

Tx Test: HS-Tx Data and Clock

D-PHY V2.1 TRANSMITTER EYE DIAGRAM

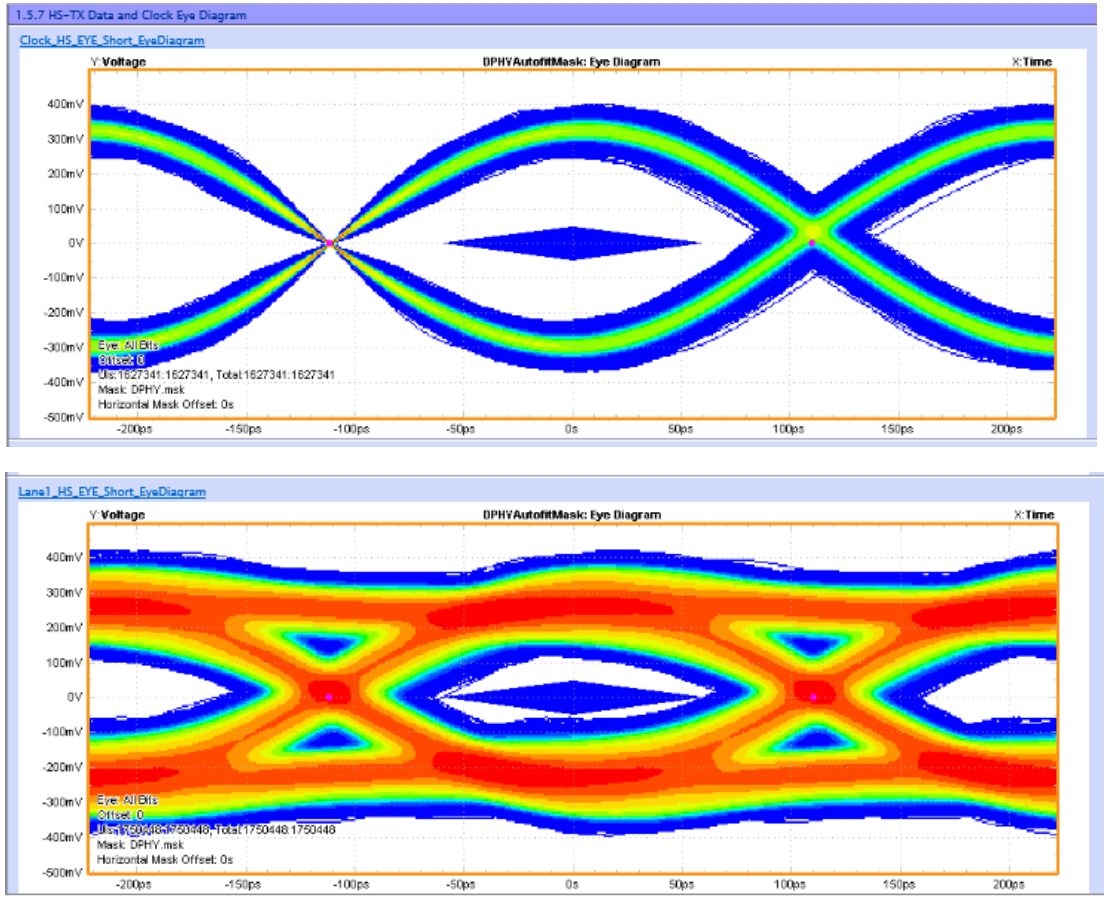
Test ID 1.5.7

- Applicable for 1.5Gbps < Data Rate < 4.5Gbps
- Measured at the end of reference channel
    1. Standard: Normative
    2. Long: Informative
    3. Short: Informative
- Pattern: Continuous HS data (Recommended) or Data from multiple bursts.

(PRBS9 recommended Pattern for Data)

- Support for Deemphasis
- Measurement using random test pattern of 3 million UI
- Mask: Yes, Diamond

Eye Diagram: Mandatory

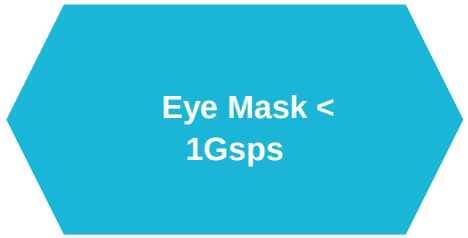


Tx Test: HS-Tx Eye Diagram

C-PHY V2.0 TRANSMITTER EYE DIAGRAM: MASKS BASED ON SYMBOL RATE

Test ID 1.2.21

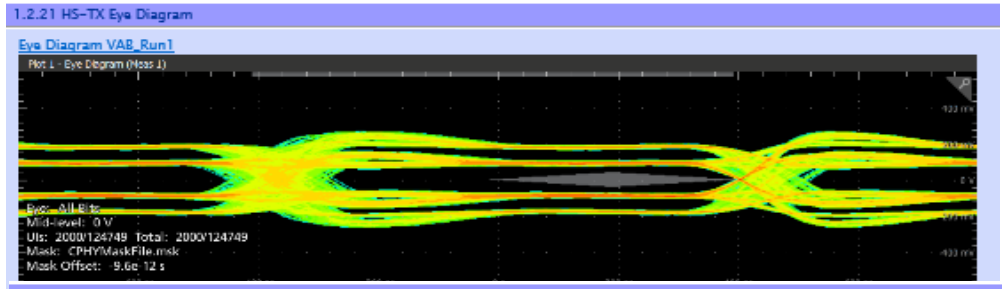
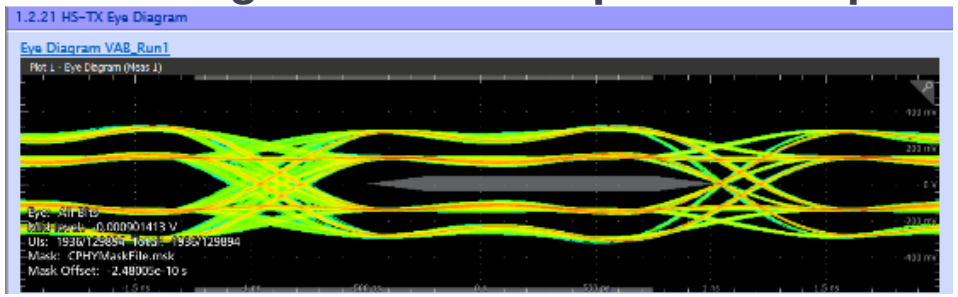
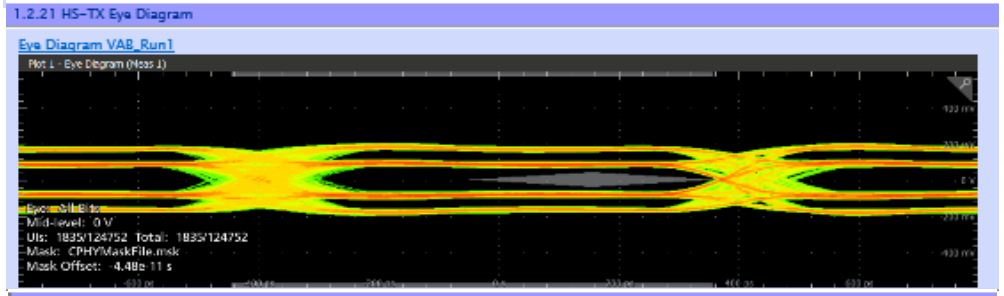
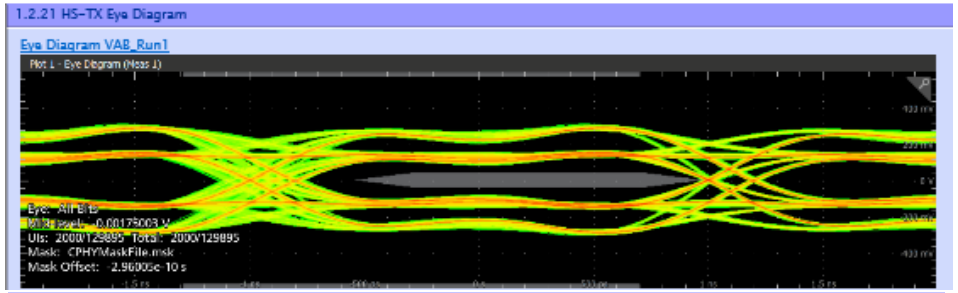
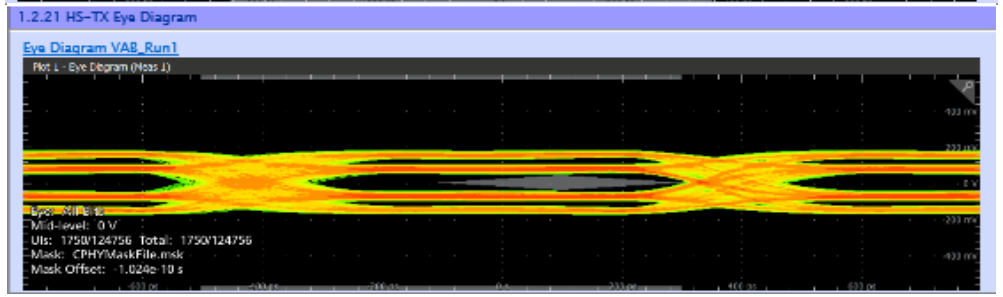
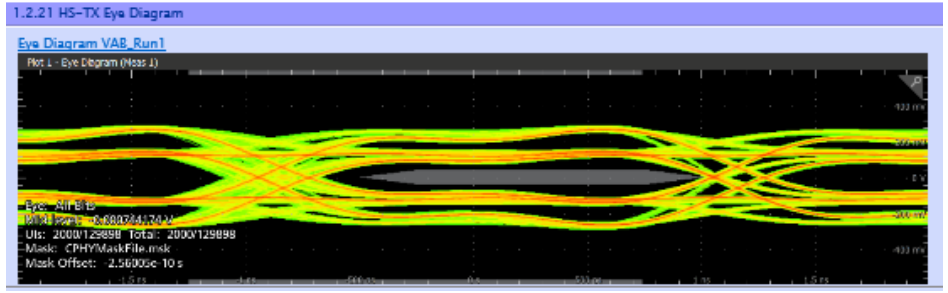
- Applicable for all Symbol rates.
  1. Hexagonal Mask shape < 1.0 Gsps
  2. Diamond Mask shape > 1.0 Gsps
- Measured at the end of reference channel
  1. Standard: Normative
  2. Long: Informative
  3. Short: Informative
- Pattern: Continuous HS data (Recommended) or Data from multiple bursts.
(PRBS9 recommended Pattern for Data)
- Measurement using random test pattern of 3 million UI



Symbol Rate Based Masks: Hexagonal and Diamond

Tx Test: HS-Tx Eye Diagram

C-PHY V2.0 TRANSMITTER EYE DIAGRAM: MASKS BASED ON SYMBOL RATE

	Diamond Mask Shape > 1.0 Gsps	Hexagonal Mask Shape < 1.0 Gsps
Short		
Standard		
Long		

Two different mask shapes as seen in an oscilloscope

Tx Test: HS-Tx Eye diagram

C-PHY V2.0 : CTLE

Test ID 1.2.21

- Applicable for above below data rates.

	Reference Channel			
Description	**Short**	**Standard**	**Long**	**Units**
USE CTLE, on operating above the Symbol Rates	**4.5**	**3.5**	**2.3**	**Gsps**

- Measured at the end of reference channel
  1. Standard: Normative; To be supported by Transmitter and Receiver
  2. Long: Informative
  3. Short: Informative
- Pattern: Continuous HS data (Recommended) or Data from multiple bursts into the reference channels with a termination of 100Ω
- Measurement using random test pattern of 3 million UI

Solutions/Applications from Tektronix

Conformance Requirements

M-PHY V5.0/M-PHY V4.0, D-PHY V2.1, AND C-PHY V2.0

M-PHY G1-G5*

Gear	23GHz	25Ghz	33GHz
G1-G3			
G4			
G5			

* 70K DX/SX Oscilloscopes only

D-PHY

Data Rate	4GHz	6GHz	8GHz	10GHz	>13*GHz
1.5Gbps					
2.5Gbps					
4.0 Gbps					
4.5Gbps					

C-PHY

Data Rate	2.5 GHz	4GHz	6GHz	8GHz	10GHz	16GHz	>20*GHz
1.0 Gsps							
2.5 Gsps							
4.0 Gsps							
6.0 Gsps							
8.0 Gsps							

Conformance

Debug

- 70K DX/SX Oscilloscopes
- Up to 10GHz on MSO6/6B

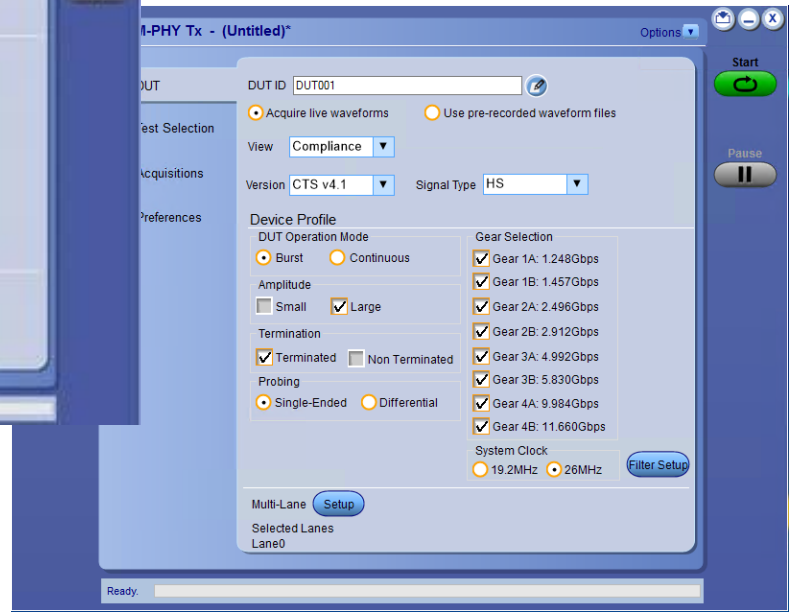
Tx conformance for three standards of MIPI: M-PHY, D-PHY and C-PHY

Tektronix Applications for C-PHY D-PHY & M-PHY

TEKEXPRESS FOR AUTOMATION OF C-PHY, D-PHY, AND M-PHY

C-PHY Tx

D-PHY Tx

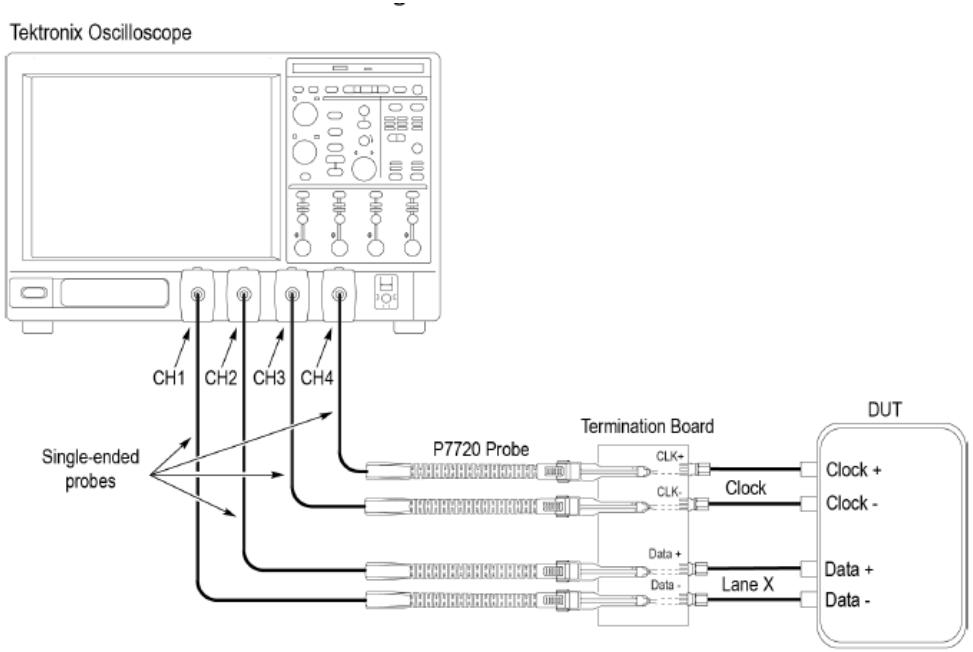


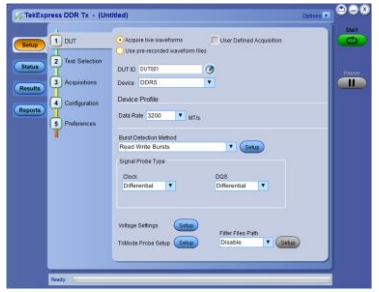
M-PHY Tx

- Automates the testing
- **Covers all Measurements** of C-PHY/D-PHY and M-PHY
- Supports RTB
- Includes filter files for Channels
- Waveform post processing for LP-HS
- Capable of running multiple times for Characterization labs

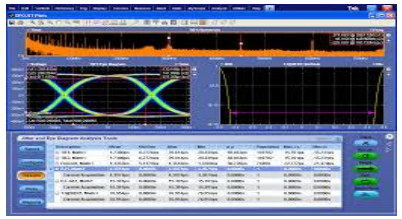
Setup for Validation/Debug

TYPICAL TEST SETUP E.G., D-PHY V2.1





+



+

+

+

RTB

Setup consists of Oscilloscope + Probes + Software on Scope + RTB

Optimized Solution Offering for C-PHY, D-PHY & M-PHY

SUMMARY

SYSTEM LEVEL TX			
Group	**D-PHY v2.1**	**C-PHY v2.0**	**M-PHY Gear5**
HW	Scope* ≥13GHz 70K DX/SX	Scope* ≥20GHz 70K DX/SX	Scope ≥33GHz DX/SX
	P7700 Series Probes (4)	P7700 Series Probes (3)	P7600 Series Probes (2)
	P7700 Probe Tips P77STFLXA(4)	P7700 Probe Tips P77STFLXA(3)	P7700 Series Probe (2)
	RTB	RTB	
SW	TekExpress DPHY21	TekExpress CPHY20	MPHY50
	DPOJET	DPOJET	DPOJET
	SR-DPHY(Optional)[1]	SDLA	SDLA

C-PHY and D-PHY solutions are also supported on MSO6B

[1] Highly recommended but not mandatory

Summary

C-PHY, D-PHY AND M-PHY VALIDATION

- Challenging with various modes of signaling involved
- Validation of Physical layer and Protocol layer
- Reference channels are part of the specification
- Equalization required in C-PHY and M-PHY
- Complete TX solution from Tektronix

Validation challenges can be overcome by using the right tools.

TEKTRONIX
INNOVATION FORUM
2022
Accelerating Progress

THANK YOU

Ravi Malladi, Product Manager – MIPI
Gajendra K Patro, Product Line Solutions Engineer