TEKTRONIX
INNOVATION FORUM
2023
Engineering the Future

PCIe 7.0 Introduction

PCIe 6.0 Anritsu/Tektronix Solution

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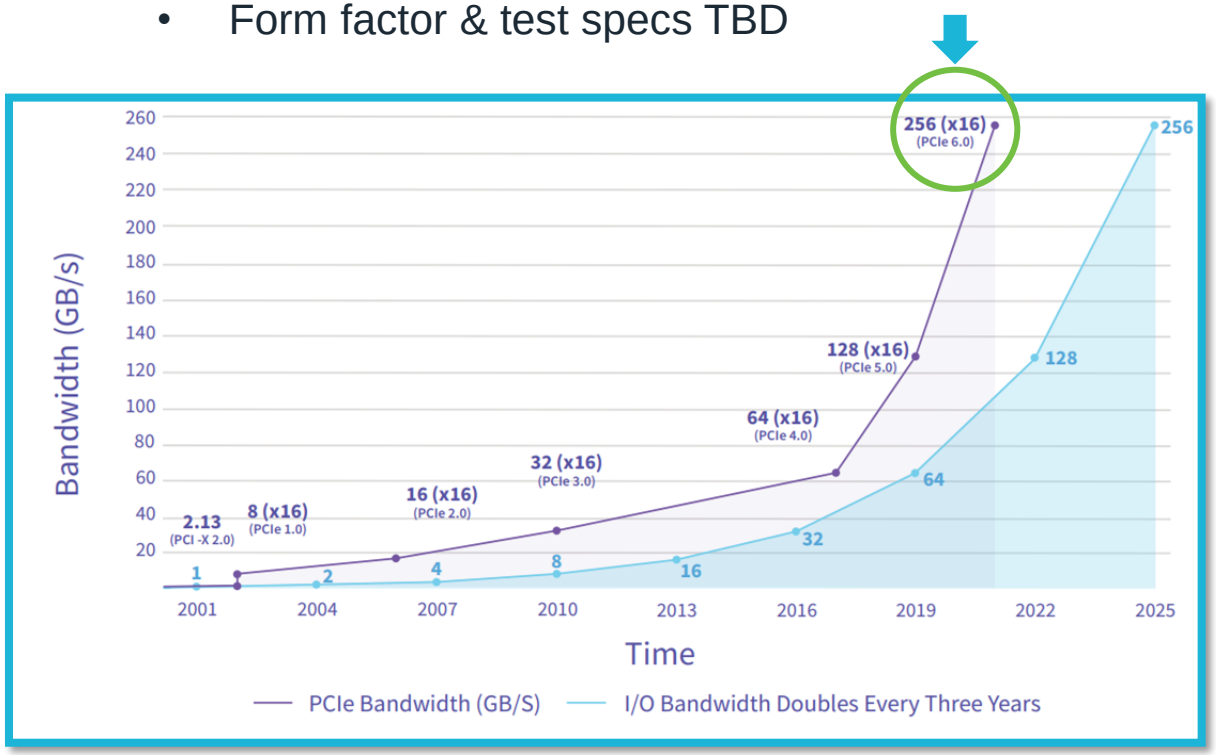
High Speed Signals Symposium
Israel 2023

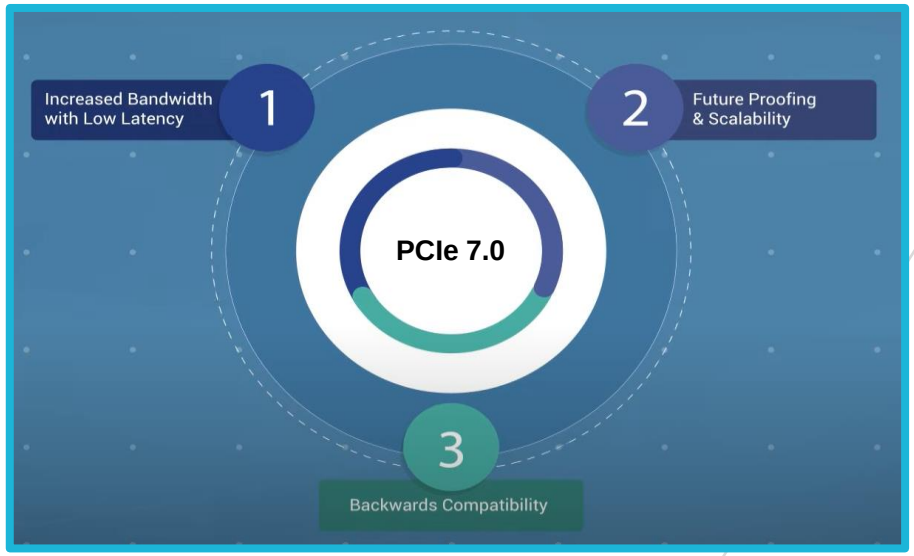
PCIe 7.0 Introduction

PCI Express Evolution

- !!! PCIe 7.0 Development Underway !!!
  - HPC & AI/ML applications
  - Increasing network bandwidths
- Specification Status
  - Base specification expected 2025
  - Form factor & test specs TBD



	Bit Rate / Lane	Link BW	Lane BW	x16 bi BW
PCIe 1.x	2.5 GT/s	2.0 Gb/s	250 MB/s	8 GB/s
PCIe 2.x	5.0 GT/s	4.0 Gb/s	500 MB/s	16 GB/s
PCIe 3.x	8.0 GT/s	8.0 Gb/s	~1 GB/s	32 GB/s
PCIe 4.x	16.0 GT/s	16.0 Gb/s	~2 GB/s	64 GB/s
PCIe 5.x	32.0 GT/s	32.0 Gb/s	~4 GB/s	128 GB/s
PCIe 6.x	64.0 GT/s	64.0 Gb/s	~8 GB/s	256 GB/s
PCIe 7.x	128.0 GT/s	128.0 Gb/s	~16 GB/s	512 GB/s



PCIe 7.0 Specification Snapshot

- **PCIe 7.0 Base Specification – Rev 0.5 under development**
  - Describes chip-level behavior on all levels of the stack
- **PCIe 7.0 CEM Specification – Pathfinding to start 2024**
  - Card electro-mechanical (CEM) defines system and Add-in Card level
- **PCIe 6.0 PHY Test Specification – Rev 0.7 under development**
  - Describes electrical compliance tests for Tx, Rx LEQ, & PLL Bandwidth

PCIe 5.0 to 7.0 Base Specification Updates

	PCIe 5.0	PCIe 6.0	PCIe 7.0 (TBD)
Data Rate	32 GT/s	64 GT/s (PAM4)	128 GT/s (PAM4)
Add-in Card Loss	9.5dB @ 16GHz	8.5dB @ 16GHz	~9dB @ 32GHz
Rx Test (Channel Loss)	- (34 to 37) dB @ 16GHz	- (30 to 33) dB @ 16GHz	- (36 to 40) dB @ 32GHz
Reference CTLE	4 Poles; 2 Zero; DC Gain Range (-5 to -15) dB	6 Poles; 3 Zero; DC Gain Range (-5 to -15) dB	6 Poles; 3 Zero; DC Gain Range (-5 to -15) dB
Reference DFE	3-Taps	16-Taps	ADC Architecture
Reference FFE	N/A	N/A	Expected
Eye Width (Rx Test)	9.375 ps	3.125 ps (top eye)	~1.5 ps (top eye)
Eye Height (Rx Test)	15 mV	6 mV (top eye)	~3 mV (top eye)
Lane Margining	Required timing/voltage	Required timing/voltage	Required timing/voltage
Refclk Jitter Limits	<= 150 fs	<=100 fs	<=67 fs

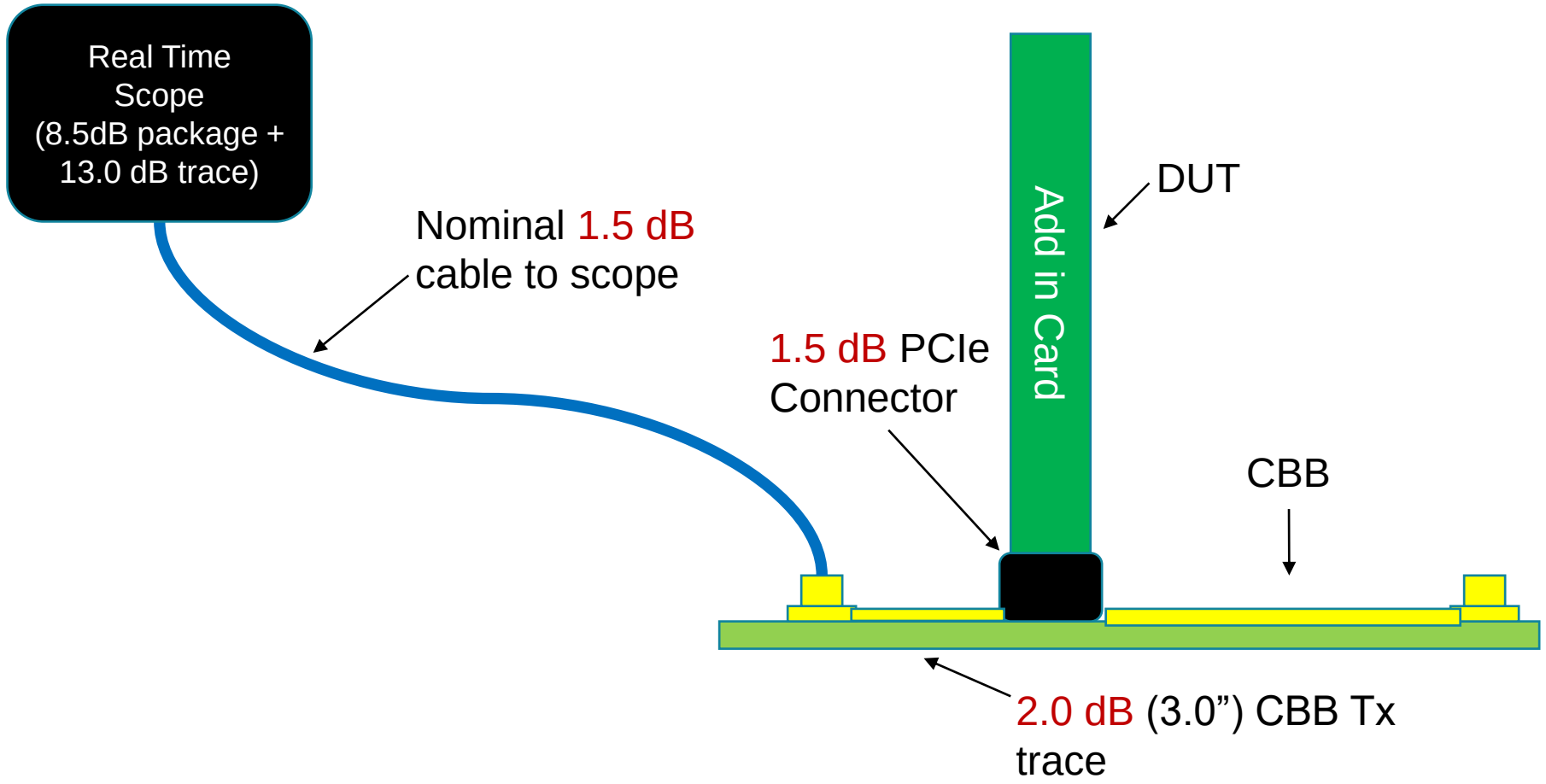
Increase in complexity of PCIe specifications

PCIe 5.0 Background

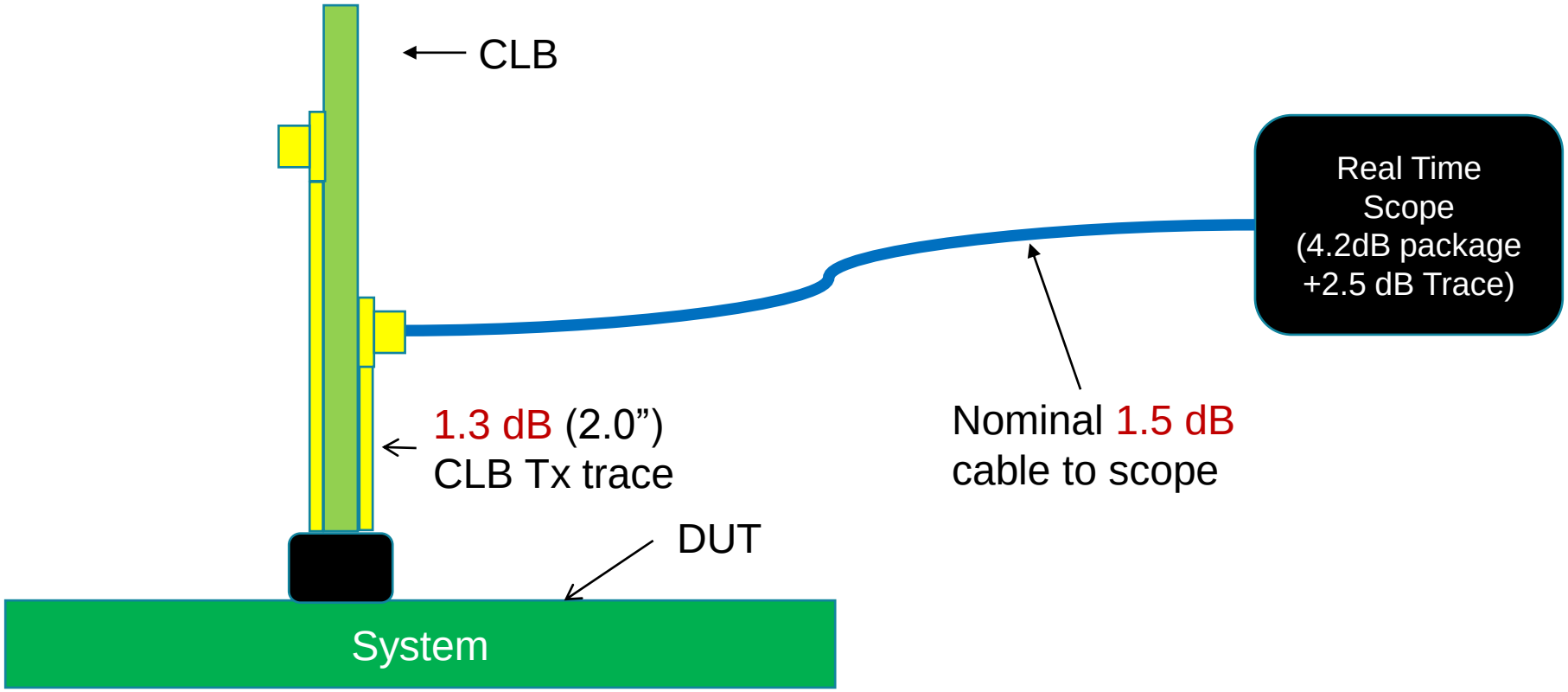
PCIe® 5.0 Electrical Tests

- **Transmitter (Tx) Signal Quality Test at 32GT/s**
  - End of channel eye diagram (eye width & eye height) @ BER E-12
- **Tx Preset Equalization Test at 32GT/s**
  - Measures voltage levels for Preset 0 to Preset 10 (new AC method)
- **Tx Uncorrelated Jitter at 32GT/s (Add-in Card)**
  - Intrinsic jitter of the Tx after removing channel impact – removed for systems
- **Tx Pulse Width Jitter (PWJ) at 32GT/s (Add-in Card)**
  - Measure of the variation between adjacent rising & falling edges – removed for systems
- **Tx PLL Bandwidth (Add-in Cards)**
  - Verifies an Add-in Cards Tx PLL bandwidth and peaking
- **Link Equalization at 32GT/s**
  - Tx starts with correct preset requested through protocol
  - Tx responds to protocol changes and adjusts
  - Receiver (Rx) correctly adjusts the link Tx and meets error criteria with a stressed signal

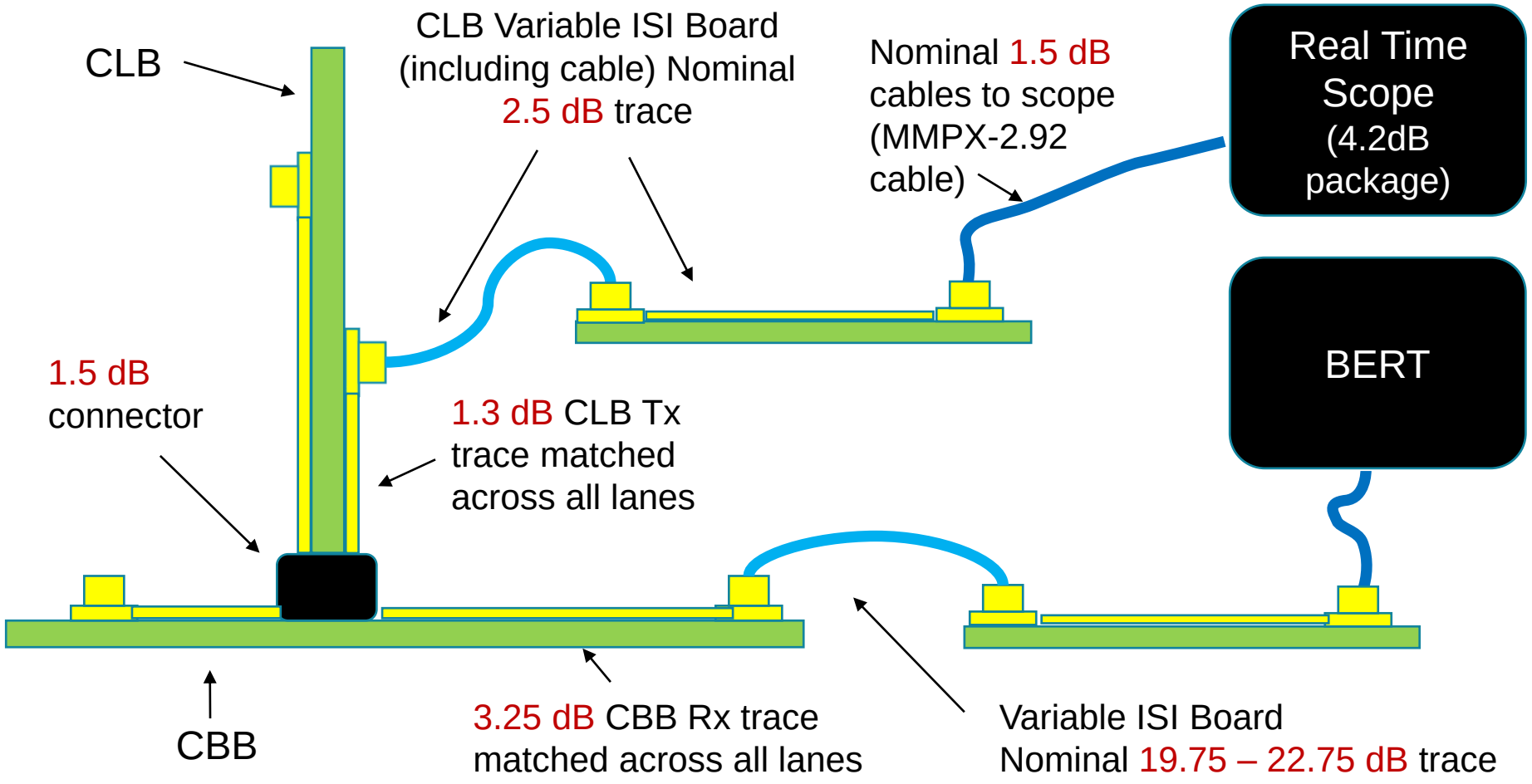
32 GT/s Signal Quality Test: Add-in Card



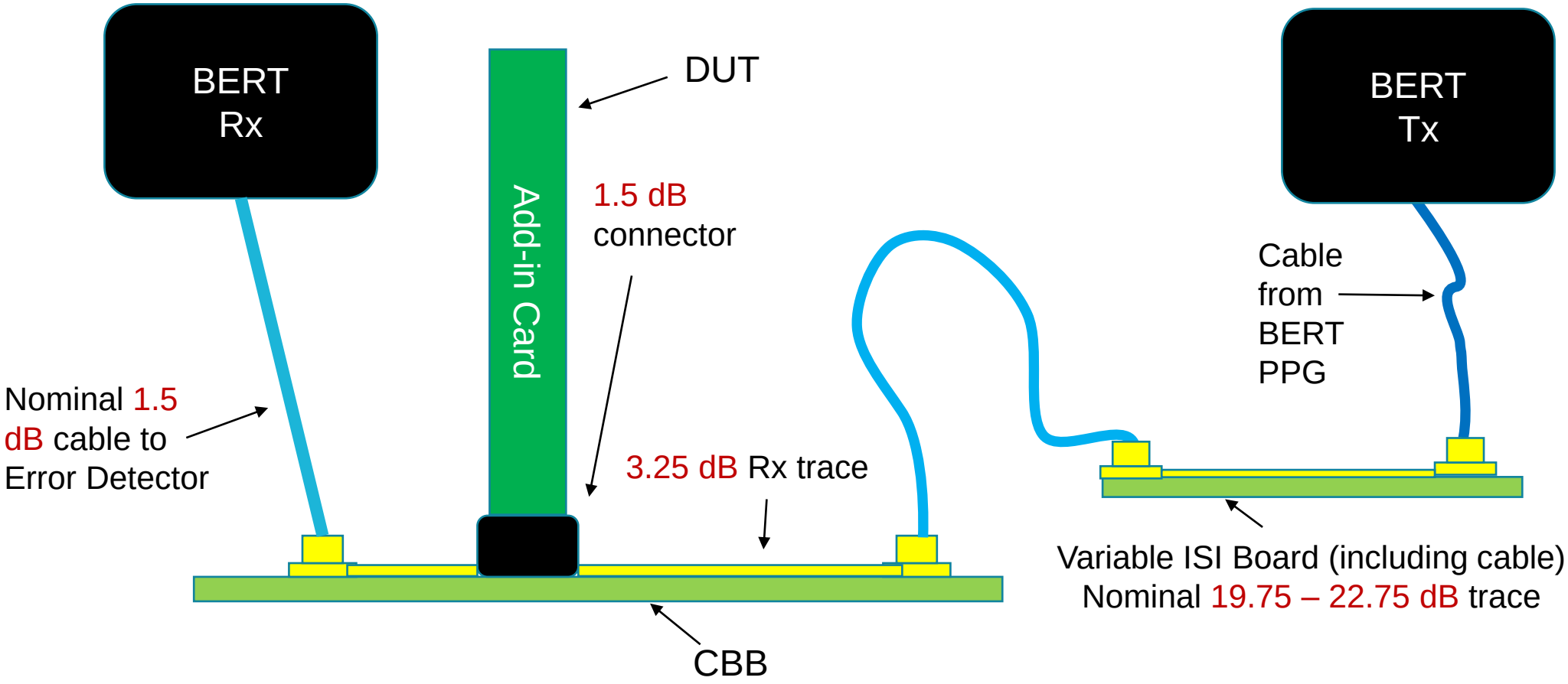
32 GT/s Signal Quality Test: System



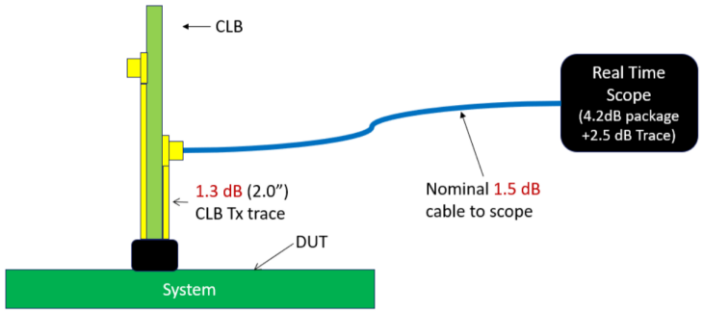
32 GT/s Rx Calibration: Add-in Card



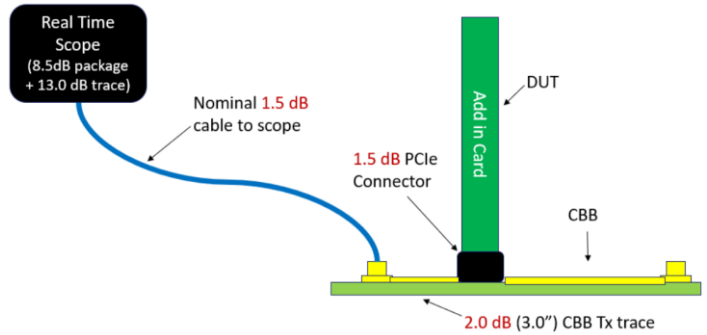
32 GT/s Rx Link Equalization: Add-in Card

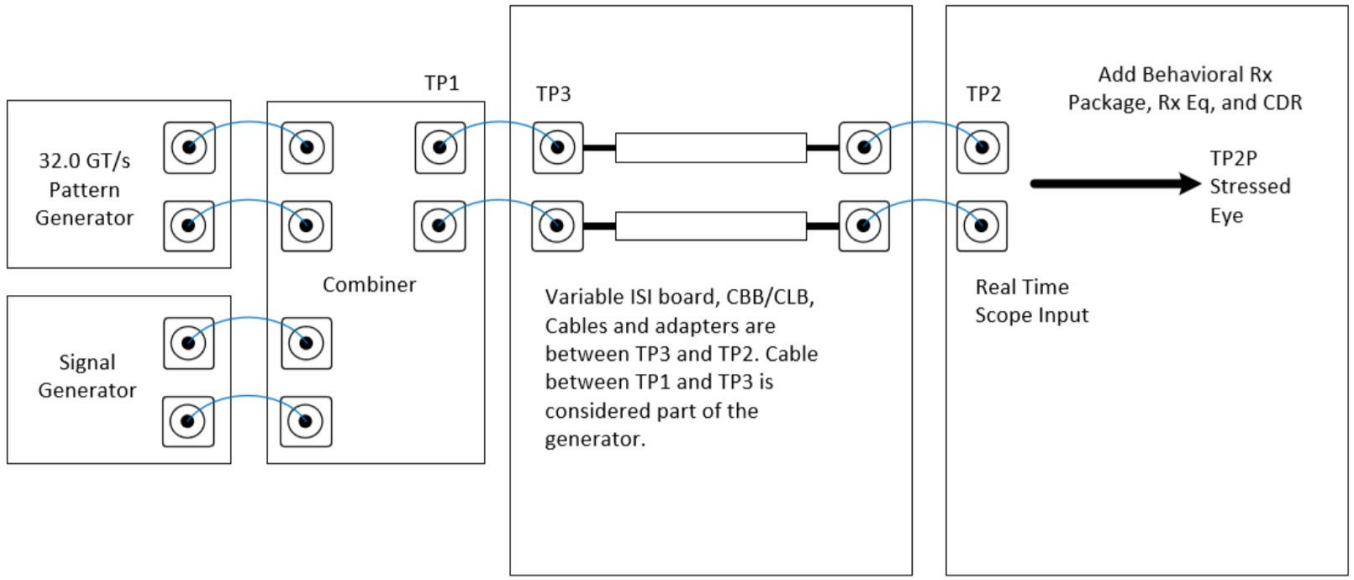


Test Fixture Characterization at 32 GT/s



- **Transmitter**
  - Signal Quality (EW/EH) @ TP2P
  - System: 9.5dB added
    - CLB, cable, **add-in card trace**, NRC package
  - Add-in Card: 26.5dB added
    - CBB, cable, **system trace**, RC package
  - VNA to identify **embedded trace loss**
    - Trace & package





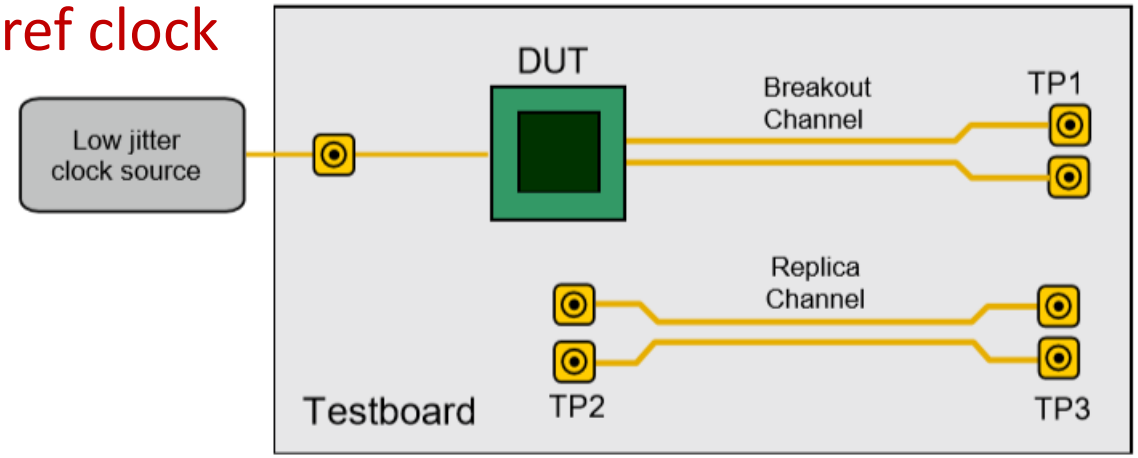
- **Receiver**
  - Stressed Eye Calibration @ TP2P
  - Loss Range: 34dB – 37dB
    - TP3 to TP2P
  - Embedded NRC or RC Package
  - System: RC Package
  - VNA to identify **Variable ISI Pair**
    - Correct **Location** of **CEM Connector**

PCIe 5.0 PHY Test Spec Appendix A & B

PCIe 6.0 Tx Validation

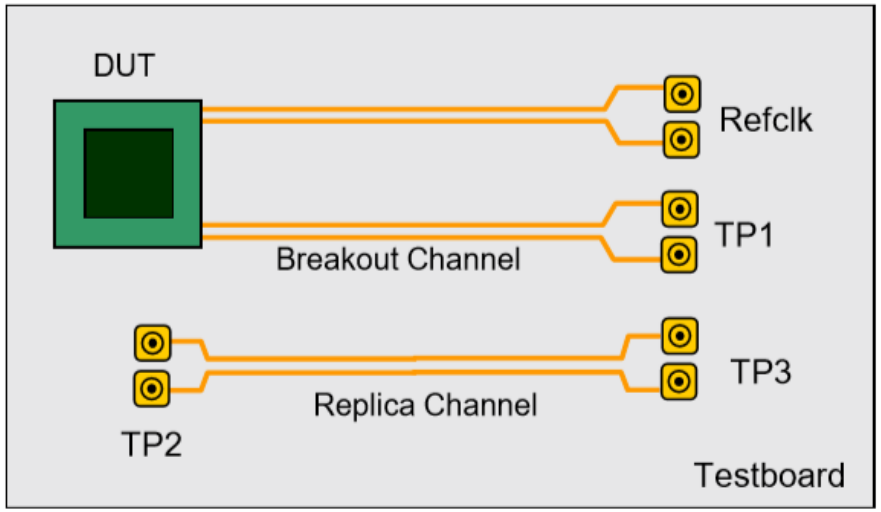
Base Tx Signal Access & Test Points

Non embedded ref clock



A low jitter Refclk source is used when the silicon supports using an external reference clock

Embedded ref clock

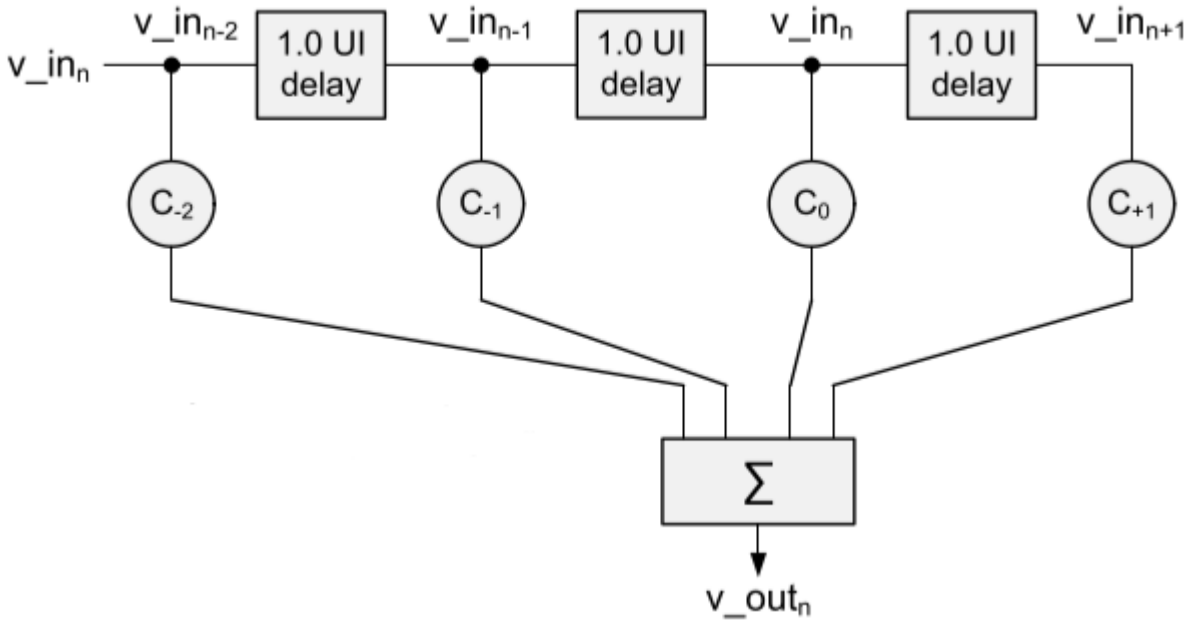


Transmitter using an embedded reference clock

Extending 6.0 Base Tx to CEM

TX Test	Pattern	CEM	Notes
SNDR	Compliance	AIC & System?	Signal Noise Distortion Ratio
Voltage Differential Peak-to-Peak	Compliance	N/A	Measured with 64 level 3s & 64 level 0s
Transmit Equalization	Compliance	AIC & System	Q0-Q10 (PAM4) with AC step method
Tx Equalization Boost	Compliance	N/A	Q10 (full swing) & Q4 (reduced swing)
EIEOS Min Voltage Swing	Compliance	N/A	Include package loss impact
Ratio Level Mismatch	Compliance	AIC & System?	PAM4 measurement only
Uncorrelated Tj	52UI Jitter Measurement	AIC	Jitter computed on each unique transition
Uncorrelated Dj	52UI Jitter Measurement	AIC	Jitter computed on each unique transition
Uncorrelated Rj	52UI Jitter Measurement	AIC	Informative
Pulse Width Jitter Tj	High Swing Toggle	AIC	0303 level patten; noise comp included
Pulse Width Jitter Dj_dd	High Swing Toggle	AIC	0303 level patten; noise comp included
Pulse Width Jitter Rj	High Swing Toggle	AIC	Informative
PS21	Compliance	N/A	Pseudo package loss

Transmitter Equalization Updates



Preset #	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q0	0.0 ±0.5 dB	0.0 ±0.5 dB	0.0 ±0.5 dB	0.000	0.000	0.000	1.000	1.000	1.000	1.000
Q1	0.0 ±0.5 dB	1.6 ±0.5 dB	0.0 ±0.5 dB	0.000	-0.083	0.000	0.834	0.834	1.000	0.834
Q2	0.0 ±0.5 dB	3.5 ±0.5 dB	0.0 ±0.5 dB	0.000	-0.167	0.000	0.666	0.666	1.000	0.666
Q3	0.0 ±0.5 dB	0.0 ±0.5 dB	-1.6 ±0.5 dB	0.000	0.000	-0.083	1.000	0.834	0.834	0.834
Q4	0.0 ±0.5 dB	0.0 ±0.5 dB	-3.5 ±0.5 dB	0.000	0.000	-0.167	1.000	0.666	0.666	0.666
Q5	-1.3 ±0.5 dB	4.7 ±1.0 dB	0.0 ±0.5 dB	0.042	-0.208	0.000	0.584	0.584	1.000	0.500
Q6	-1.6 ±0.5 dB	3.5 ±0.5 dB	-3.5 ±0.5 dB	0.042	-0.125	-0.125	0.750	0.500	0.750	0.416
Q7	-2.9 ±0.5 dB	4.7 ±1.0 dB	0.0 ±0.5 dB	0.083	-0.208	0.000	0.584	0.584	1.000	0.418
Q8	-3.5 ±0.5 dB	6.0 ±1.0 dB	0.0 ±0.5 dB	0.083	-0.250	0.000	0.500	0.500	1.000	0.334
Q9	-4.4 ±1.0 dB	6.9 ±1.0 dB	-1.6 ±0.5 dB	0.083	-0.250	-0.042	0.500	0.416	0.916	0.250
Q10	0.0 ±0.5 dB	0.0 ±0.5 dB	Note 2	0.000	0.000	Note 2	1.000	Note 2	Note 2	Note 2

- **Cursor Expansion:** 2nd Precursor Added
  - 2 pre-cursors
  - 1 post-cursor
- **Presets:** Q0 to Q10
  - Heavier pre-cursor weighting
  - Numerous optimal presets for Rx Calibration

- **Measurement Method:** AC Fit Method
  - Step response captured
    - *Equalized & Non-Equalized*
  - Cursors applied to Non-Equalized step
  - Minimized Mean Square Error (MSE)

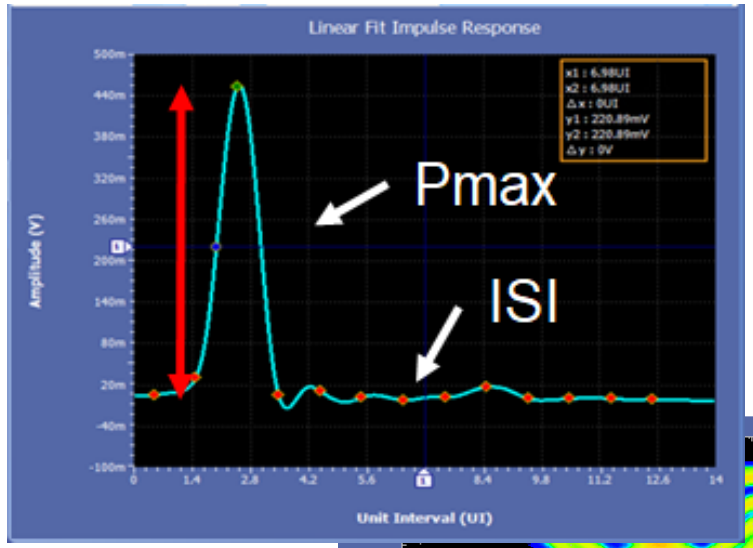
Signal to Noise Distortion Ration (SNDR)

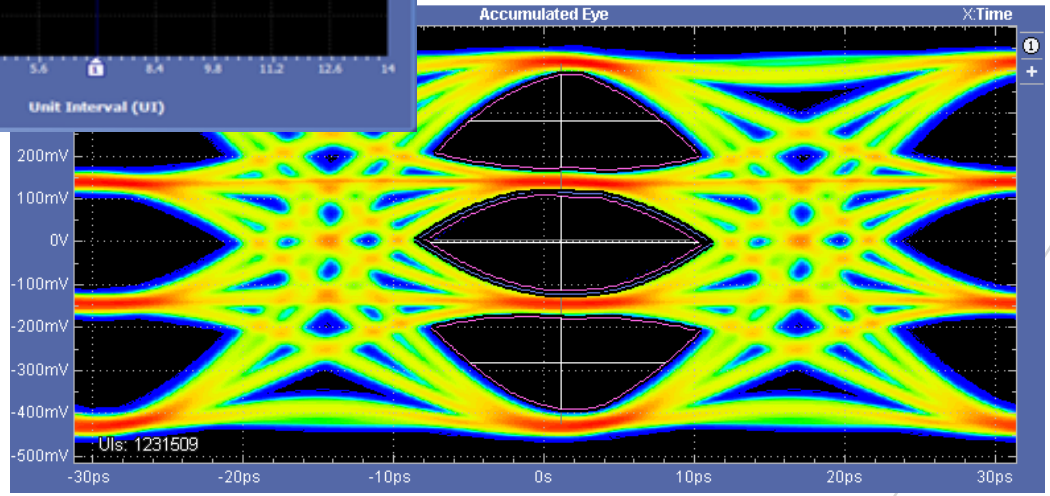
$$SNDR = 10\log_{10}\left(\frac{p_{max}^2}{\sigma_e^2 + \sigma_n^2}\right) \text{ dB}$$

Signal power

Non-compensable distortion

Noise



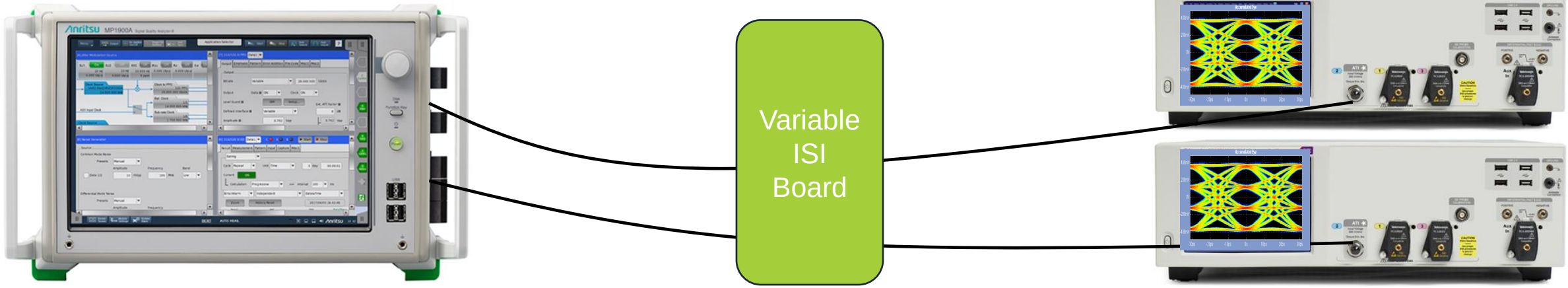


p_{max} = peak of linear fit pulse
σ_e = standard deviation of error waveform
σ_n = standard deviation of noise

PCIe 6.0 SNDR Requirements

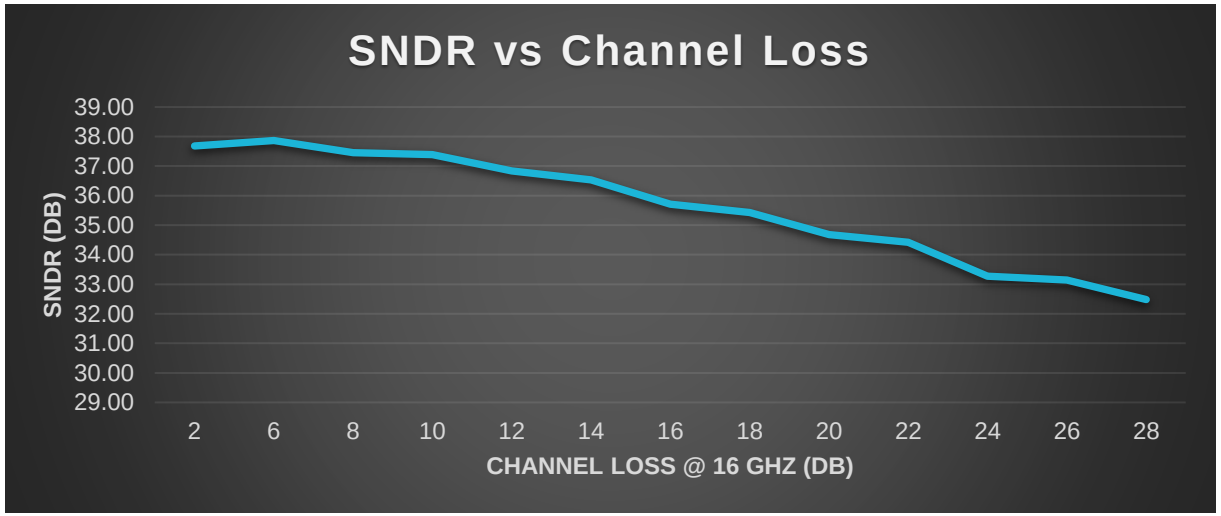
- Pattern: 6.0 compliance pattern (SSC considered for SRIS)
- Tx Equalization: Q0 (C-2 = C-1 = C+1 = 0.0)
- RT Scope waveform capture
  - BW of 50GHz (minimum)
  - Record Length: min of 250 pattern repetitions
  - Filtering: 4th order Bessel-Thomson (3dB roll-off from DC at 33GHz)
- Sigma E
  - Pulse Length = Np = 600UI
  - Pulse Delay = Dp = 4
  - 32 points/UI (resampling)
  - PRBS portion of compliance pattern only
- Clock Recovery Applied (DSP implementation not explicitly defined)
- Sigma N
  - 61st UI of 64 UI run for each PAM4 voltage level considered
  - Eight evenly spaced points within 61st UI averaged
  - Instrument Noise compensation

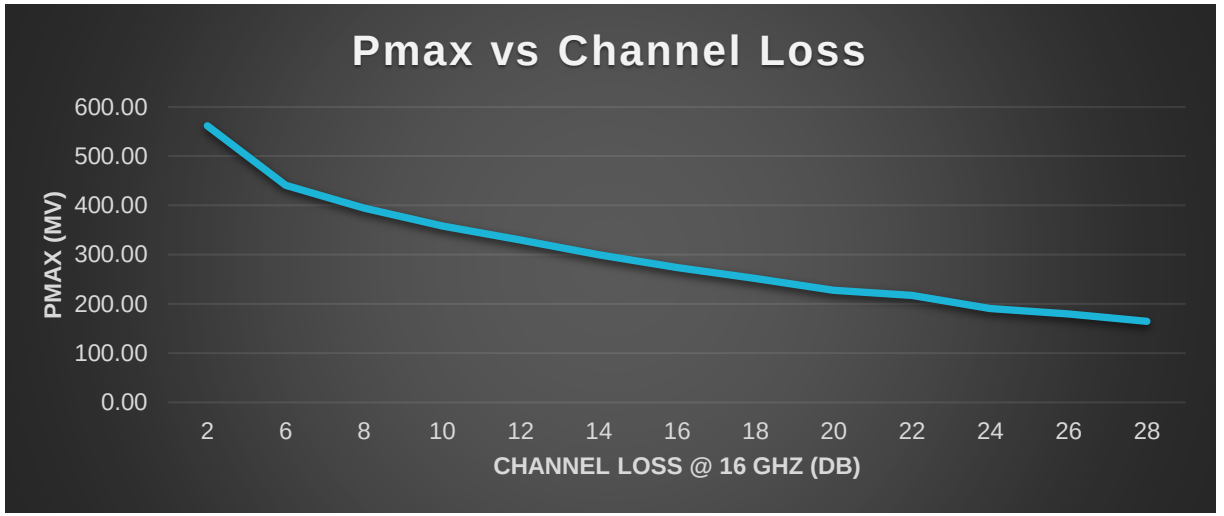
64 GT/s SNDR Study

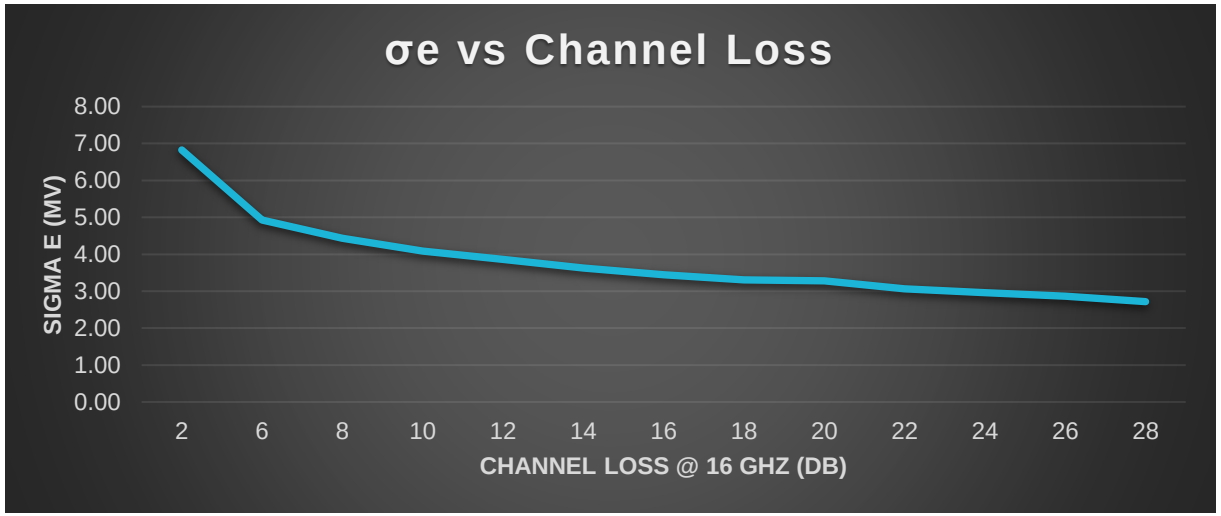


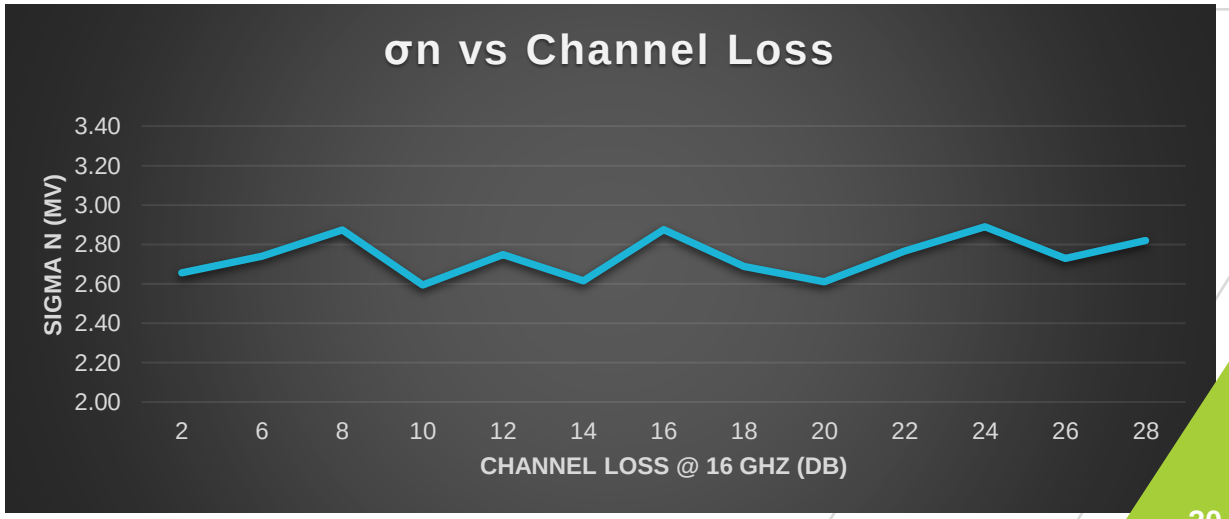
Channel Loss	SSC	Scope BW	Pattern	Np	Scope Noise Removal	SNDR	Pmax	Sigma E	Sigma N
1.5 dB (cable only)	On	33 GHz BT	Gen6 Compliance	600	3.8	40.7	369.6	3.31	0.84
"	Off	"	"	"	"	40.0	367.0	3.47	1.18
7.43 dB (4" Replica)	On	"	"	"	"	39.6	239.4	2.18	1.25
"	Off	"	"	"	"	40.0	239.4	2.26	0.79
10.79 dB (8" Replica)	On	"	"	"	"	39.4	195.1	1.88	0.91
"	Off	"	"	"	"	39.8	195.1	1.95	0.41
14.33 dB (12" Replica)	On	"	"	"	"	39.0	162.0	1.71	0.62
"	Off	"	"	"	"	39.0	161.9	1.76	0.41

64 GT/s CEM SNDR Study





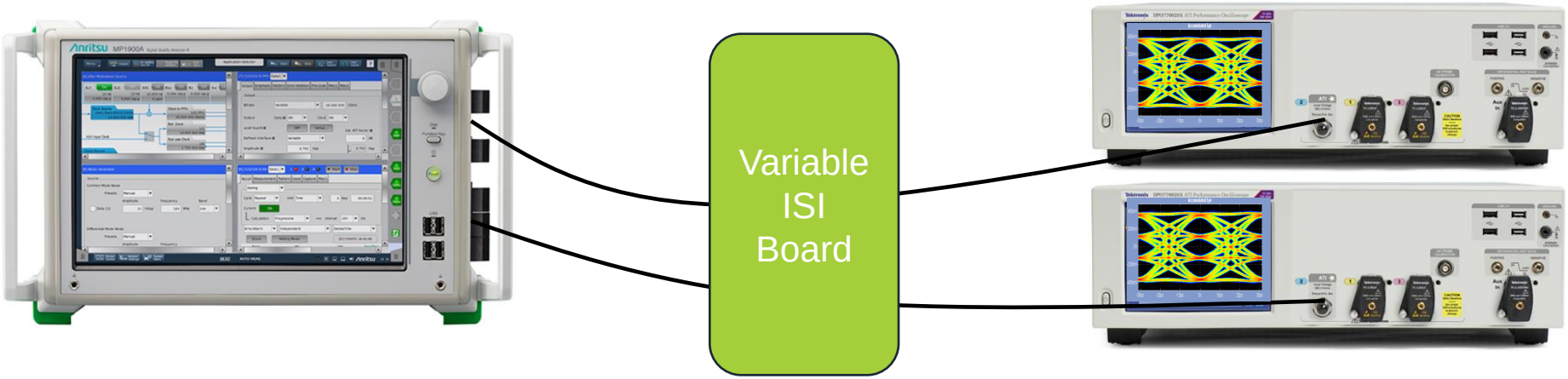


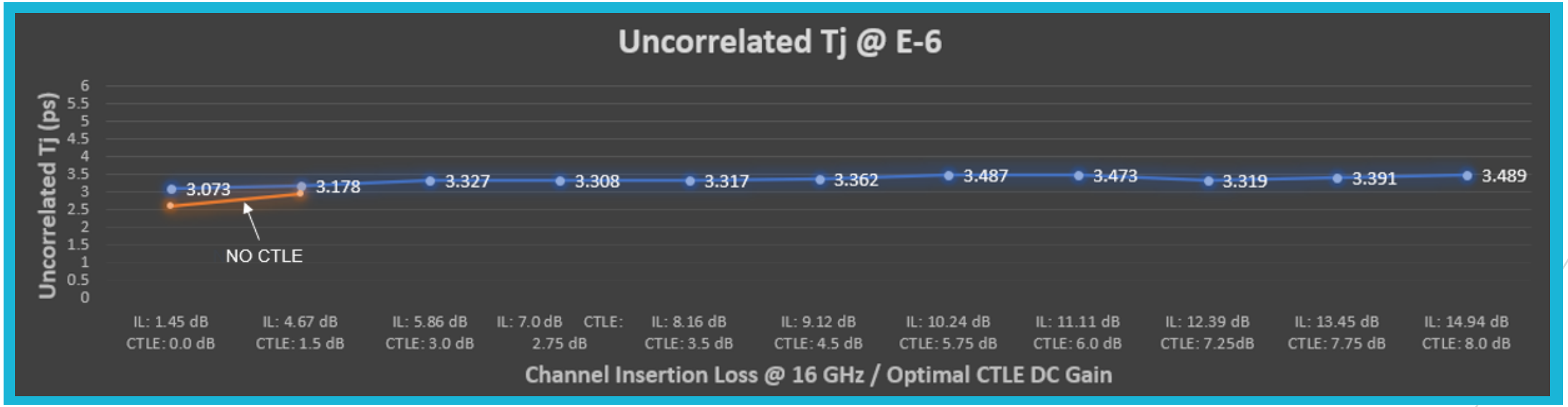


PCIe 6.0 Uncorrelated Jitter Requirements

- Pattern: 52UI Jitter Measurement Pattern
  - Four instances of all 12 PAM4 transitions & DC balancing bits
- Tx Equalization: Q0 (C-2 = C-1 = C+1 = 0.0)
- RT Scope waveform capture
  - BW of 50GHz (minimum)
  - Record Length: min of 2E6 UI (37.5 UI per unique edge)
  - Filtering: 4th order Bessel-Thomson (3dB roll-off from DC at 33GHz)
- Jitter measured on all 48 edges separately and then averaged
- Select CTLE or No CTLE resulting in lowest Rj
- Scope noise removed separately for each transition type

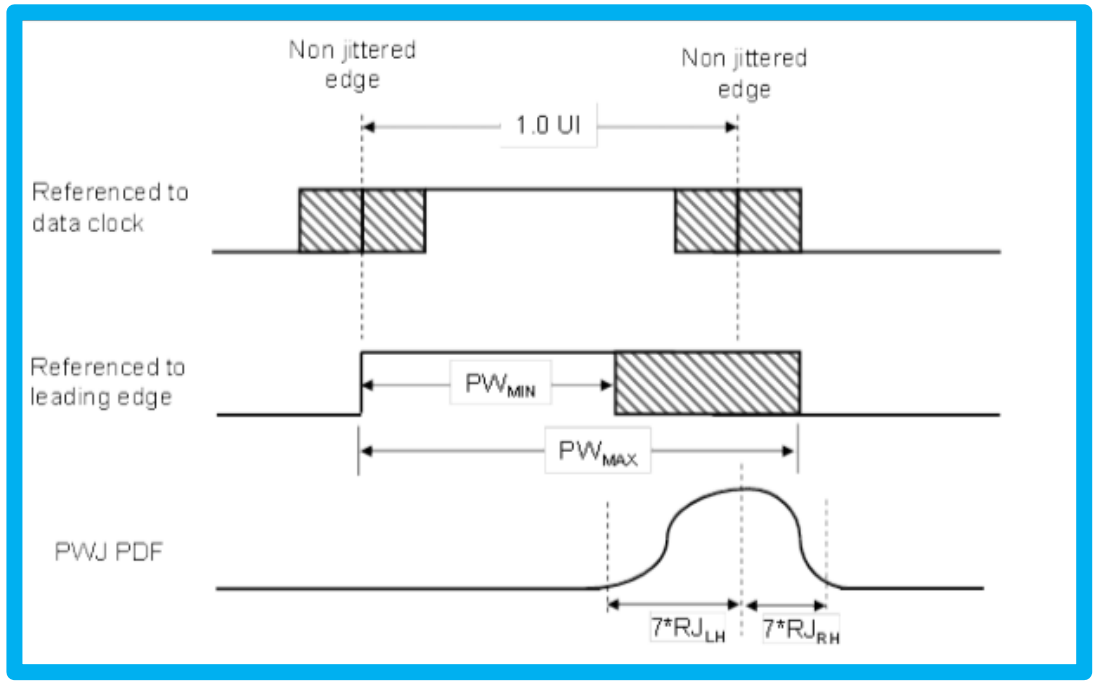
64 GT/s Uncorrelated Jitter Study





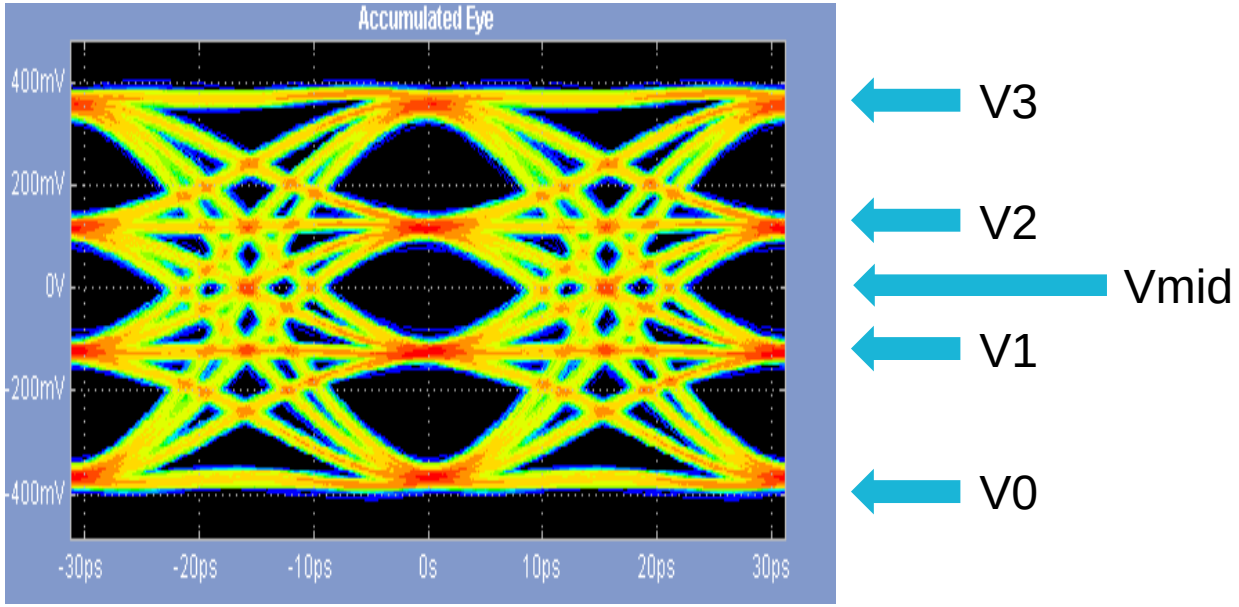
PCIe 6.0 Pulse Width Jitter

- High Low “0303” Pattern
- Scope BW 50 GHz
- 4th Order 33GHz BT filter
- Optimize ADC (max signal)
- CTLE 5 to 15 dB allowed
- Capture Instrument noise



- Tektronix PAMJET
- No ISI (pattern ensures)
- Edge to Edge (pulse width)
- Even Odd Jitter included
- Separate PDFs & Medians
- Total PWJ < 4 ps @ E-6

Tx Ratio Level Mismatch (RLM)



•RLM Equation

$$V_{mid} = (V_0 + V_3) \mid 2$$

$$ES_1 = (V_1 - V_{mid}) \mid (V_0 - V_{mid})$$

$$ES_2 = (V_2 - V_{mid}) \mid (V_3 - V_{mid})$$

$$R_{LM} = min((3 \times ES_1), (3 \times ES_2), (2 - 3 \times ES_1), (2 - 3 \times ES_2))$$

•Nominal Values

- V3 = 400 mV
- V2 = 133 mV
- Vmid = 0 mV
- V1 = -133 mV
- V0 = -400 mV

•ES1&ES2

- ES1 = (-133 mV – 0 mV) / (-400 mV – 0 mV) = ~1/3
- ES2 =(133 mV – 0 mV) / (400 mV – 0 mV) = ~1/3
-

•RLM

- RLM = min[(3 * 1/3) , (3 * 1/3), (2 – 3 * 1/3) , (2 – 3 * 1/3)]
- RLM = min[1, 1, 1, 1] = 100%

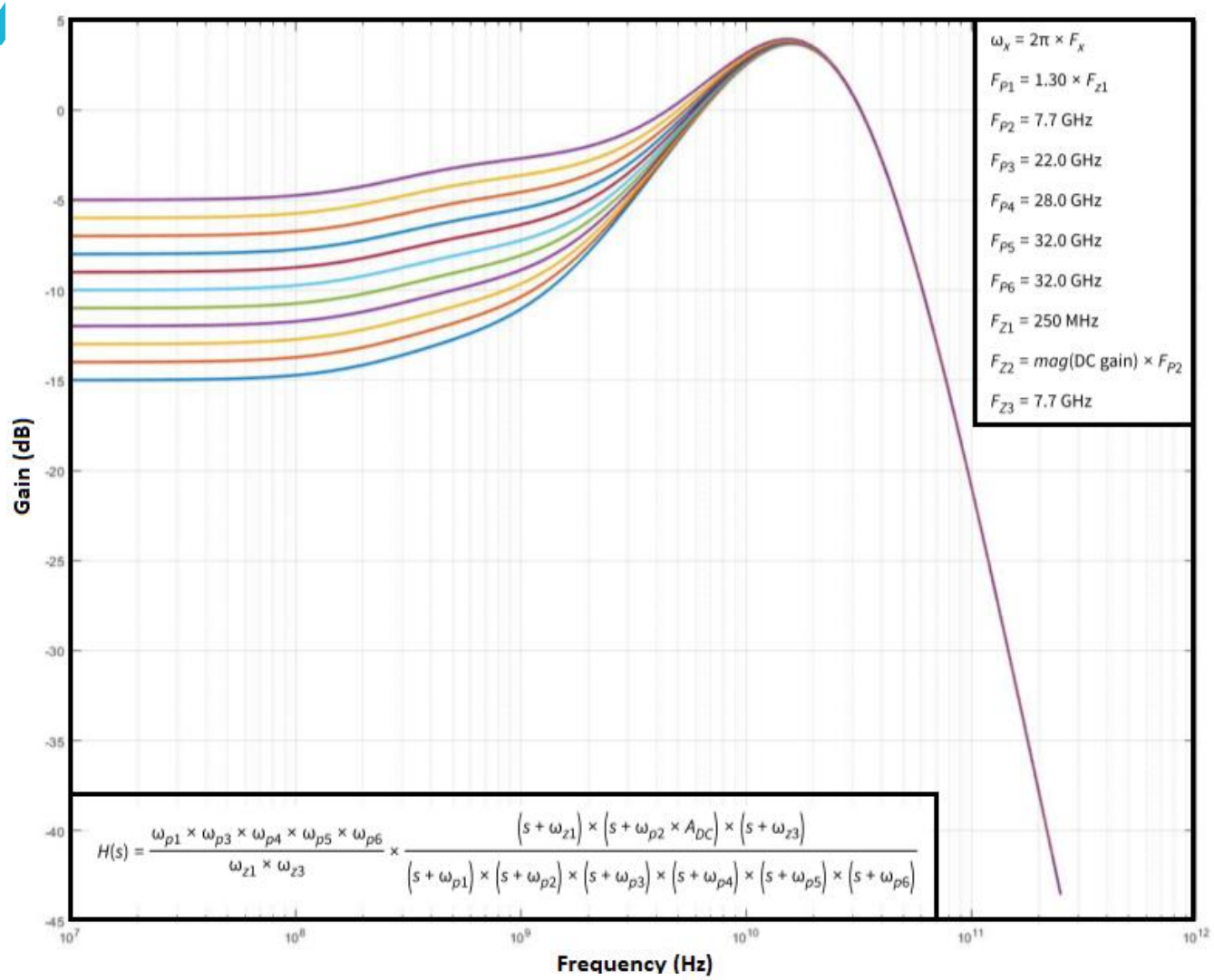
Ideal RLM Result

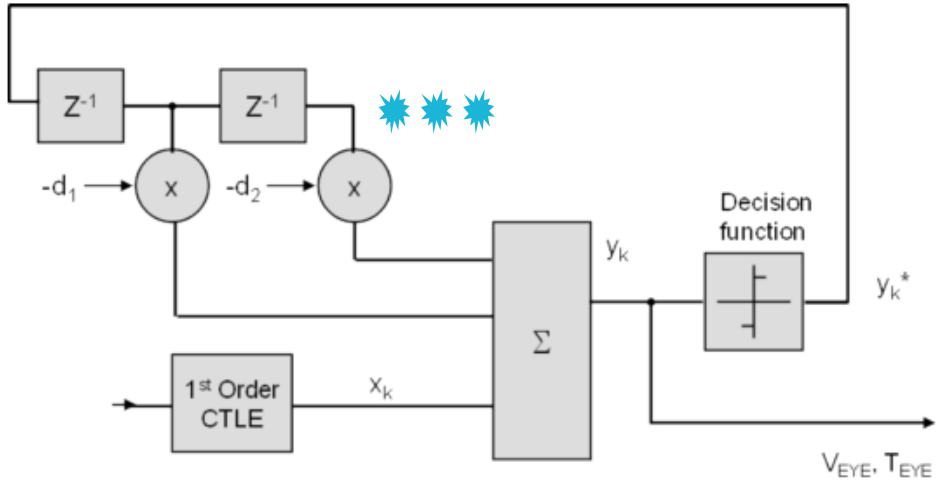
Applying CTLE or De-embedding

Measurement	Pattern	De-embedding	CTLE
Uncorrelated Jitter	2.5 to 16 GT/s: Compliance 32 & 64 GT/s: Jitter pattern (1010)	2.5 to 8 GT/s 16 GT/s (de-embed or CTLE) – pick lowest jitter result	16 GT/s (-12dB) 32 & 64 GT/s (-5 to -15dB)
Pulse Width Jitter	2.5 to 16 GT/s: Compliance 32 & 64 GT/s: Jitter pattern (1010)	2.5 to 8 GT/s 16 GT/s (de-embed or CTLE) – pick lowest jitter result	16 GT/s (-12dB) 32 & 64 GT/s (-5 to -15dB)
Data Dependent Jitter	Compliance Pattern	Yes	No
SNDR	64 GT/s Compliance Pattern	No	No
RLM (level separation)	64 GT/s Compliance Pattern	No	No
PS21 (package loss)	Compliance Pattern	Yes	No
EIEOS	FS (P10/Q10 Compliance Pattern) RS (P1/Q4 Compliance Pattern)	Yes	No
AC Common Mode	Compliance Pattern	No	No
Voltage Swing	Compliance Pattern	No	No

PCIe 6.0 Rx Validation

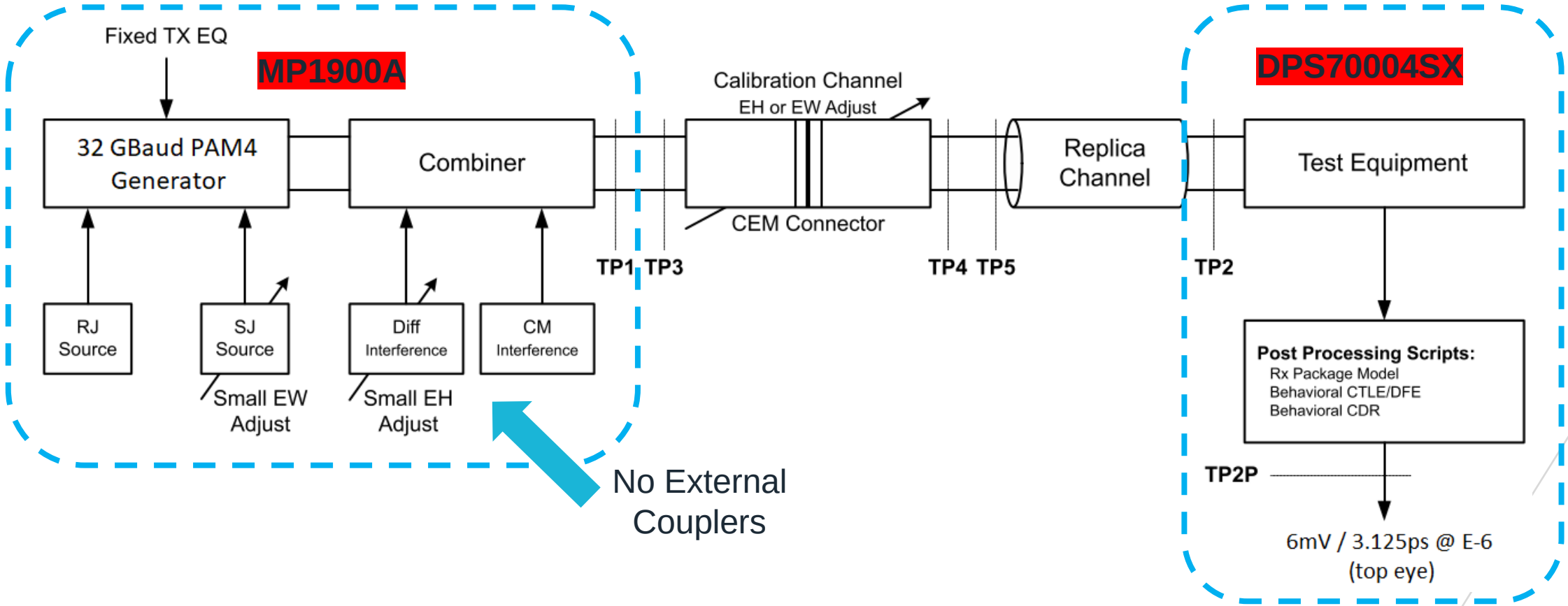
Receiver Equalization Updates





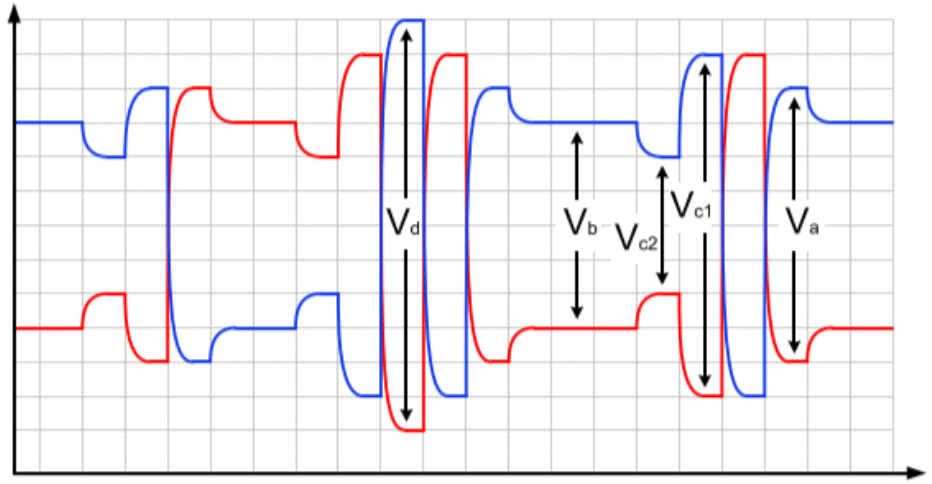
- **CTLE:** 64 GT/s
  - 6 Poles & 3 Zeros
  - DC Gain: -5dB to -15dB (1dB steps)
- **DFE:** 64 GT/s
  - 16 taps (-d1, -d2, … , -d16)
  - DFE taps constrained to min burst errors
  - Empirical formula in spec

PAM4 64 GT/s Stressed Eye Calibration



TP3 Calibration Updates

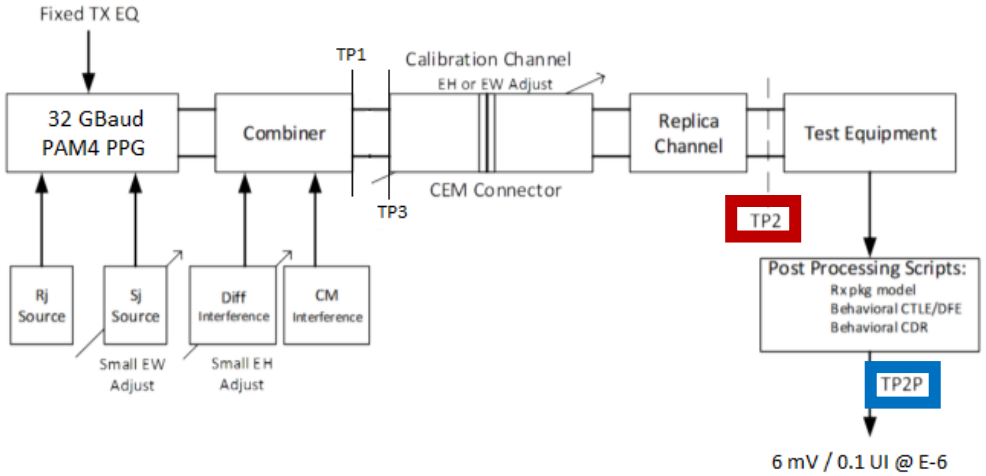
Tx Coefficient Dependencies			
	C_{-2}	C_{-1}	C_{+1}
Pre-shoot 2	Yes	Yes	Yes
Pre-shoot 1	No	Yes	No
De-emphasis	No	No	Yes



- TP3 include $V_{peak\text{-}peak}$, AC/DC Balance, Tx EQ, Rj, & Sj
- Cable (TP1 to TP3) excluded from 30 to 33 dB channel loss
- Tx Equalization: C_{-2} depends on C_{-1} & C_{+1}
- Rj (250 fs) & Sj (1 to 3 ps) Calibration with 52 UI pattern & noise compensation
- Sj Multi-tone Calibration 33 KHz (SSC) & 400 KHz to 100 MHz

TP2 Calibration Updates

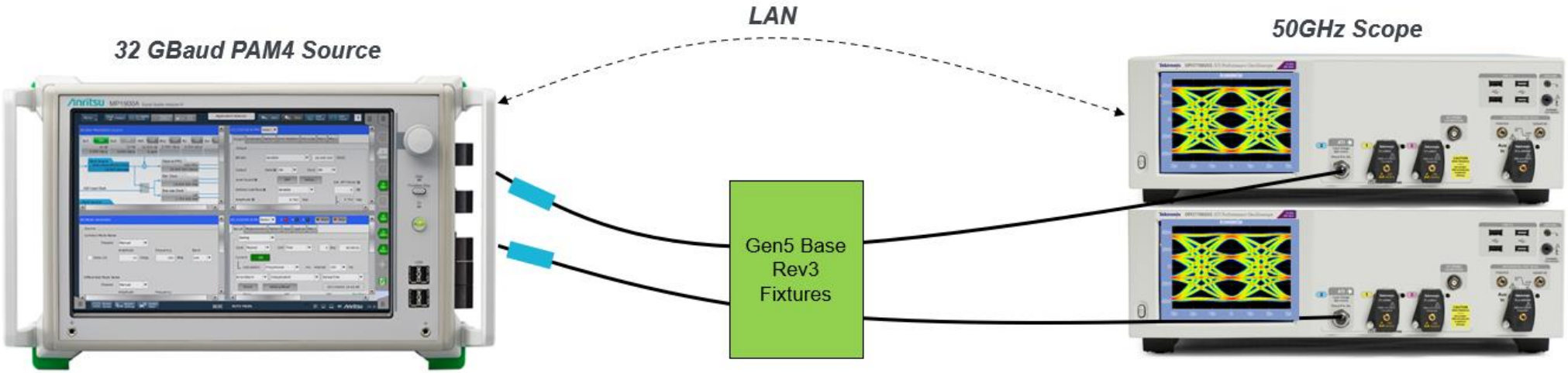
- DMI (2.1 GHz) : 5 to 25 mV @ TP2
  - Seasim injects at **TP2P**
  - BERT calibration at **TP2** (no CTLE or package)
  - Conversion factor required
- Seasim SNDR (input) – noise compensation
- Channel Loss: 30 to 33 dB (TP3 to TP2P)
- Step Response includes Tx EQ
- Stress
  - Sj: 1 to 3 ps
  - Rj: 250 fs



Seasim adaptation

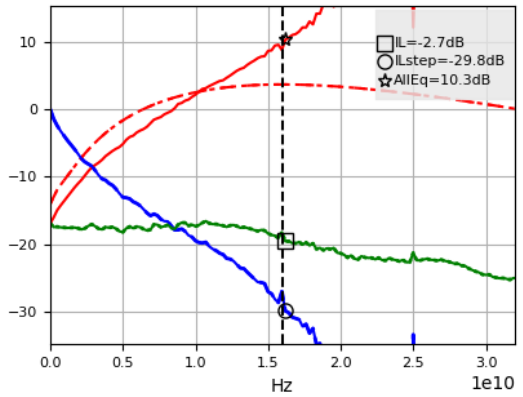
CTLE Curve DC Gain	-15	-14	-13	-12	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2
CTLE Loss @ 2.1 GHz	-7.611	-7.288	-6.912	-6.482	-5.994	-5.449	-4.848	-4.193	-3.488	-2.737	-1.946	-1.120	-0.263	0.620
CTLE Conversion Factor	2.402	2.314	2.216	2.109	1.994	1.873	1.747	1.621	1.494	1.370	1.251	1.138	1.031	0.931
RC Package Rev0p7 Conversion Factor	1.241	1.241	1.241	1.241	1.241	1.241	1.241	1.241	1.241	1.241	1.241	1.241	1.241	1.241
NRC Package Rev0p7 Conversion Factor	1.105	1.105	1.105	1.105	1.105	1.105	1.105	1.105	1.105	1.105	1.105	1.105	1.105	1.105
DMSI Conversion Factor RC Package	2.982	2.873	2.751	2.618	2.475	2.325	2.169	2.012	1.855	1.701	1.553	1.412	1.280	1.156
DMSI Conversion Factor NRC Package	2.654	2.557	2.449	2.331	2.203	2.069	1.931	1.791	1.651	1.514	1.383	1.257	1.139	1.029

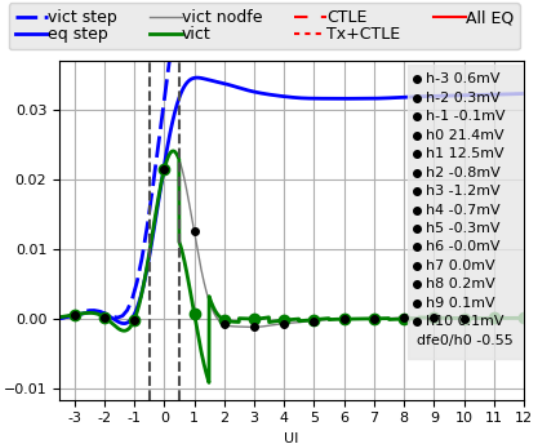
PAM4 Stressed Eye Example



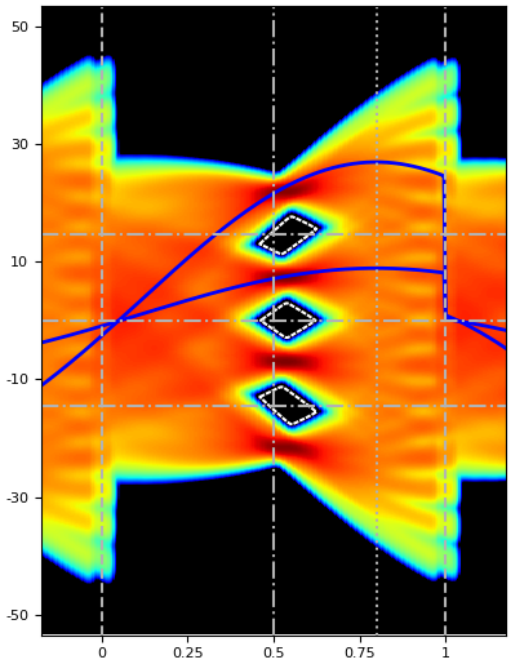
- **Source:** PAM4 PPG
  - 64 GT/s (32 GBaud PAM4) – Step Response
  - Tx EQ Pre Cursor 1 & 2 optimized
- **Channel:** 33.1dB @ 16GHz
  - Gen5 Base Rx Fixtures
- **Scope:** Real Time Scope (50 GHz)
  - 50 GHz with 200 GS/s
  - Root Complex package embedded
- **Post Processing:** Seasim 1.0.6
  - CTLE/DFE
  - Sj, Rj, & Crosstalk (DMI)

Successful 64 GT/s Rx Calibration





step=Seasim_StepResponse
LEQ=CTLE_gen6_0p7_Proposal_AMD_rev1_May2020.pkl
job=step_responses_Seasim_StepResponse_32.00G_1
UI=31.25ps PAM4 v1.06

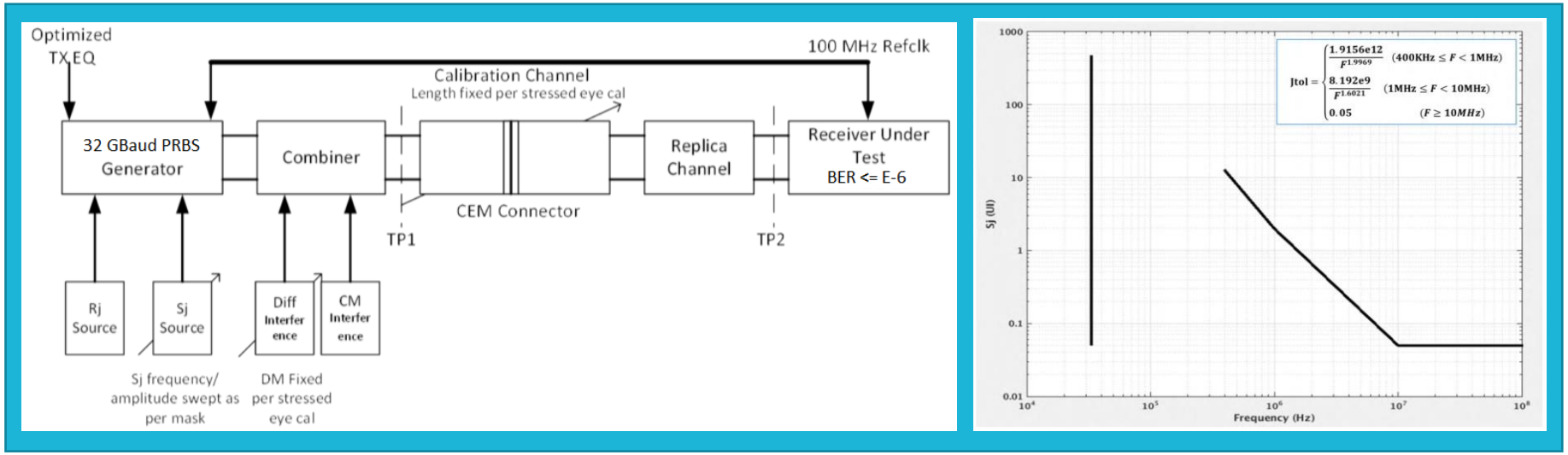


	1e-06
eh top	5.59mV
eh mid	5.83mV
ew top	0.110UI
ew mid	0.159UI
pkeh off	0.040UI
vref top	14.5mV

```
pwrj          0.20ps
pwddj         0.12ps
lfrj          0.25ps
lfddj         1.70ps
UTJ           4.49ps @1e-06
vn_lfudn      1.7mV pkpk
Tx SNDR       -
lanes         1
aggr align    center
nui           120
adapt_nui     20
precursors    2
cursor block  4
preCompTxEQ   False
vbin          0.035mV
tbin          0.156ps
Adapt FOM     area
Tx coeff      [-0.000,1.000,-0.000]
DFE coeff     [
    -11.8,  0.7,  1.2,  0.5,  0.2,  0.0,
      0.0, -0.2,  0.0,  0.0,  0.0,  0.0,
      0.0,  0.0,  0.0,  0.0]
DFE quant     128
cursor delay -0.300UI
DC_idx        1
pole_idx      0
```

- ✓ Channel Loss: 33.1 dB
- ✓ Tx Preset: Q8
- ✓ Rj: 250 fs
- ✓ Sj: 1.7 ps
- ✓ DMI: 4.8 mV @ TP2

Rx Jitter Tolerance Methodology



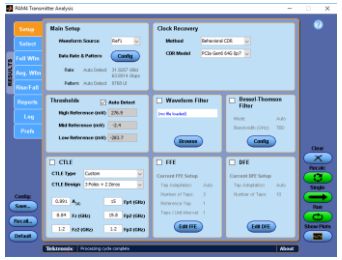
- **Modified Compliance pattern**
  - SSC disabled on data signal
- **Tx Eq may be optimized for Rx**
- **Independently swept 33 KHz tone**
  - Common Clock – swept to 1ns
  - SRIS – swept to 15ns

- **JTOL mask - 400 KHz and 100 MHz**
- **Additional 210 MHz tone (Sj > 0.05UI)**
- **FBER target of E-6**
  - Without accounting for burst errors

Tektronix PCIe 6.0 Solutions

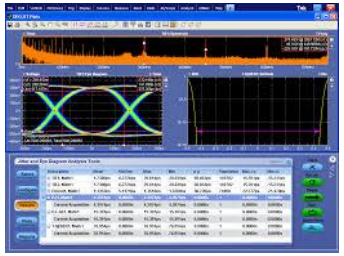
Tektronix PCI Express 6.0 Solution

PAM4 Analysis Application



SDLA

DPOJET Plugin for Debug



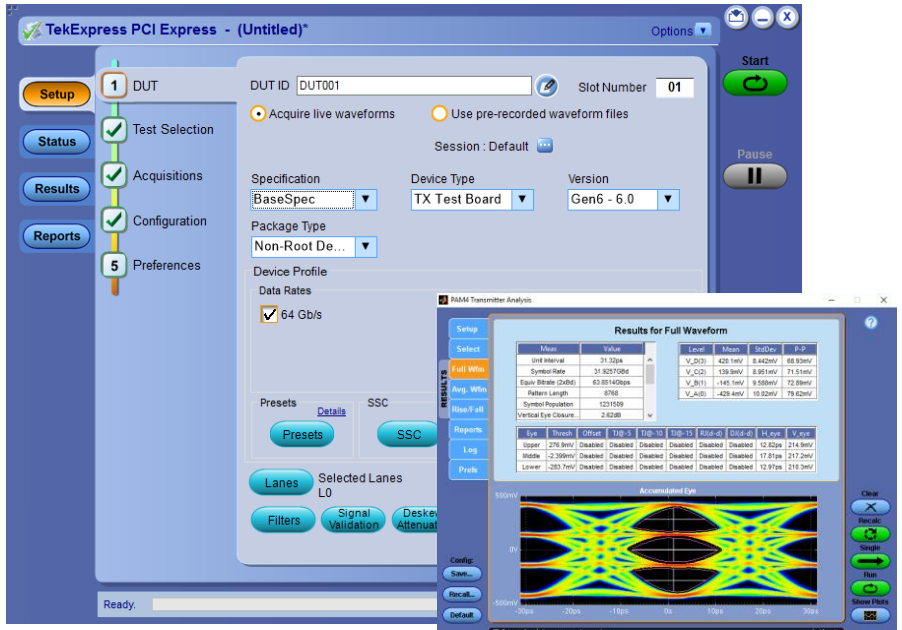
Tektronix Innovative Gen6 DSP Tools

Transmitter

Base | CEM | Ref CLK

PAM4 Analysis App & DPOJET

TekExpress Automation



PCIe Gen5 CEM Fixtures Enable Early Gen6 Signal Access

Tektronix is ready for Gen6 customer engagements today – contact local representative

Tektronix TMT4 (Margin Tester)

Tektronix TMT4 Margin Tester

Simple setup and configuration

minimizes the need for senior engineers to perform margin testing

Targeted Tx/Rx capability

to capture high-level design issues with PCIe Gen 3 and Gen 4 communication technologies on both ends of the link in a single box

Multi-lane testing

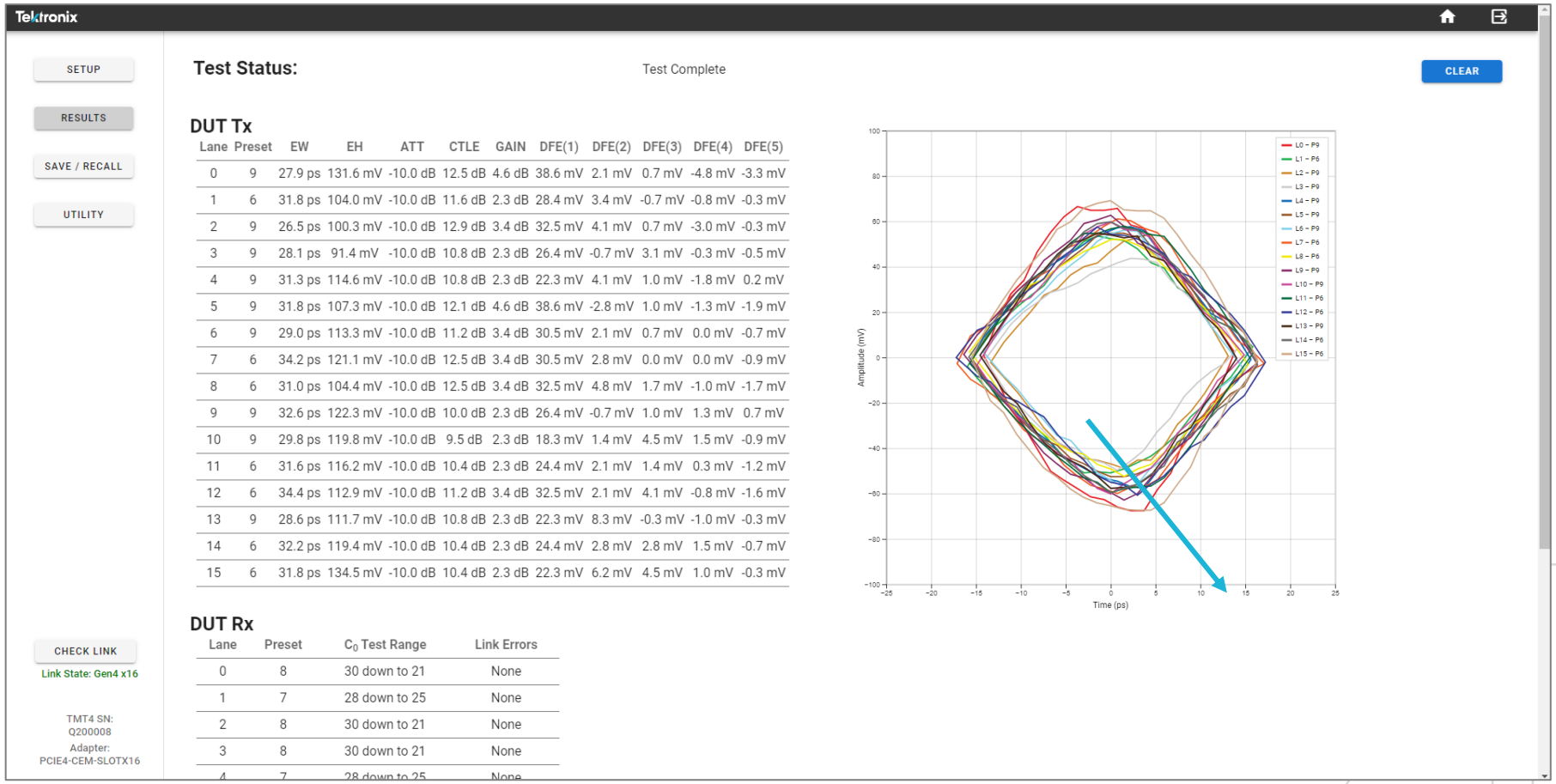
reduces testing times for preliminary link health evaluation of link health and gain insights into potential design margins issues

Margin-specific testing solution

to assist in more frequent testing of PCIe Gen 3 and Gen 4 devices in development to build confidence in validation and compliance

TMT4 Margin Tester Quick Scan – Tx and Rx

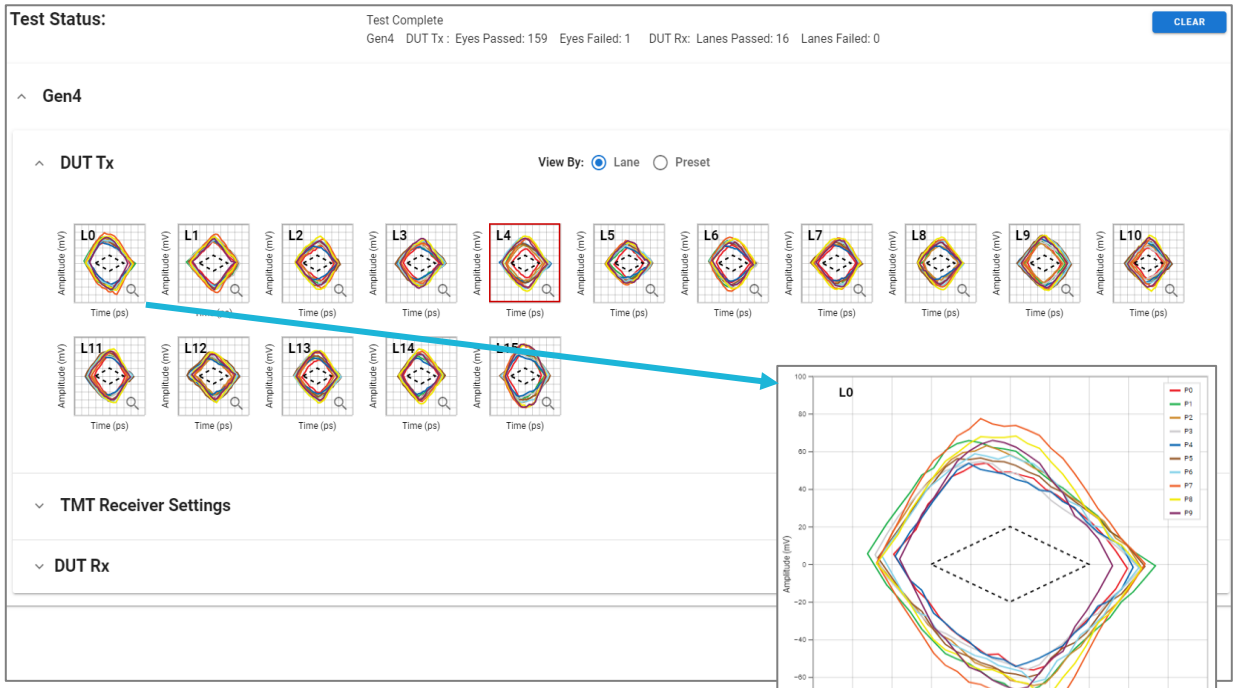
1. DUT and Margin Tester **train naturally** and negotiate presets for **Tx test**
   - Display eye diagram & link training parameters
2. DUT and Margin Tester **train naturally** and negotiate presets for **Rx Test**
   - Display outputs of Rx test range and link errors by lane/preset combination



Est. Test Time for Gen4 x16 DUTs: ~**2 minutes**

TMT4 Margin Tester Custom Scan – Tx Eye Diagrams

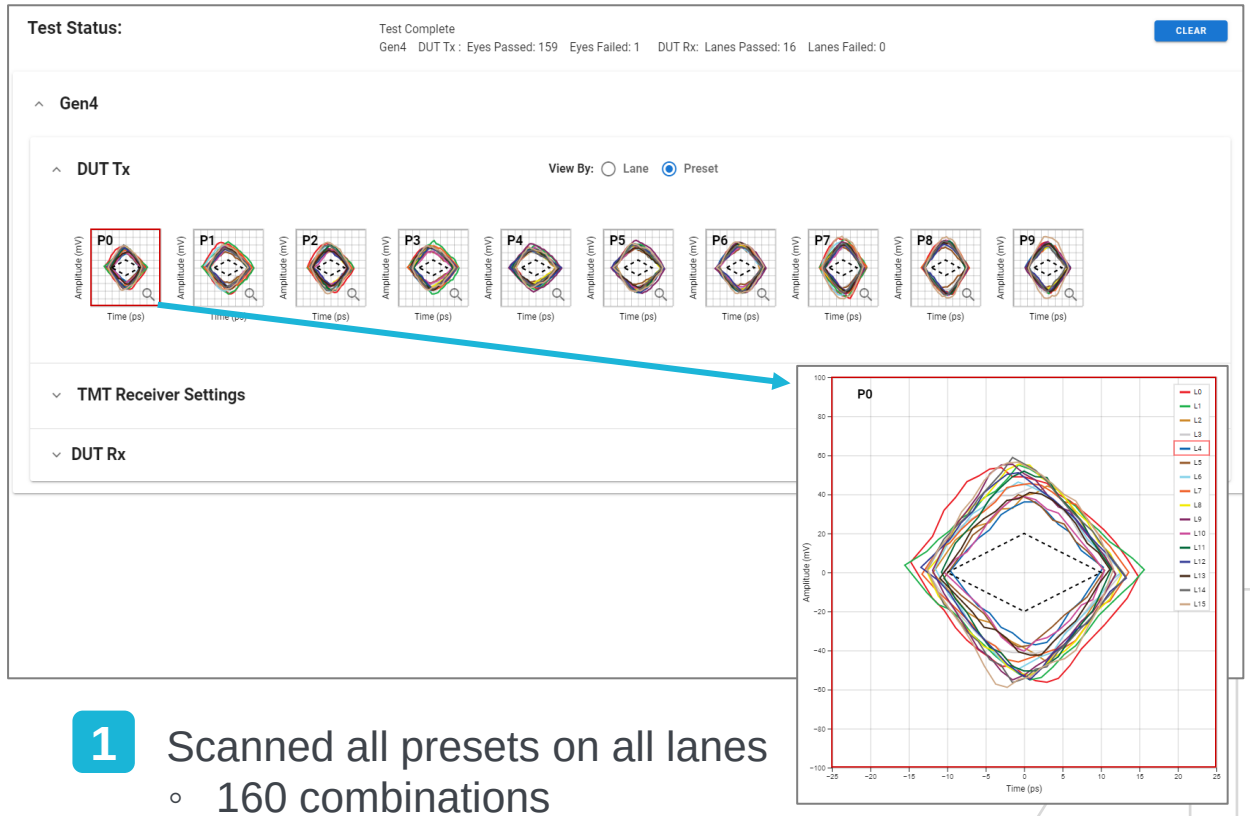
Presets Plotted Per Lane



1. Scanned all presets on all lanes
   - 160 combinations
2.
3. All presets plotted together for each lane

Very clear that there are **lane to lane variations**

Lanes Plotted Per Preset



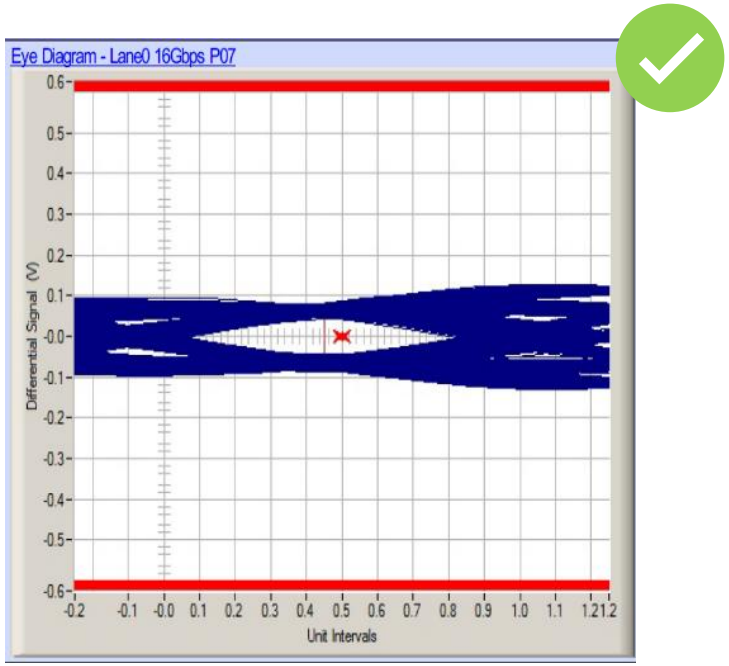
1. Scanned all presets on all lanes
   - 160 combinations
2. All lanes plotted together for each preset
3. Alternative view makes the lane-to-lane variations even clearer

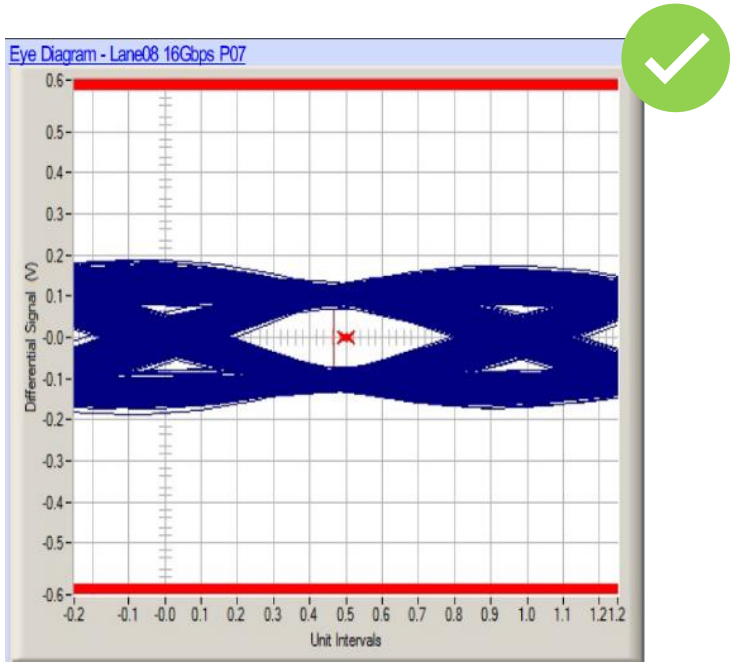
Est. Test Time for Gen4 x16 DUTs: **8-10 minutes**

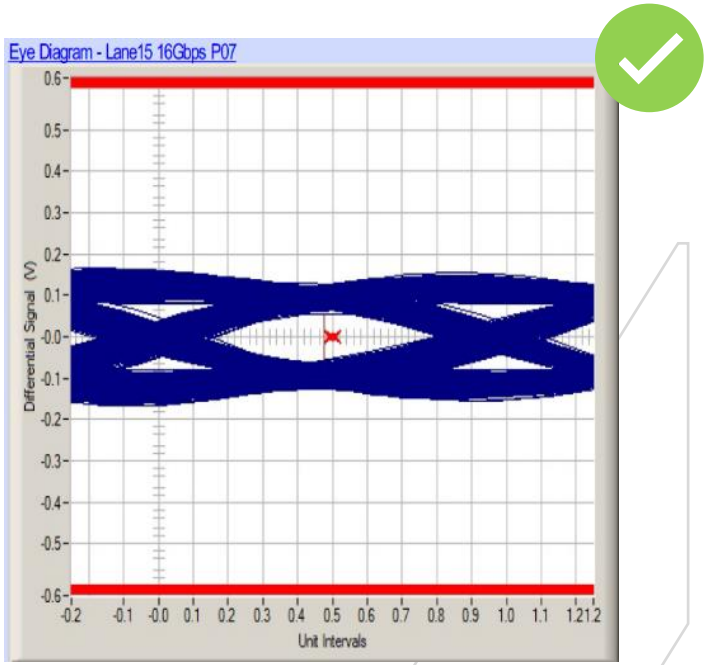
TekExpress Results – Gen 4 Re-Driver Design

A motherboard manufacturer was attempting to resolve an issue they were seeing with their re-driver gain setup.

They had used the reference design from their silicon vendor and were seeing passing results using Tektronix's TekExpress software and oscilloscope as shown in the diagrams below for lanes 0, 8, and 15.



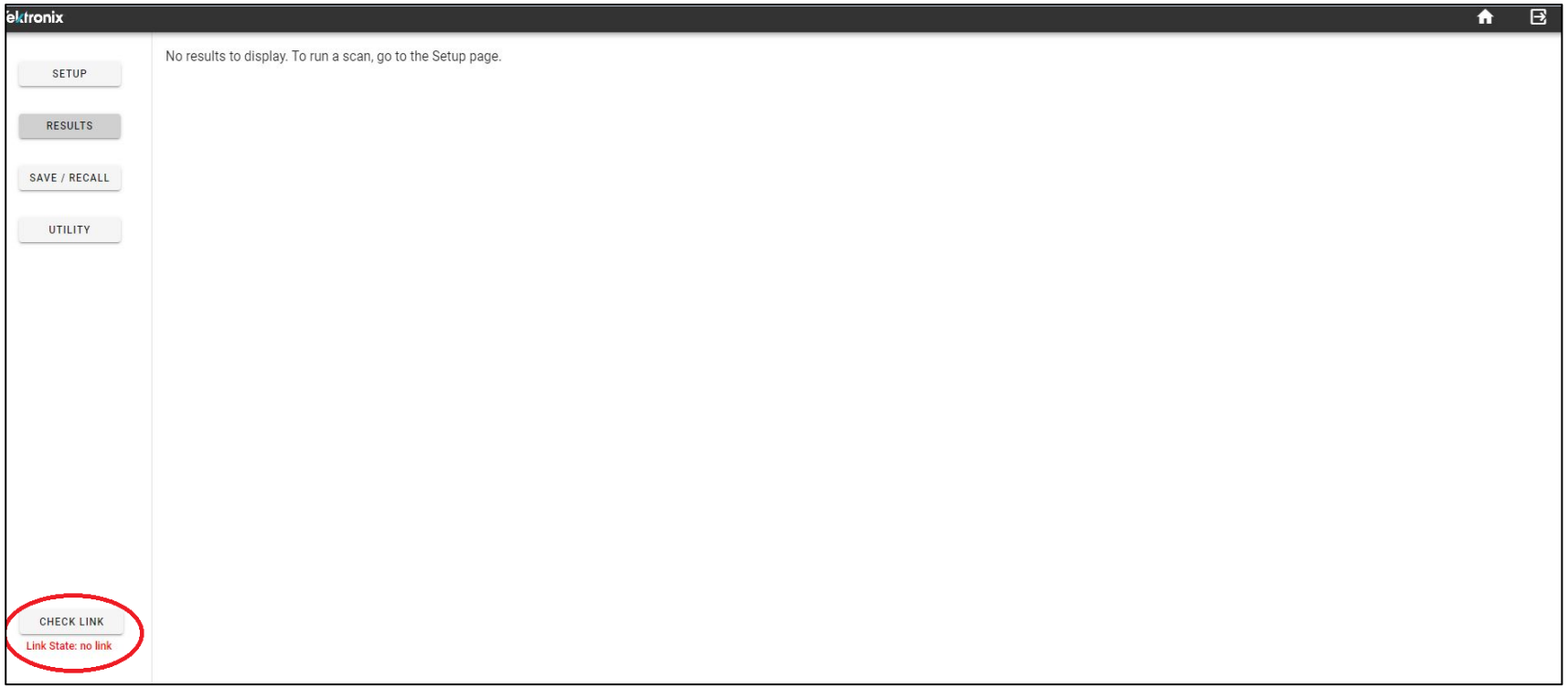




TMT4 Margin Tester Results – Scanning at Gen 4

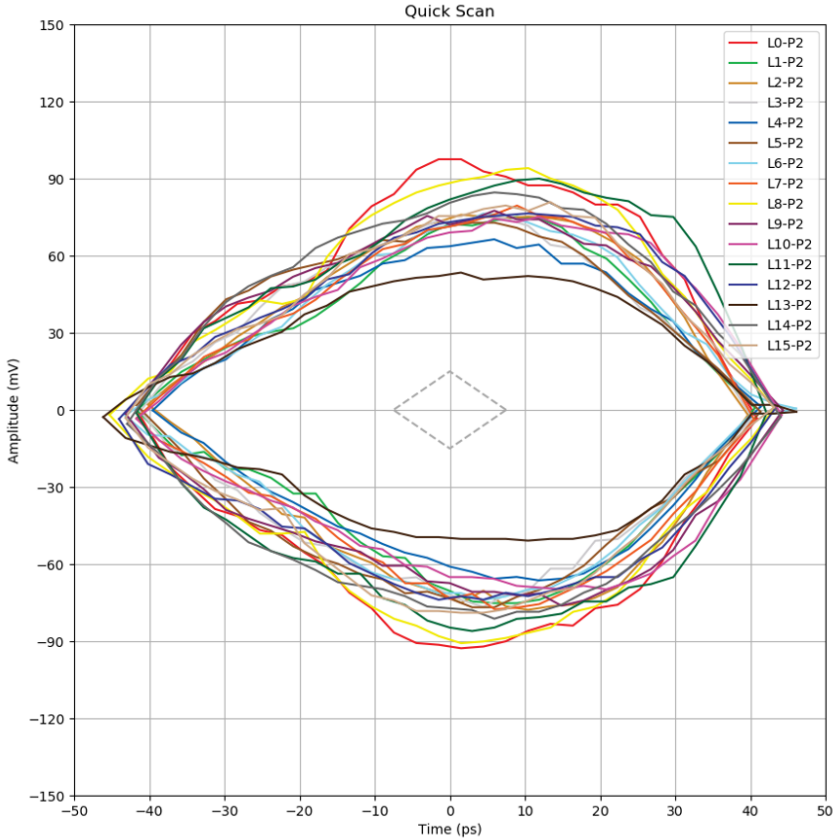
Despite these passing results, the manufacturer has been experiencing interoperability issues that they were unable to root-cause.

Using a TMT4 Margin Tester at Gen 4 speeds, they also ran into interop issues:



TMT4 Margin Tester Results – Gen 3

To try to draw insight into the interop issues, TMT4 Margin Tester was used to run a Quick Scan at Gen 3 speeds. TMT4 Margin Tester was able to link and test at Gen 3. Results and insights below:



lane	preset	eye_width	eye_height	att	vga	ctle	dfe1	dfe2	dfe3	dfe4	dfe5
0	2	82.6	190.3	-8.86	2.28	3.67	-2.04	0	7.21	1	1.71
1	2	82.3	150.3	-8.86	1.71	4.51	-12.19	8.25	5.15	0.25	0.68
2	2	79.9	153.0	-10	1.14	4.09	-6.1	0.68	2.06	1	0.85
3	2	81.5	152.3	-8.86	1.14	4.09	-10.16	1.37	1.03	-2	2.75
4	2	80.9	132.0	-7.72	1.14	3.25	4.06	4.12	2.4	1.5	3.78
5	2	83.0	149.6	-8.86	1.14	3.67	-2.04	3.43	3.78	2	3.26
6	2	89.3	150.3	-8.86	1.14	3.25	2.03	1.37	2.06	-0.25	3.26
7	2	82.2	156.4	-7.72	1.14	3.67	0	2.06	3.09	-0.25	2.92
8	2	88.5	182.1	-7.72	0	2	-18.29	-4.82	-1.04	-3.25	1.03
9	2	87.5	148.3	-5.43	0.57	2	-12.19	-4.13	-0.69	-3.25	-0.69
10	2	85.9	144.2	-7.72	0	2	-14.22	[illegible]	-1.38	-1.75	0.34
11	2	83.9	172.0	-7.72	0	2	-20.32	-3.44	-3.44	-1.25	-2.07
12	2	87.3	149.0	-7.72	0.57	2	-2.04	0.68	[illegible]	-2.25	1.2
13	2	92.3	103.6	-8.86	0	2	-2.04	3.43	-2.41	-1.5	-0.52
14	2	87.0	165.9	[illegible]	0	2	-8.13	-2.75	-1.04	[illegible]	0.51
15	2	86.3	157.1	-7.72	0.57	2	-8.13	6.87	2.4	-1.25	1.03

Equalization of lanes 8-11 and eye height of lane 13 indicate potential issues with the back 8 lanes of the re-driver design

Lane 13 eye almost half the height of Lane 0 eye

Higher levels of DFE 1 equalization for lanes 8-11 compared to all other lanes

Conclusions

1. In just 5 minutes of testing, the user was able to identify that the problems with their re-driver setup likely lies in the back 8 lanes of their re-driver setup.

2. The TMT4 Margin Tester also replicated the interoperability issues that were seen at Gen 4 speeds, but, with a quick Gen 3 test, were able to identify lanes 8-11 and 13 as the primary lanes of interest for causing their interop issues at Gen 4 speeds.

THANK YOU

Contact Information

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High Speed Signals Symposium