Tektronix® | TekDay 2025 -High Speed Hsinchu

PCIe技術從Gen5 to Gen6的遷移解決方案

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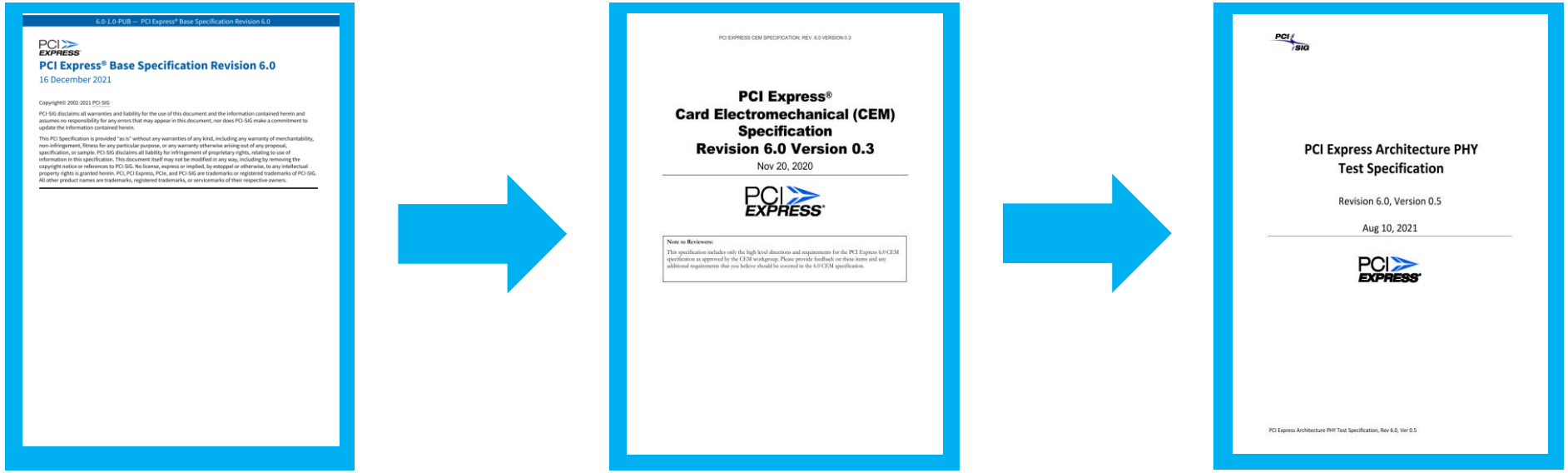
PCI Express 6.0 Specification Overview

PCIe 6.0 Specification Snapshot (Q1 2025)

- **PCIe 6.2 Base Specification – Rev 1.0 released (Q1 2022)**
  - Describes chip-level behavior on all levels of the stack
- **PCIe 6.0 CEM Specification – Rev 0.9 under development**
  - Card electro-mechanical (CEM) defines the system and Add-in Card level
- **PCIe 6.0 PHY Test Specification – Rev 0.7 under development**
  - Describes electrical compliance tests for Tx, Rx LEQ, & PLL Bandwidth

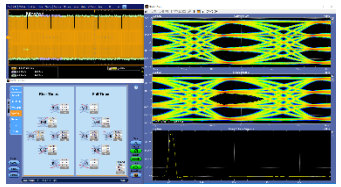


PCIe6 Solutions Landscape

Released

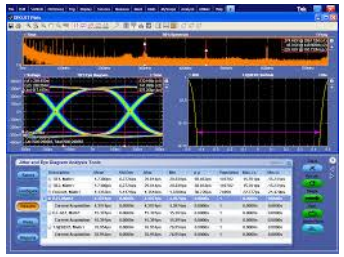
Under development for Gen6 CEM

PAMJET (PAM4 Analysis)



SDLA
Embed/De-embed, CDR, Equalization

DPOJET Plugin for Debug

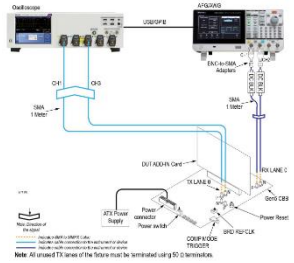


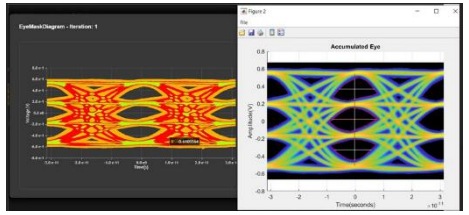
Transmitter

- BASE-TX*
- CEM-TX
- PLL bandwidth
- Ref Clk

PAMJET + DPOJET + SDLA

TekExpress





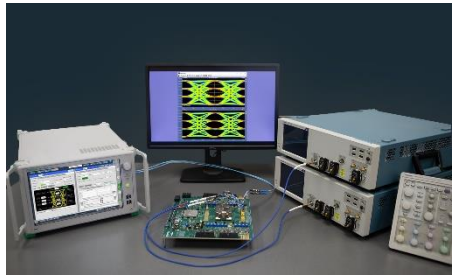
Receiver

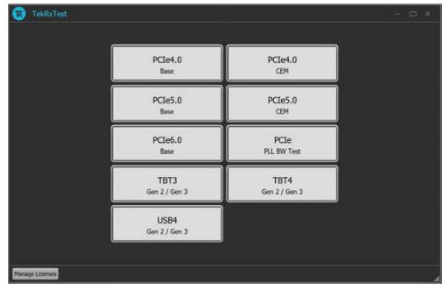
- BASE-RX*
- CEM-RX

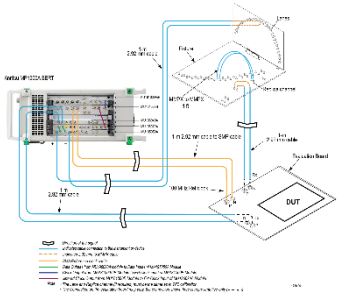
BERT Calibration/JTOL

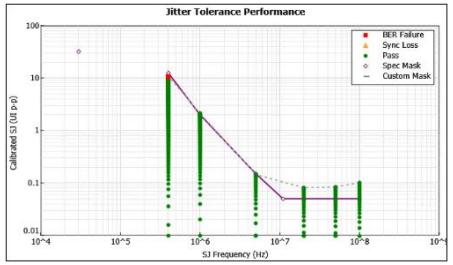
Link Equalization

TekRXTest









*Fully featured Gen6 BASE solution per spec.

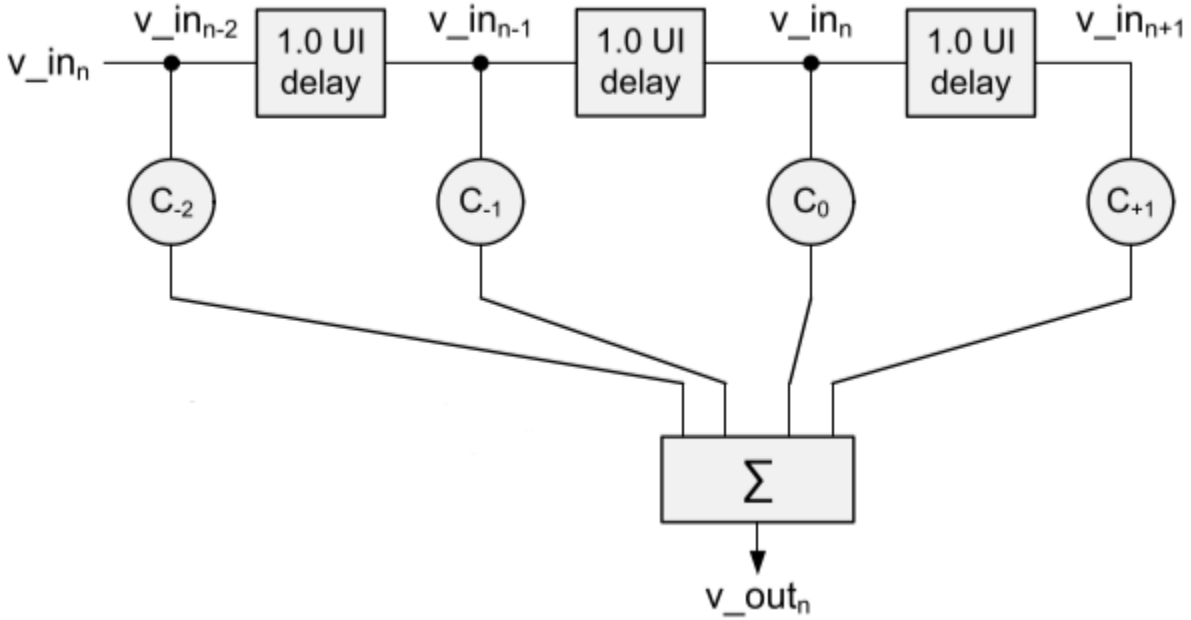
PCIe 4.0 to 6.0 Base Specification Changes

Parameters	PCIe 4.0	PCIe 5.0	PCIe 6.0
Data Rate	16 GT/s	32 GT/s	64 GT/s (PAM4)
Add-in Card Loss	8dB @ 8Ghz	9.5dB @ 16GHz	8.5dB @ 16GHz
Rx Test (Channel Loss)	- (27 to 30) dB @ 8GHz	- (34 to 37) dB @ 16GHz	- (30 to 33) dB @ 16GHz
Reference CTLE	2 Poles; 1 Zero; DC Gain Range (-6 to -12) dB	4 Poles; 2 Zero; DC Gain Range (-5 to -15) dB	6 Poles; 3 Zero; DC Gain Range (-5 to -15) dB
Reference DFE	2-Taps	3-Taps	16-Taps
Eye Width (Rx Test)	18.75 ps	9.375 ps	3.125 ps (top eye)
Eye Height (Rx Test)	15 mV	15 mV	6 mV (top eye)
Lane Margining	Required timing only	Required timing/voltage	Required timing/voltage
Refclk Jitter Limits	<= 500 fs	<= 150 fs	<=100 fs
Min Scope BW	25 GHz	50 GHz	50 GHz

PCIe 6.0 Base Tx Measurements

TX Test	Pattern	Notes
SNDR	Compliance	Signal Noise Distortion Ratio
Voltage Differential Peak-to-Peak	Compliance	Measured with 64 level 3s & 64 level 0s
Transmit Equalization	Compliance	Q0-Q10 (PAM4) with AC step method
Tx Equalization Boost	Compliance	Q10 (full swing) & Q4 (reduced swing)
EIEOS Min Voltage Swing	Compliance	Include package loss impact
Ratio Level Mismatch	Compliance	PAM4 measurement only
Uncorrelated Tj	52UI Jitter Measurement	Jitter computed on each unique transition
Uncorrelated Dj	52UI Jitter Measurement	Jitter computed on each unique transition
Uncorrelated Rj	52UI Jitter Measurement	Informative
Pulse Width Jitter Tj	High Swing Toggle	0303 level patten; noise comp included
Pulse Width Jitter Dj_dd	High Swing Toggle	0303 level patten; noise comp included
Pulse Width Jitter Rj	High Swing Toggle	Informative
PS21	Compliance	Pseudo package loss

Transmitter Equalization Expansion

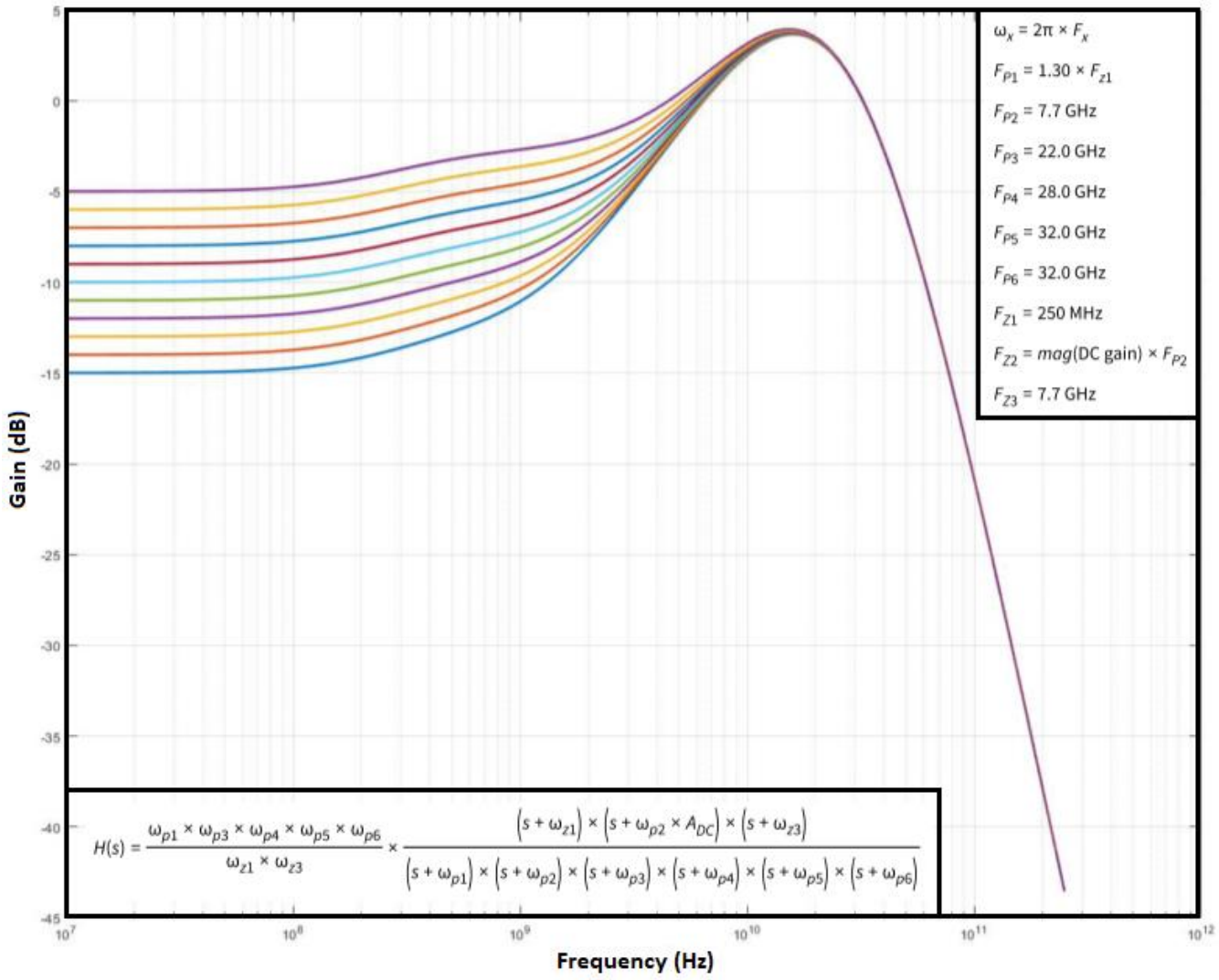


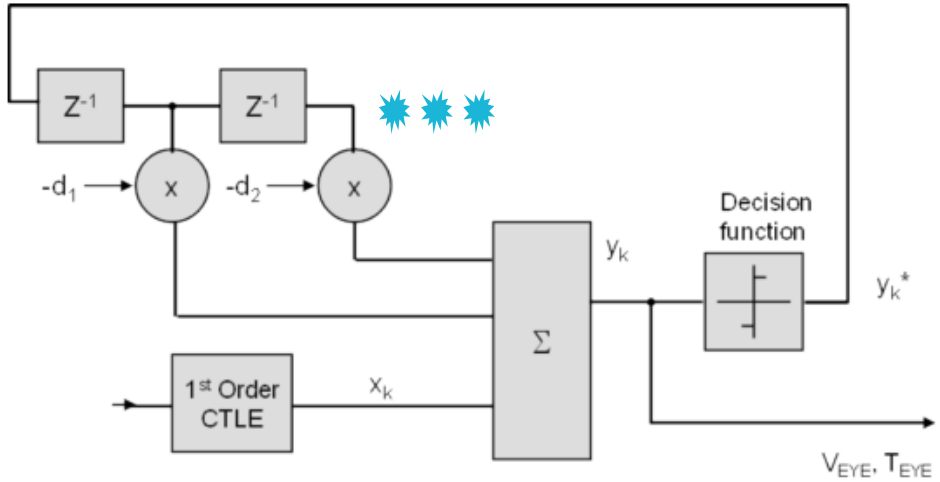
Preset #	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q0	0.0 ±0.5 dB	0.0 ±0.5 dB	0.0 ±0.5 dB	0.000	0.000	0.000	1.000	1.000	1.000	1.000
Q1	0.0 ±0.5 dB	1.6 ±0.5 dB	0.0 ±0.5 dB	0.000	-0.083	0.000	0.834	0.834	1.000	0.834
Q2	0.0 ±0.5 dB	3.5 ±0.5 dB	0.0 ±0.5 dB	0.000	-0.167	0.000	0.666	0.666	1.000	0.666
Q3	0.0 ±0.5 dB	0.0 ±0.5 dB	-1.6 ±0.5 dB	0.000	0.000	-0.083	1.000	0.834	0.834	0.834
Q4	0.0 ±0.5 dB	0.0 ±0.5 dB	-3.5 ±0.5 dB	0.000	0.000	-0.167	1.000	0.666	0.666	0.666
Q5	-1.3 ±0.5 dB	4.7 ±1.0 dB	0.0 ±0.5 dB	0.042	-0.208	0.000	0.584	0.584	1.000	0.500
Q6	-1.6 ±0.5 dB	3.5 ±0.5 dB	-3.5 ±0.5 dB	0.042	-0.125	-0.125	0.750	0.500	0.750	0.416
Q7	-2.9 ±0.5 dB	4.7 ±1.0 dB	0.0 ±0.5 dB	0.083	-0.208	0.000	0.584	0.584	1.000	0.418
Q8	-3.5 ±0.5 dB	6.0 ±1.0 dB	0.0 ±0.5 dB	0.083	-0.250	0.000	0.500	0.500	1.000	0.334
Q9	-4.4 ±1.0 dB	6.9 ±1.0 dB	-1.6 ±0.5 dB	0.083	-0.250	-0.042	0.500	0.416	0.916	0.250
Q10	0.0 ±0.5 dB	0.0 ±0.5 dB	Note 2	0.000	0.000	Note 2	1.000	Note 2	Note 2	Note 2

- **Cursor Expansion:** 2nd Precursor Added
  - 2 pre-cursors
  - 1 post-cursor
- **Presets:** Q0 to Q10
  - Heavier pre-cursor weighting
  - Numerous optimal presets for Rx Calibration

- **Measurement Method:** AC Method
  - Step response captured
    - *Equalized & Non-Equalized*
  - Cursors applied to Non-Equalized step
  - Minimized Mean Square Error (MSE)

Receiver Equalization Expansion





- **CTLE:** 64 GT/s
  - 6 Poles & 3 Zeros
  - DC Gain: -5dB to -15dB (1dB steps)
- **DFE:** 64 GT/s
  - 16 taps (-d1, -d2, … , -d16)
  - DFE taps constrained to min burst errors
  - Empirical formula in spec

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PCI Express 6.0 CEM Compliance Program Overview

PCI Express 6.0 CEM Compliance Program

- First PCIe 6.0 CEM Pre-FYI Workshop (June 3rd, 2024, week).
- Status will remain "Pre-FYI" until test methodologies, test fixtures, analysis tools (Seasim & SigTest), and test specifications are finalized.
  - Second Pre-FYI Workshop (October 14th, 2024, week).
  - Correlation between test vendors performed.
- Status changes to "FYI" and must maintain collateral stable for 6 months.
- No requirement for # of 6.0 FYI workshops.
- Latest Pre-FYI Workshop scheduled March 24-28, 2025
- Official integrators list testing can begin.
  - https://pcisig.com/developers/integrators-list

PCIe Compliance Testing

PCIE COMPLIANCE TESTING FOR INTEROPERABILITY

- PCIE holds regular compliance workshops/plugfests to certify individual devices' compliance and interoperability, typically 4x/yr
- Vendors who desire to be on PCI-SIG Integrator's List plan to attend PCI-SIG workshops where they must pass all four electrical tests & 80% of interoperability tests
- These vendors look at tests and test equipment and assume that if they buy & use the same equipment, they will pass the workshop electrical tests

PCIE 6.0 Electrical PHY Compliance Tests
Transmitter Testing
Tx/Rx Link Equalization Testing
PLL Loop Bandwidth Testing
RefClk Testing

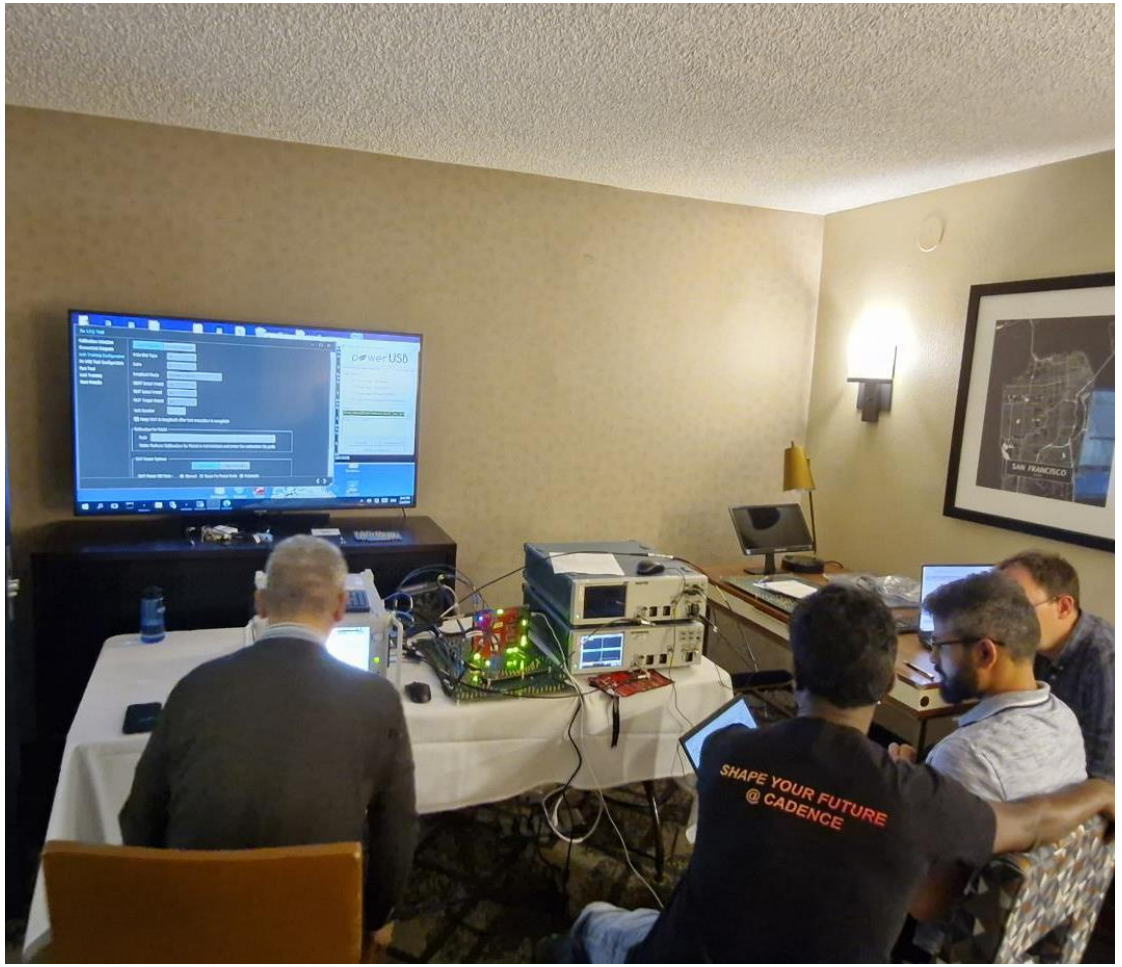
For more details visit PCI Compliance program:
http://www.pcisig.com/specifications/pciexpress/compliance/compliance_library#electrical30

PCIe 6.0 Electrical Tests

- **Transmitter (Tx) Signal Quality Test at 64GT/s**
  - End of channel eye diagram (eye width & eye height) @ BER E-6
  - Feasibility still under exploration by the PCI-SIG workgroups
- **Tx Preset Equalization Test at 64GT/s**
  - Measures voltage levels for Preset 0 to Preset 10 (AC method)
- **Tx Uncorrelated Jitter at 64GT/s (Add-in Card only)**
  - Intrinsic jitter of the Tx after removing channel impact
- **Tx Pulse Width Jitter (PWJ) at 64GT/s (Add-in Card only)**
  - Measure of the variation between adjacent rising & falling edges
- **Tx PLL Bandwidth (Add-in Card only)**
  - Verifies an Add-in Cards Tx PLL bandwidth and peaking
- **Tx Signal to Noise Distortion Ratio (SNDR) at 64GT/s (Add-in Card only)**
- **Tx Ratio Level Mismatch (RLM) at 64GT/s**
- **Link Equalization at 64GT/s**
  - Tx starts with correct preset requested through protocol
  - Tx responds to protocol changes and adjusts
  - Receiver (Rx) correctly adjusts the link Tx and meets error criteria with a stressed signal

PCIe Gen6 CEM – What's new

- **SNDR**
  - ECN released for new Pmax (sum of Np) & Sigma E (even/odd pulse)
  - Consensus reached to remove System SNDR test
- **RLM**
  - Tektronix proposed multi-pulse RLM method (28dB - SSC/Stress demonstrated)
  - ECR approved by EWG (May/2024)
  - https://members.pcisig.com/wg/PCIe-Electrical/document/20910
- **SigTest PAM4 support**
  - Early SigTest 6.0 build available for Rx TP3 Cal; TP2 for Seasim.
  - Tektronix PAMJET used for Tx until SigTest available/stable
- **Compliance program**
  - Tektronix attended and supported Tx, Rx, & PLL BW at first Pre-FYI workshop in June 2024.
  - **3rd FYI workshop scheduled in March 2025.**



PCIe Gen 6 Pre-FYI event (June 2024)

PCIe Gen6 CEM-TX Tests: System Host

PCIe Gen6 TX - system host	*Test pattern*	*Analysis Tool*	*CTLE Optimization*	*DFE*	*Noise compensation*	*Notes*
TX Preset Test (Q0 - Q10)	Gen6 Compliance pattern (all preset tests)	PAMJET	No	No	No	64GT/s data, CTLE used for clock recovery only, not waveform EQ.
TX Signal Quality (EW and EH at 1E-6)	Gen6 Compliance pattern	PAMJET	Yes	Yes	TBD*	50GHz acquisition BW, 4th order BT filter @ 33GHz, 12.5M capture @ 200Gs/sec (no interpolation)
RLM	Gen6 Compliance pattern	PAMJET	No	No	Yes	Preset Q0
100MHz refclk jitter	100 MHz Refclk	Skyworks PCIe Clock Jitter Tool	No	No	Yes	Capture 100MHz refclk

- Max channel loss expected = 27dB (23.5dB for System and 3.5dB for fixtures and cables)
- Tektronix working with EWG and SEG to finalize ECN (multi-pulse linear fit RLM method)
- *Tektronix can perform noise compensation for Tx Signal Quality tests. Noise compensation is anticipated for this measurement.

PCIe 6.0 CEM Tx Tests: Add-in Card

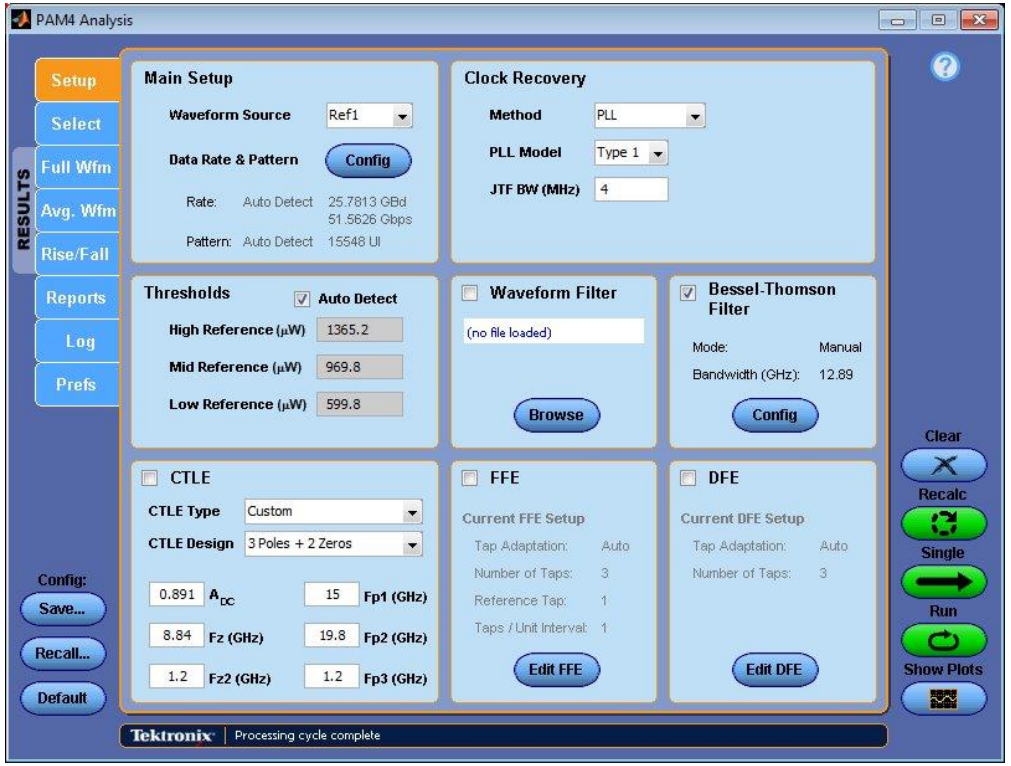
PCIe Gen6 TX - add-in card	*Test pattern*	*Analysis Tool*	*CTLE Optimization*	*DFE*	*Noise compensation*	*Notes*
SNDR	Gen6 Compliance pattern	PAMJET	No	No	Yes	Preset Q0
RLM	Gen6 Compliance pattern	PAMJET	No	No	Yes	Preset Q0
Uncorrelated Jitter TJ	52UI pattern	PAMJET	Yes	No	Yes	Preset Q0
Uncorrelated jitter DJ-dd	52UI pattern	PAMJET	Yes	No	Yes	Preset Q0
Uncorrelated jitter RJ	52UI pattern	PAMJET	Yes	No	Yes	Preset Q0
PWJ	High swing toggle pattern	PAMJET	Yes	No	Yes	Preset Q0
TX Preset Test (Q0 to Q10)	Gen6 Compliance pattern (all presets)	PAMJET & Sigtest	No	No	No	Presets Q0 to Q10
TX Signal Quality (EW and EH at 1E-6)	Gen6 compliance pattern	PAMJET	Yes	Yes	TBD*	50GHz acquisition BW, 4th order BT filter @ 33GHz, 12.5M capture @ 200Gs/sec (no interpolation)

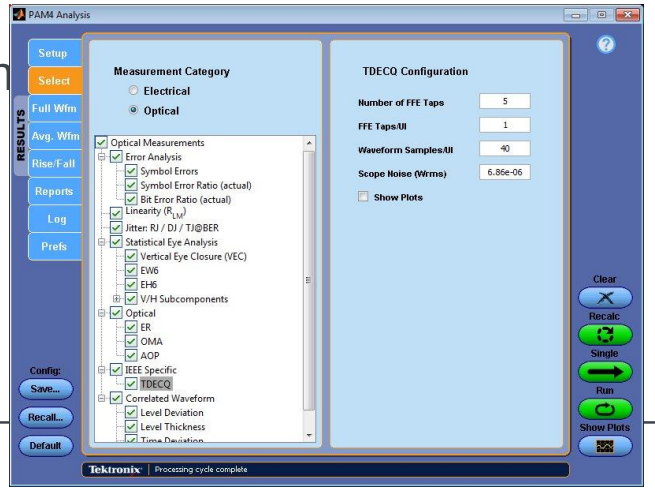
- Max channel loss expected = 12dB (8.5dB for AIC and 3.5dB for fixtures and cables)
- *Tektronix can perform noise compensation for Tx Signal Quality. Noise compensation is anticipated for this measurement.

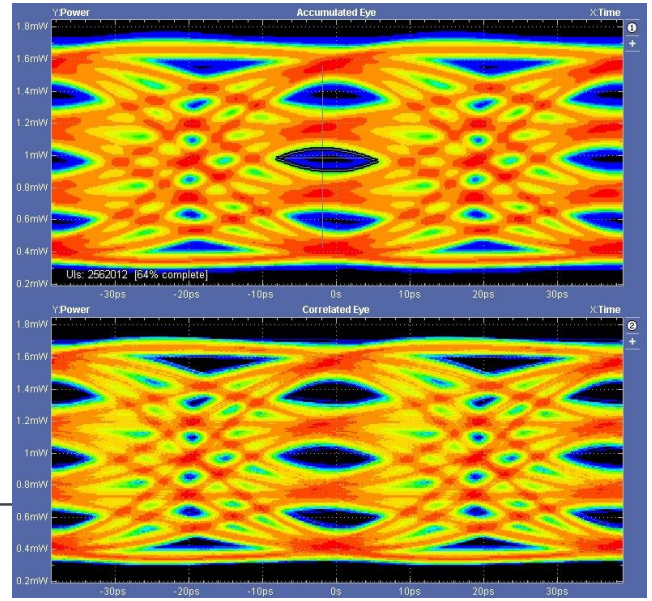
PCIe Gen6 – Debug Measurement Solution

PAMJET Software

- Industry best tool for PAM4 analysis
- Best-in-class clock recovery
- Integrated embedding and de-embedding
- Built-in functions to supports Gen 6 measurements
  - Configure measurement
  - Bessel Thompson filtering
  - CTLE optimization
  - SNDR
  - Noise characterization and compensation
  - Report results and eye diagrams.
- Gen 7 capability to do early debug



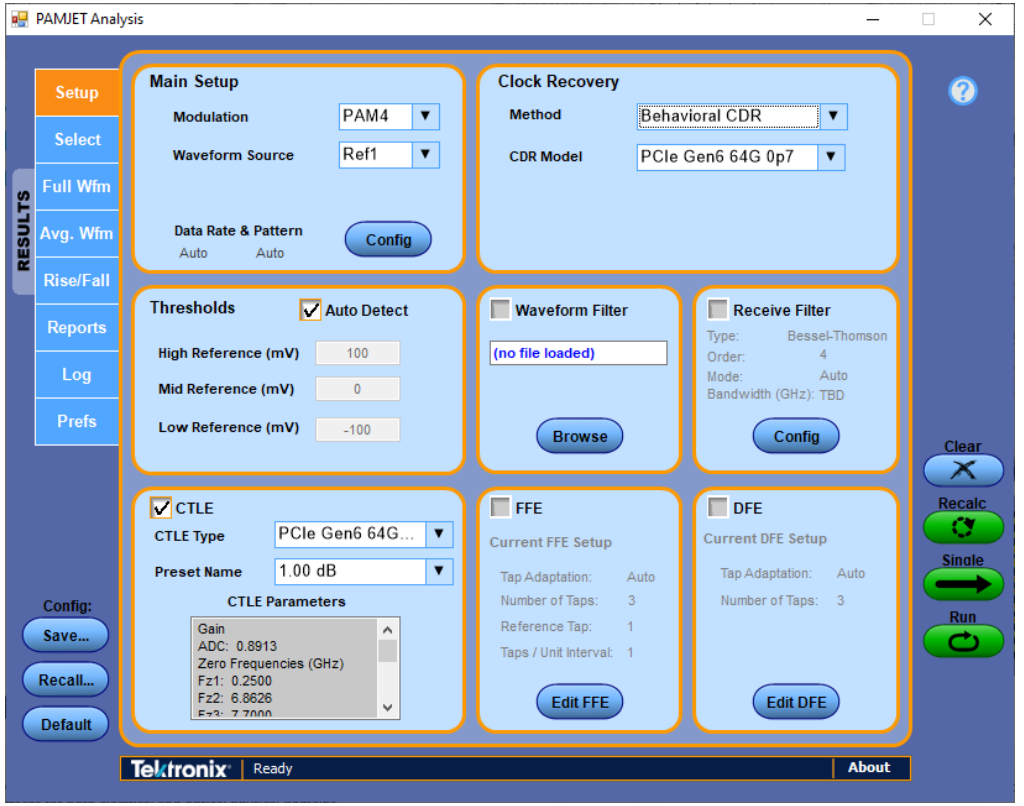


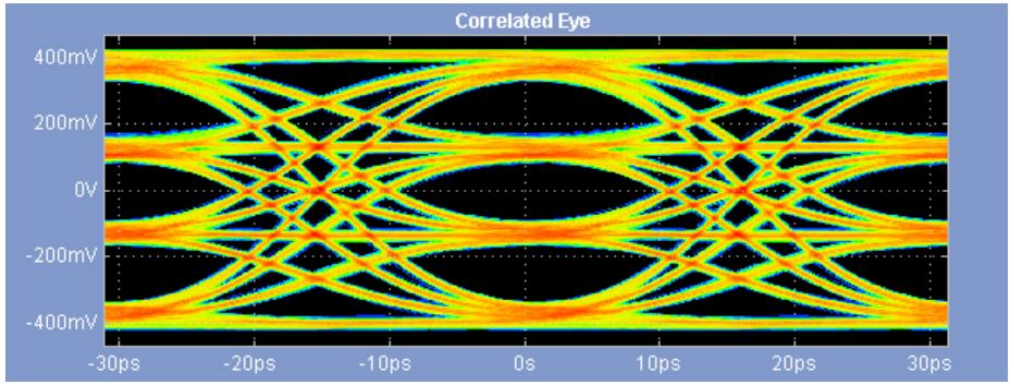


PAMJET – PCIe Gen 6

PAMJET provides PAM4 signal analysis for PCIe:

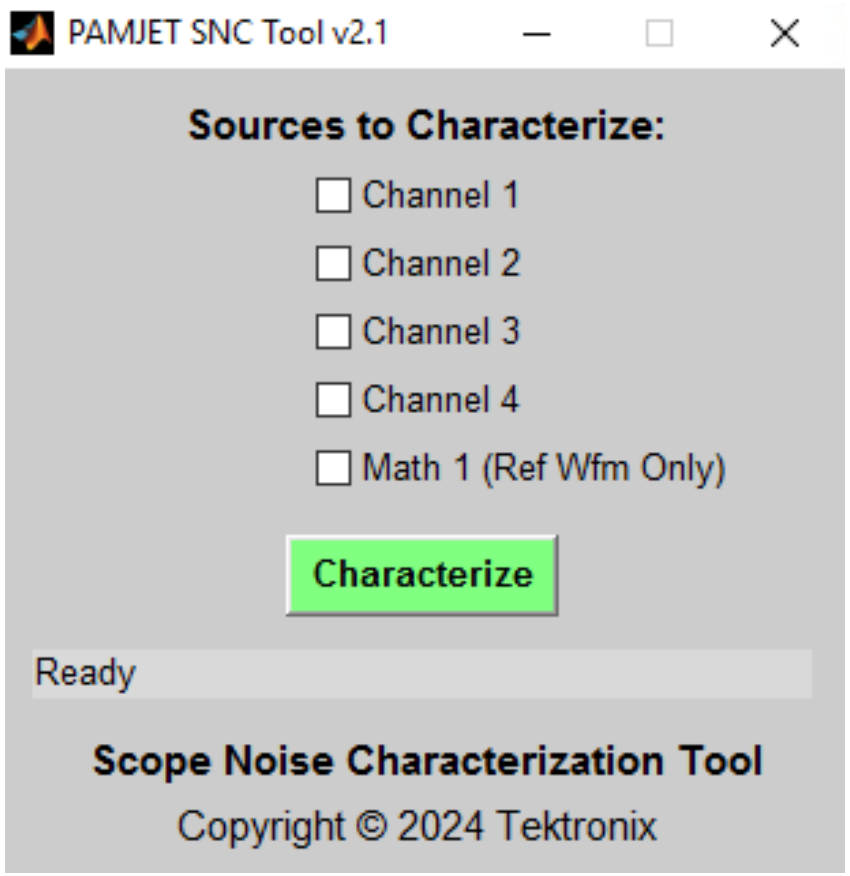
- Gen6 Base & CEM TX measurements:
  - SNDR, RLM-Tx, UI, VTx-diff-pp, Vtx-EIEOS, Vtx-Utj, TTx-UDJDD, TTx-RJ, TTx-UPW-TJ, TTx-UPW-DJDD, PS21-Tx, VTx-boost, VTx-AC-CM-pp, VTx-AC-CM-pp-filtered, PS21, Q0 to Q10 Tx Preset (AC method)
  - ECN (SNDR Pmax & σ_e enhancements)
  - Symbol rate, pattern length, symbol population
  - Voltage levels A/B/C/D (mean, stddev, P-P)
  - Eye diagram thresholds
  - Lower/middle/upper eye width and height TJ, RJ, DJ at BER-5 and BER-10
  - Level deviation and thickness, time deviation
  - Level 0/1/2/3 times, amplitude, and std dev
  - 48-edge rise and fall times.
- PAMJET Software runs on DPO70000SX scope





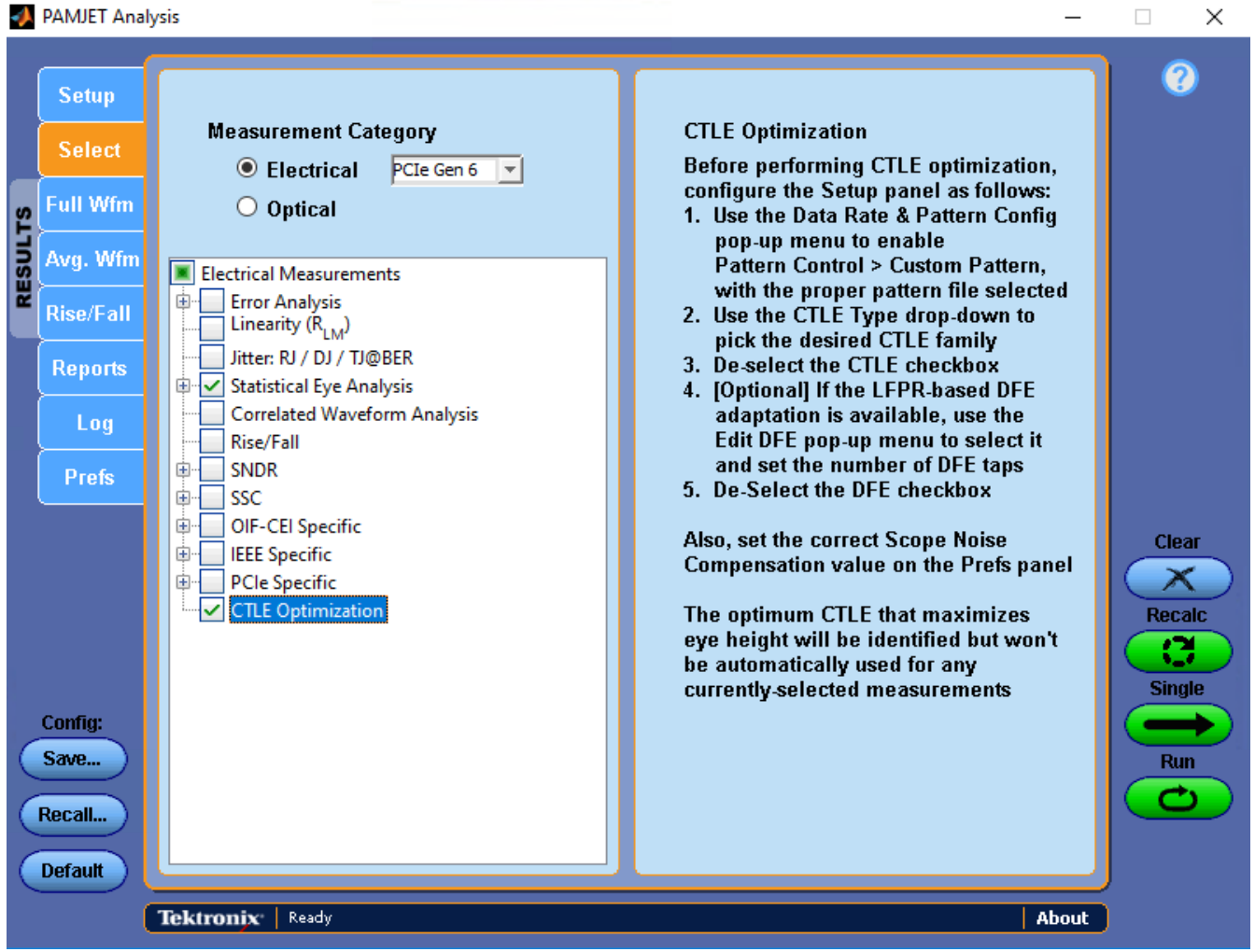
Scope Noise Compensation

- PAMJET includes application for scope noise characterization and compensation.
- User determines scope channel(s) for PCIe 6.0 waveform acquisitions.
- V/div settings and DC offsets are automatically swept to characterize scope noise across the ADC range.
- PAMJET reads noise database to interpolate noise values based on V/div settings and compensates noise effects during the waveform DSP analysis.
- Impact on noise from filters and embed/de-embed is automatically handled by PAMJET.



CTLE Optimization

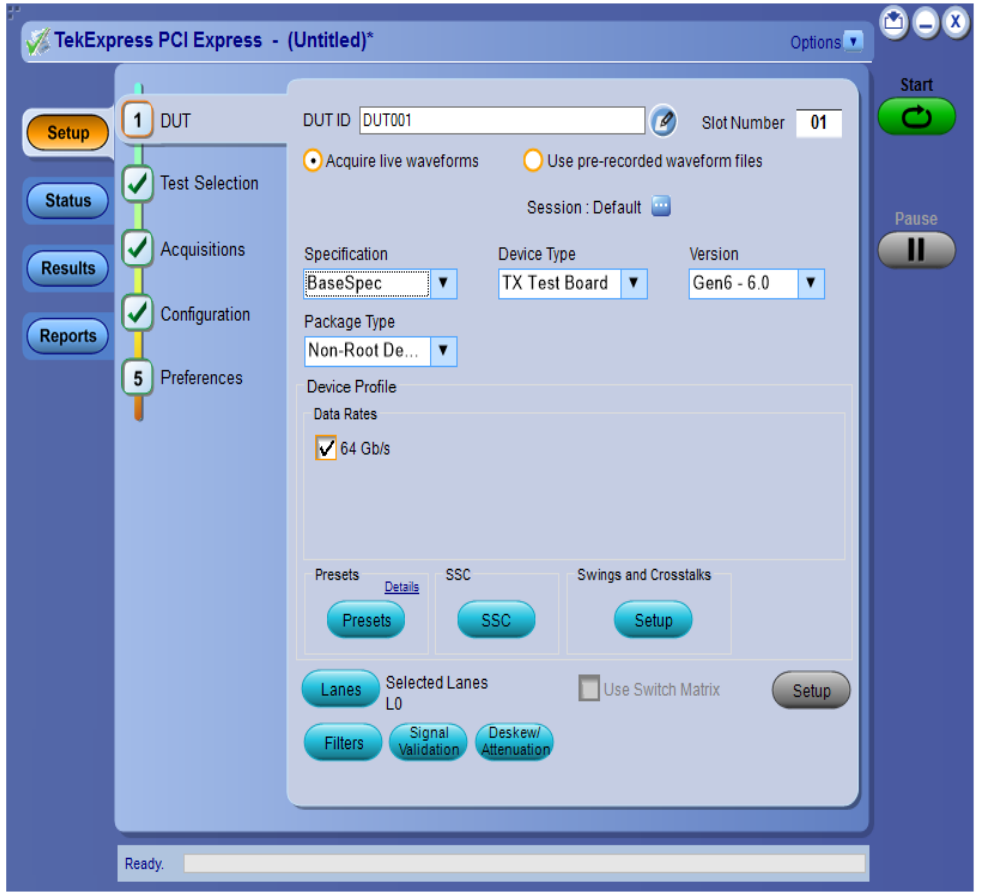
- PAMJET can optimize CTLE for PAM4 eye diagram (signal quality) measurements
  - CTLE optimized to maximize eye height @ BER
  - Not designed for jitter optimization
- PAMJET CTLE settings provided in “Select” tab as shown.
- Output of “CTLE Optimization” is optimal CTLE curve
- Optimal CTLE may then be applied to a PAM4 measurement



Tx – Automated Compliance Testing

Tek Express PCIe 6.0 Transmitter Test Software

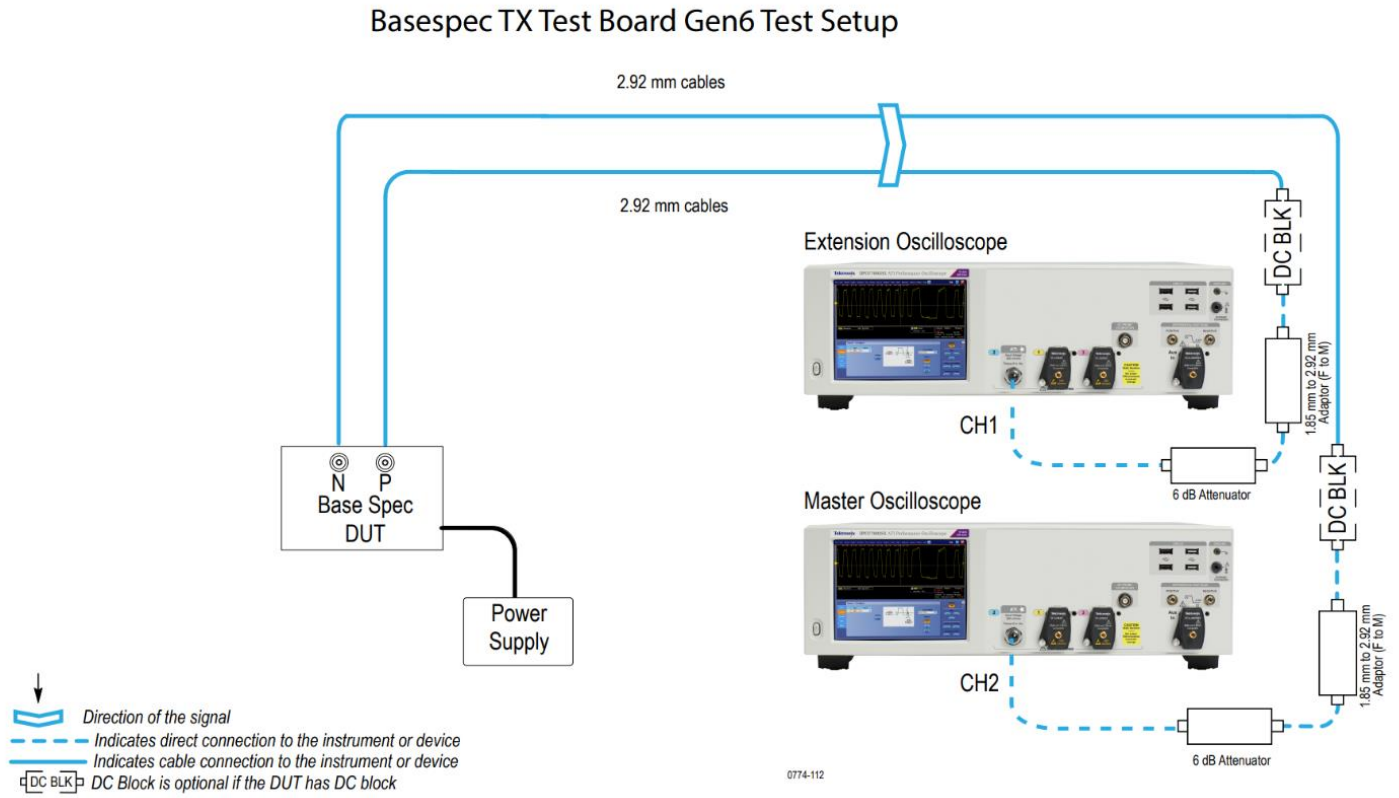
- Support Gen 6 Base/CEM spec.
  - Compliance Testing of Gen 6 CEM Add-In Card and System device types
  - Jitter, voltage, eye diagram and Preset Equalization tests via PAMJET/SigTest Library
  - Scope Noise characterization and compensation support
  - Automated CTLE optimization support
  - PAM4 4 level Eye Diagram support
  - Comprehensive programmatic interface for automation of tests
- Debug tools for analysis and experiments.



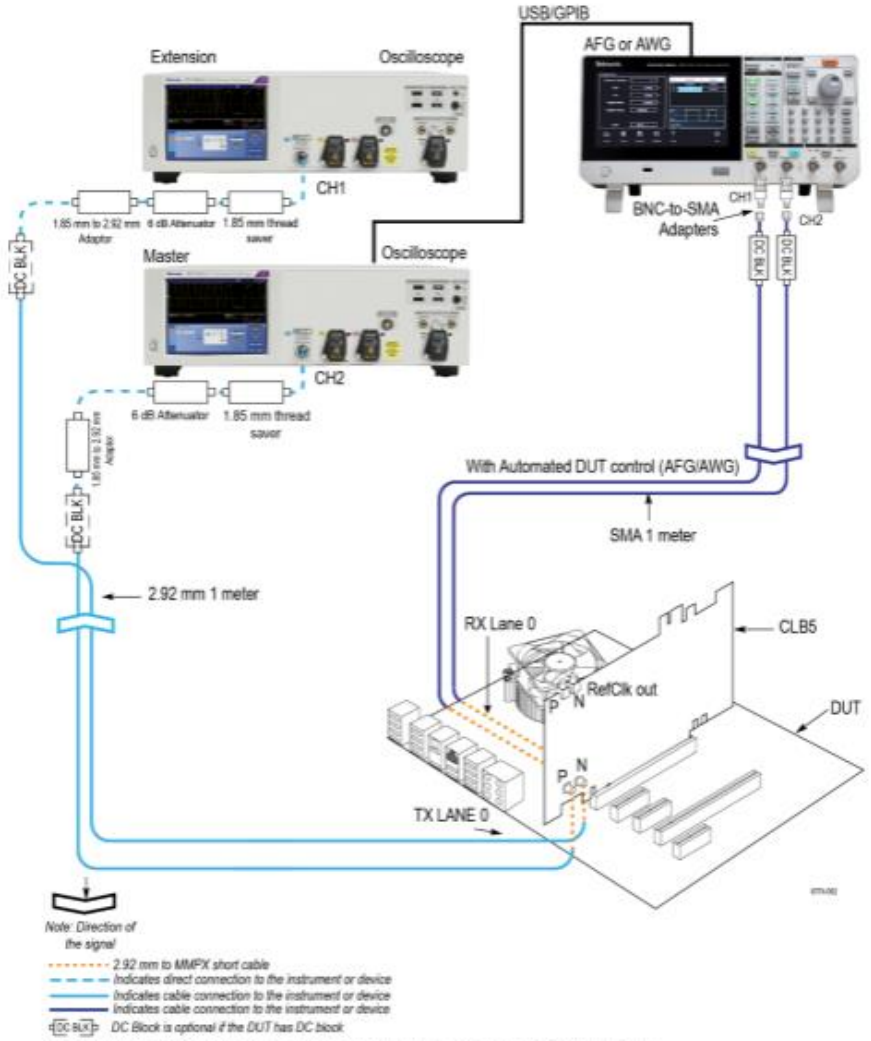
Transmitter - HW Requirements

- **Real Time Scope**
- ≥50GHz scope bandwidth, DPS75004SX real-time scope
- ≥ 128GS/s sample rate with 2x interpolation
- **Fixtures:**
- BASE – Low-loss break-outs from test board to scope inputs required. Option to de-embed cable/adapter effects.
- CEM - PCI-SIG 6.0 CEM fixture kit
- **Other:**
- Function generator and USB I/O dongle solutions for TX data rate / preset control.
- RF switch matrix may be added for multi-lane testing. Mini-circuits ZTM/ZTM2 style switch mainframes are recommended.

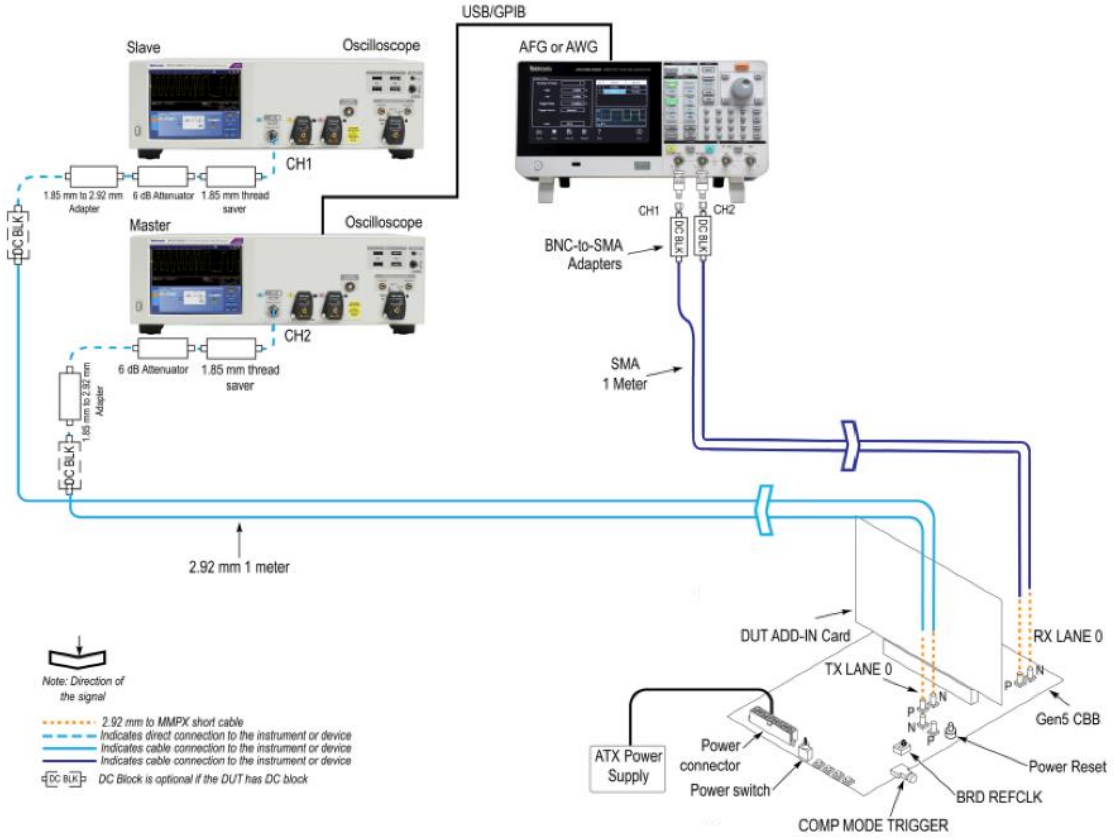
Gen 6 Base Tx - connection diagrams



Gen 6 CEM Tx wiring diagram – Sys and AIC



Note: All unused TX lanes of the fixture must be terminated using 50 Ω terminators.



These are Gen 5 connection diagrams. This can be similar to Gen6 as PCI-SIG Gen 6 is under FYI.

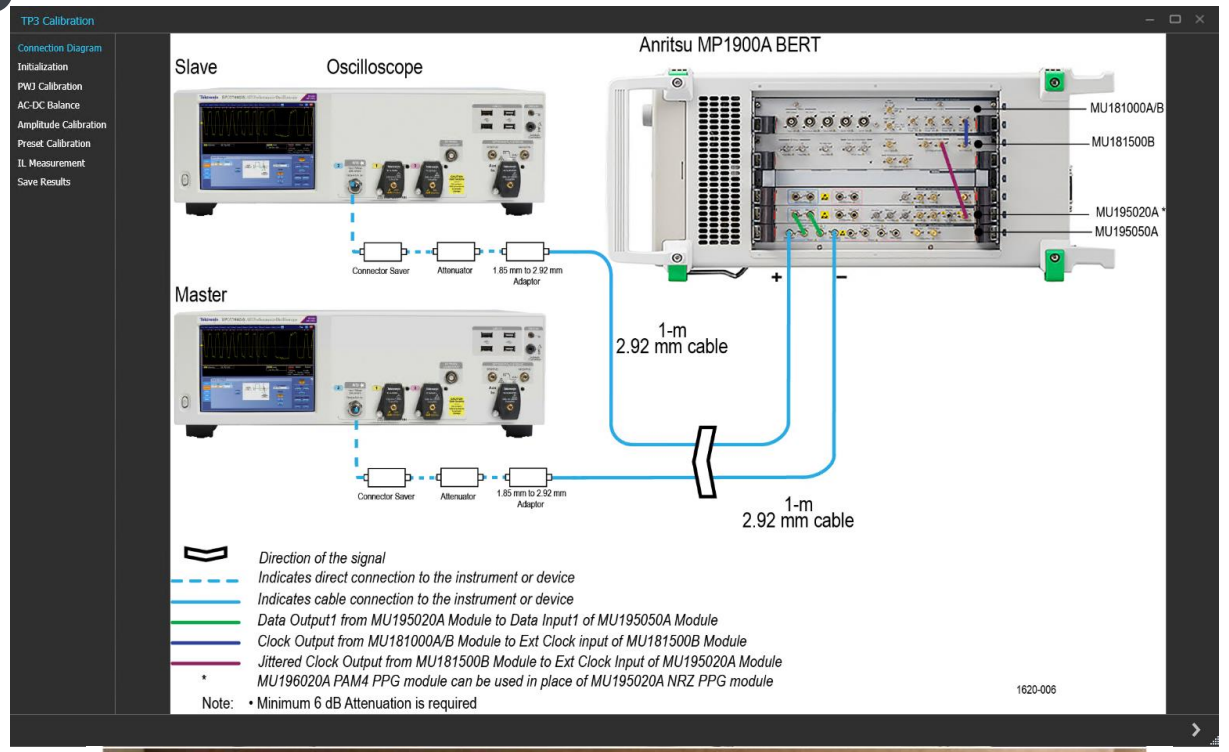
Rx – Automated Compliance Testing

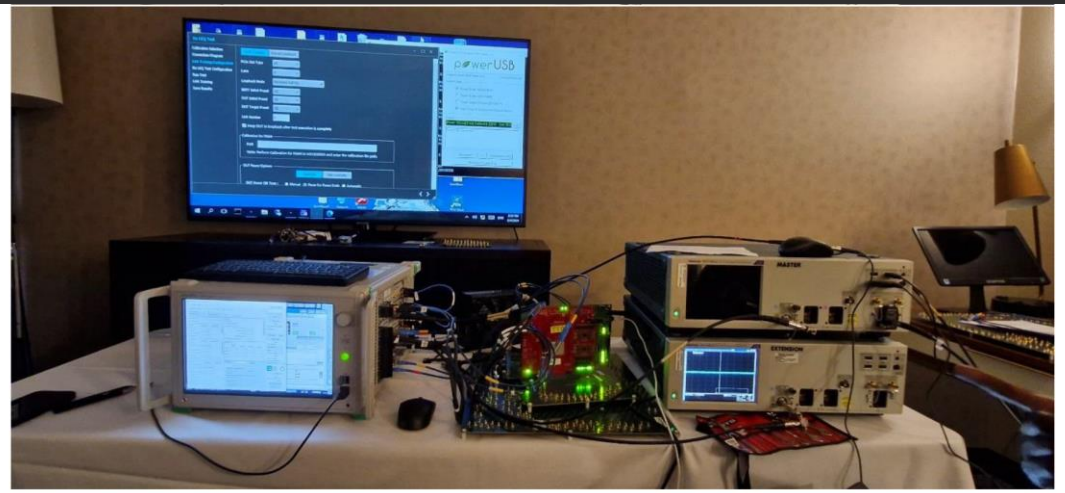
Receiver Test Software

- Supports Gen 6 BASE & CEM testing.
- GUI-based software runs on a host PC or Windows-enabled instrument.
- Gen 6 CEM solution in development to:
  - Connect and initialize scope and BERT
  - Enable user input to control BERT calibration parameters
  - Run TP3 & TP2 BERT calibration steps
  - Provide BERT calibration test reports
  - Run JTOL tests (pass/fail, margin), TX/RX Link EQ, and PLL loop BW tests and provide test reports

PCIe Gen6 Rx Software

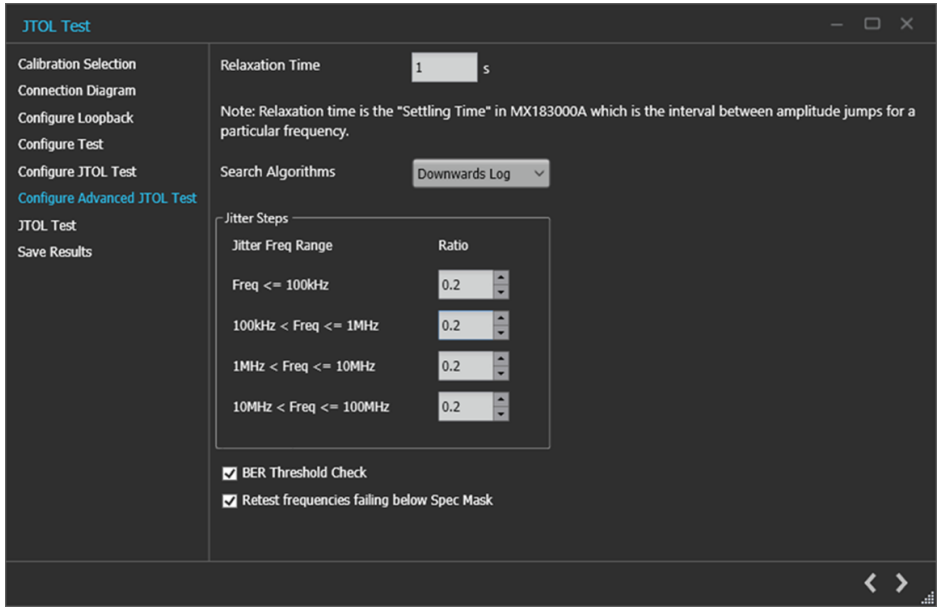
- Easy-to-use wizard interface
- Scope and BERT auto setup
- Base testing:
  - BERT calibration for TP3 and TP2
  - JTOL
- CEM testing:
  - BERT stress calibration using Seasim and SigTest
  - Tx LEQ
  - RX LEQ
  - JTOL
  - PLL Bandwidth
- Software runs from any host PC, instrument connection via Ethernet / LAN
- Built-in patterns, setups, and sample calibration results.
- Peripheral automation controls available for customed workflow





RX Test Improvements

- ***BER Threshold check:*** performs BER check before initiating Jitter Tolerance tests. BER verified at lowest SJ amplitude to ensure it meets threshold requirements set by user at Configure Test pane. If threshold is not met, user is given choice to continue the test, re-train PHY, or cancel test. This ensures PHY is in correct state before performing JTOL test.



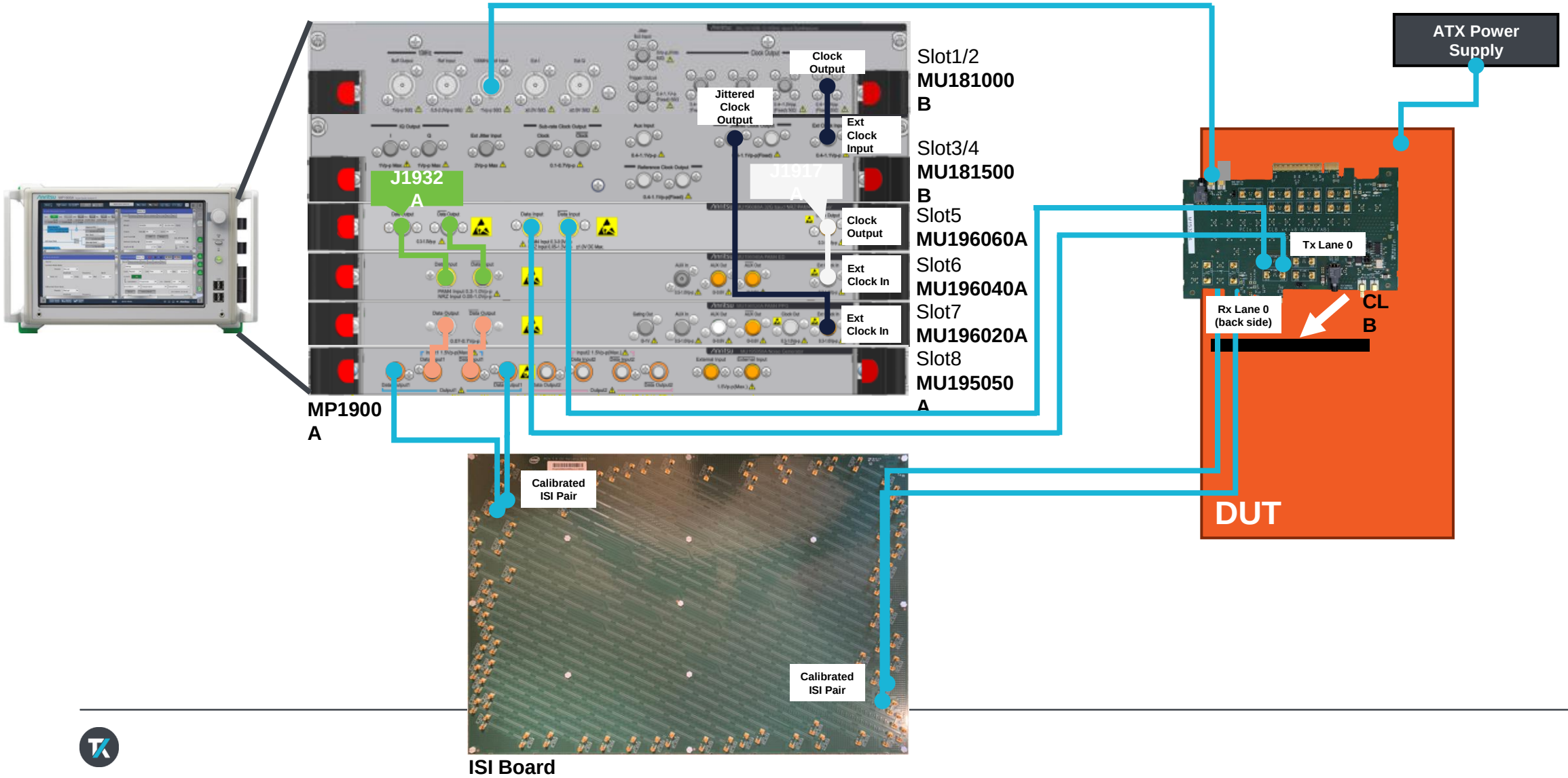
- ***SJ Frequency Re-test:*** If a user-configured SJ tone RX BER test result fails below spec limit, RX software will display a pop-up window “Failure below Spec mask”. User may **PROCEED** (record BER test result and move to next SJ frequency), RETEST (re-run RX test), or **AUTOSEARCH** and **RETEST** (re-configure BERT settings and re-test RX test).

Receiver - HW Requirements

- **Instruments**
- ≥50GHz scope bandwidth, DPS75004SX real-time scope
- Anritsu MP1900A BERT configured for PAM4 testing.
- **Fixtures:**
- BASE: low-loss break-out connectors from test board to scope inputs required. Option to de-embed cable/adapter effects.
- CEM: PCI-SIG 6.0 CEM fixture kit

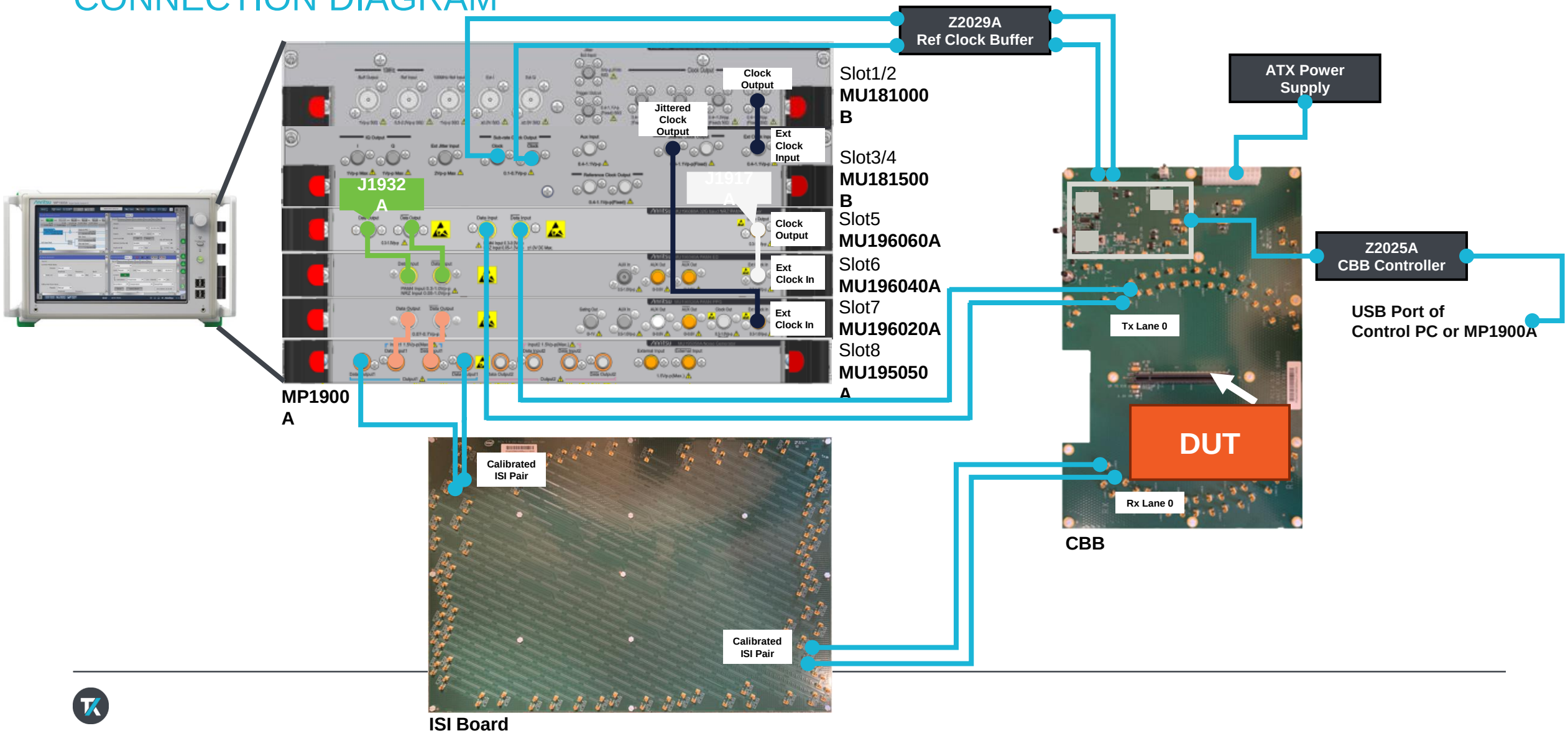
HW Requirements – PCIe 6 Rx (System)

CONNECTION DIAGRAM



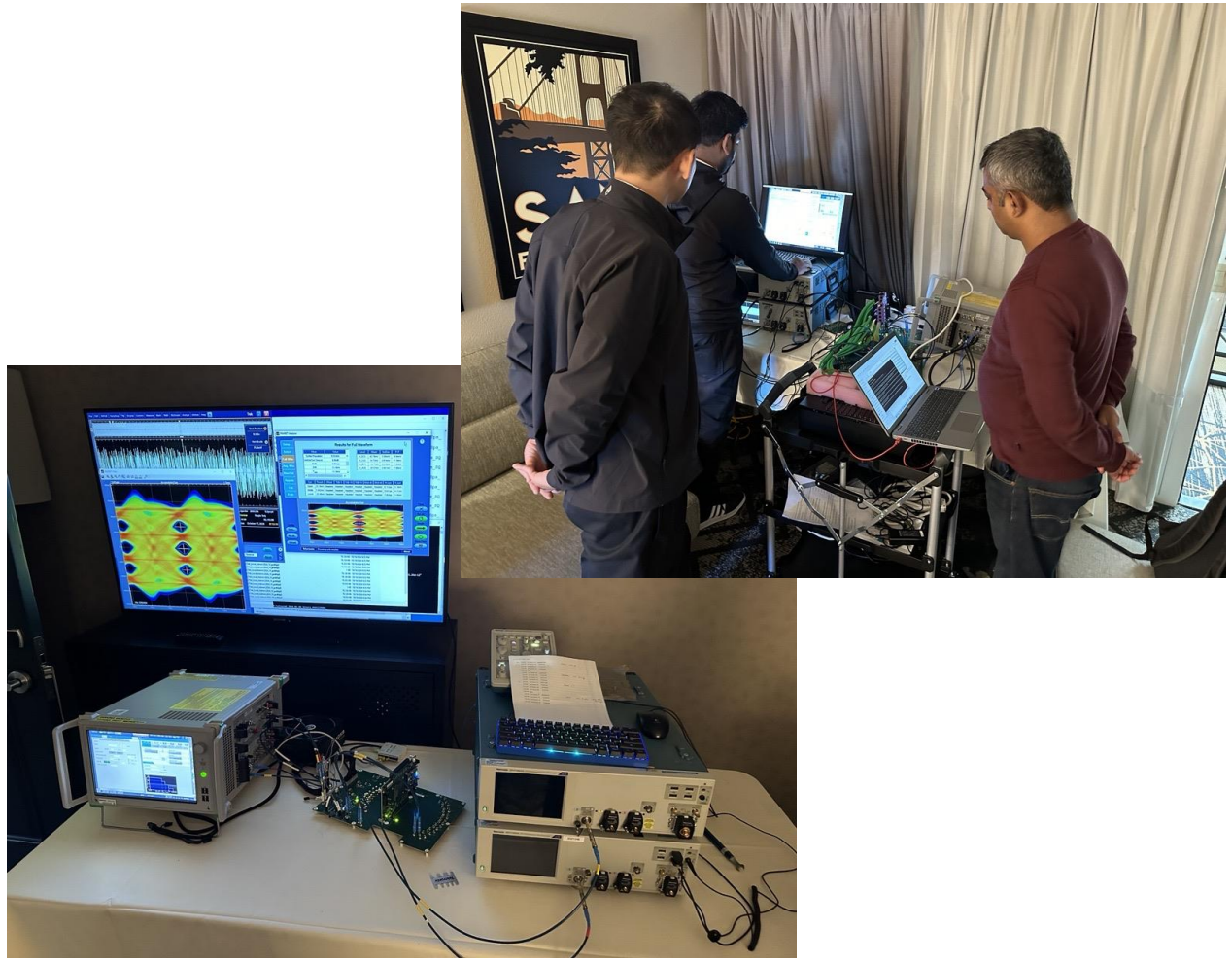
HW Requirements – PCIe 6 Rx (Add-in Card)

CONNECTION DIAGRAM



PCIe 6.X Preliminary FYI Workshop Update

- **Last Pre-FYI event: October 2024**
  - Supported Tx/PLL/Ref-clk/Rx JTOL and Tx/Rx LEQ suites covering all physical layer tests for CEM form factor.
  - Tx: Tests including Signal Quality test, Preset, Jitter, RLM & SNDR. In addition, PLL Loop Bandwidth and System Ref-clk tests.
  - Rx: Automated TP3 and TP2 BERT stress calibration, Tx & Rx LEQ tests, and Rx JTOL tests with Anritsu MP1900A.
  - Tx & Rx correlation studies planned for test equipment, test configuration, and analysis tool in PCI-SIG work group
- **Next Pre-FYI event: March 24-28, 2025**

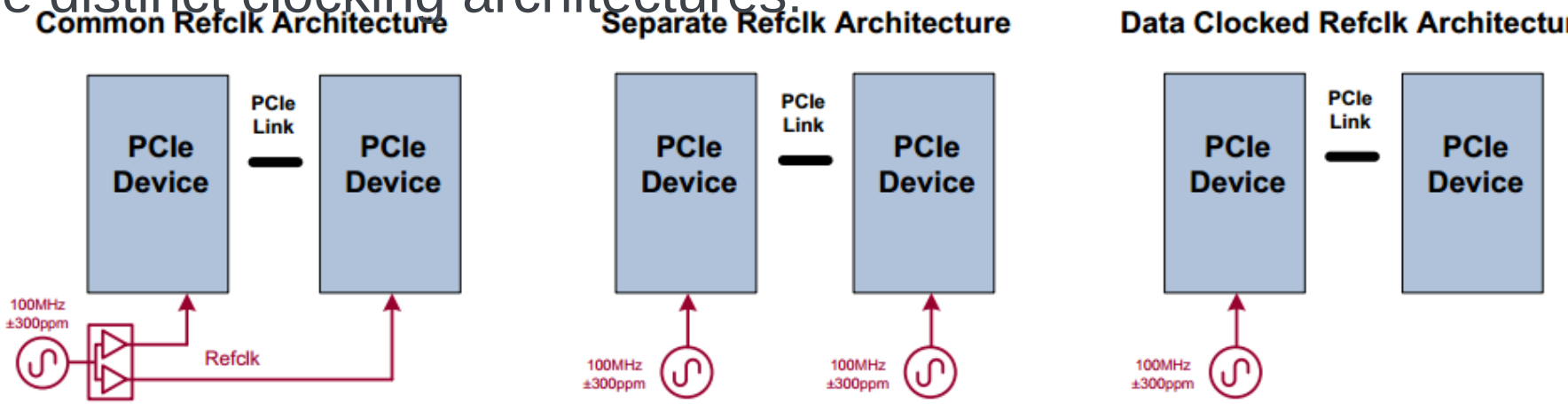


PCIe Gen6 Pre-FYI event - Oct 2024

Ref Clock Testing

PCIe RefClk Architectures

- PCIe standard specifies a 100 MHz clock (Refclk) with greater than ±300 ppm frequency stability at both the transmitting and receiving devices and support for three distinct clocking architectures:



  - **Common** – most popular, supports SSC; same clock must be connected to all devices while maintaining skew <= 12 ns between devices
  - **Separate/independent** – used for cabled applications; SSC not historically used prior to Gen4; now becoming increasingly used via SRIS
  - **Data Clocked** – simplest to implement, but not very common

100MHz Ref-clk Tests

- Verify jitter (HF RMS, LF RMS, Pk-Pk phase, cycle-cycle, Gen1/2/3/4/5) and signal quality AC specifications (rise/fall time, high/low, period accuracy, duty cycle).
- Clk termination requirements must be provided by the platform or probing solution.
- De-embed of scope noise supported via SkyWorks tool and Intel Clock Jitter Tool (CJT).
- 5GHz real-time scope recommended for refclk tests.
- Tektronix will continue alignment with refclk methodologies and provide a solution for Gen6.

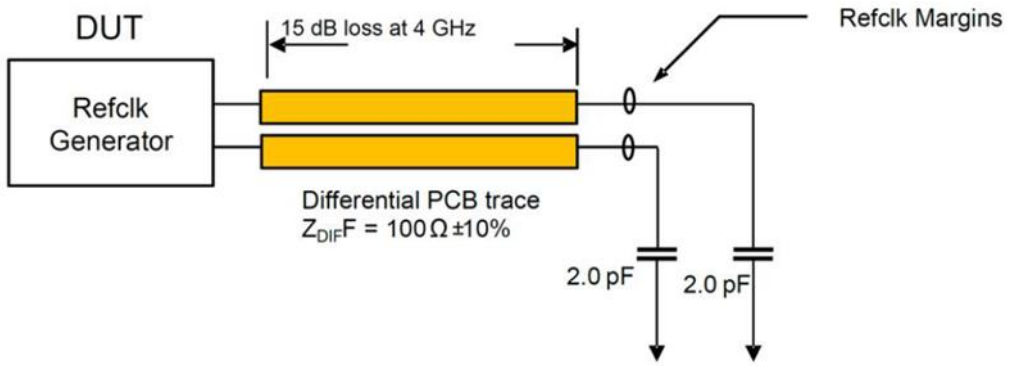
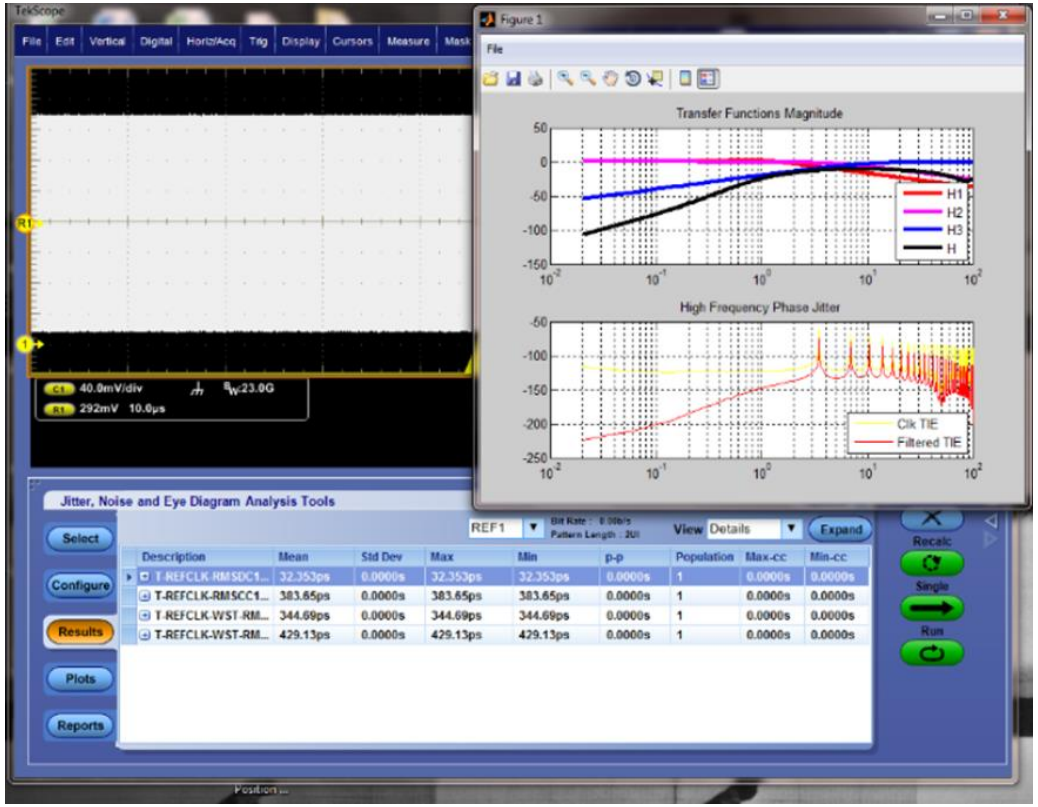


Figure 8-64 Oscilloscope Refclk Test Setup For All Cases Except Jitter at 32.0 GT/s

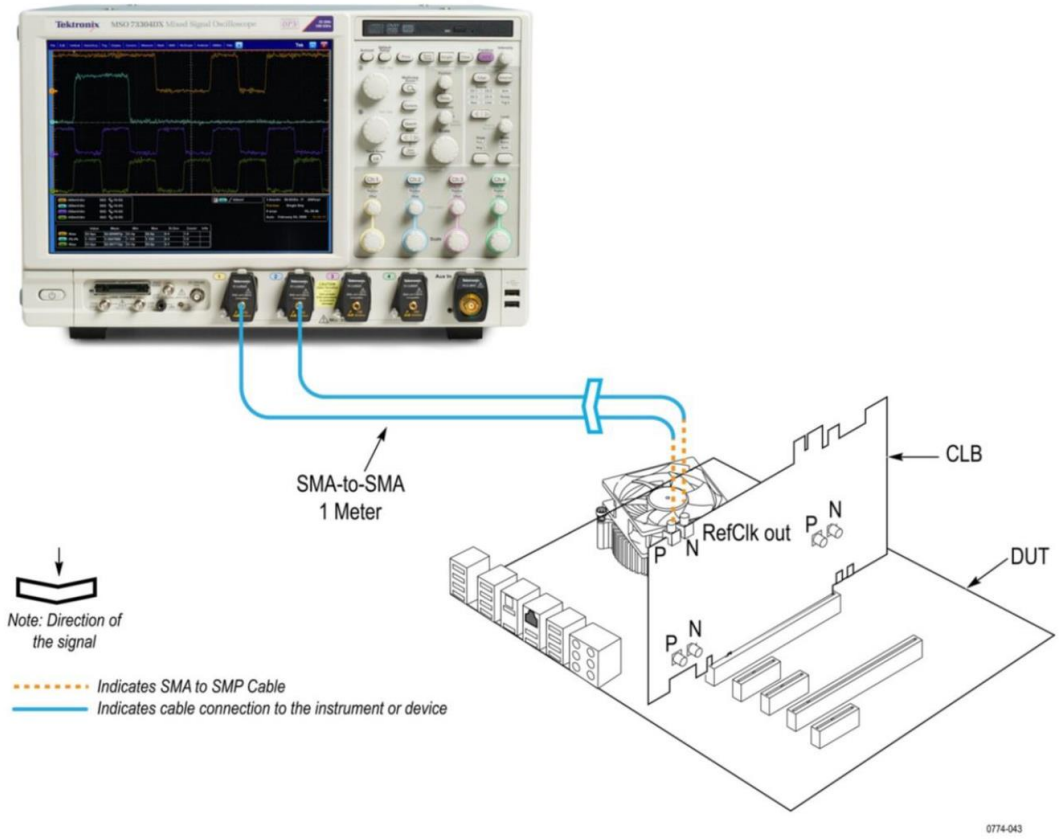


RefClock - HW Requirements

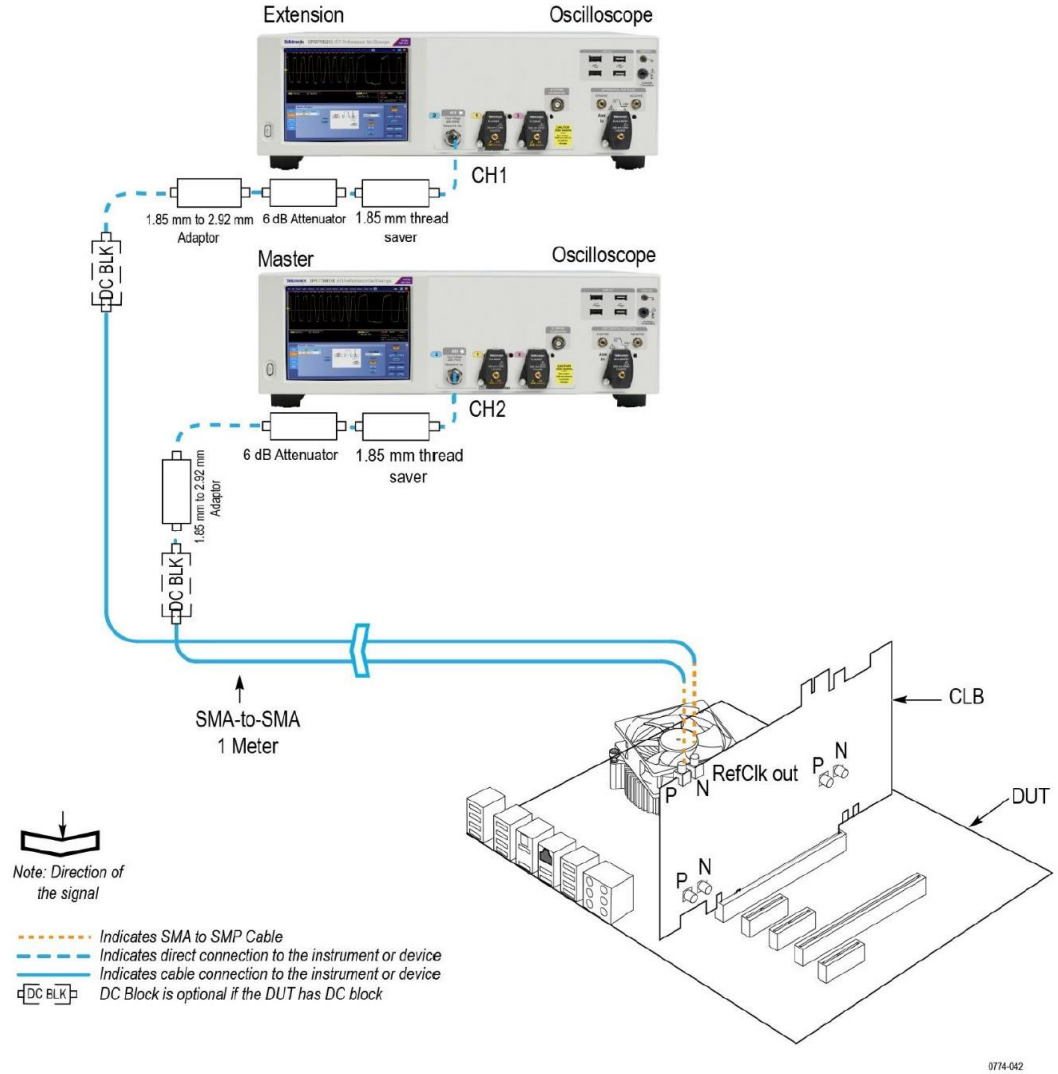
- **Real Time Scope**
  - Min BW 5GHz
    - DPS75004SX – Dual Stack 50GHz SX scope
    - DPO75002SX
    - MSO64B
- **Test Fixtures**
  - PCI-SIG CLB Fixture
- **PC/Laptop (Option)**
  - Windows 10/11 OS to install Intel or Skyworks Clock Jitter Tool

Ref-Clock Connection Diagram

Ref-Clock Test Setup- Non-ATI mode



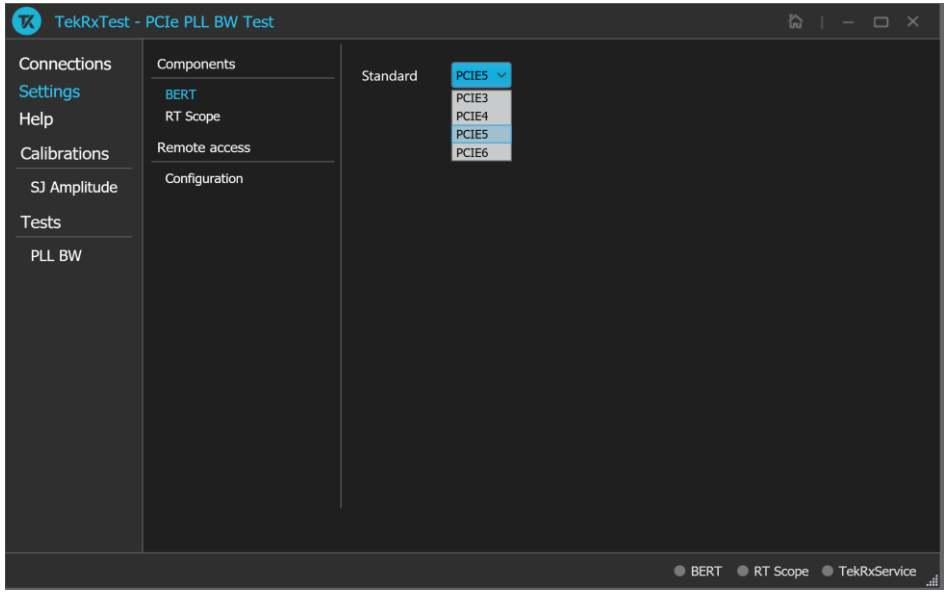
Ref-Clock Test Setup- ATI mode

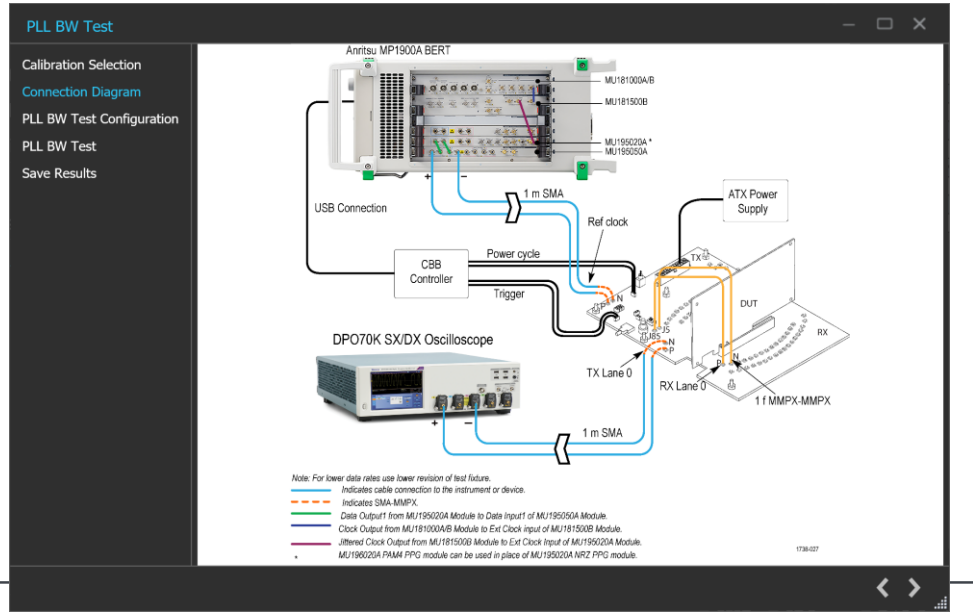


PLL Bandwidth Testing

PLL Bandwidth Test

- The Phase Locked Loop (PLL) application tests the Device Under Test (DUT) to ensure it can tolerate clock variations with injected sinusoidal jitter (SJ) to meet the specified limits.
- It offers multiple frequencies to calibrate for a defined SJ amplitude at a 100MHz clock.
- The BERT generates a signal with SJ amplitude injected into the 100MHz reference clock, allowing the DUT to be tested for device to get the peaking, bandwidth, and PLL response.
- The test verifies that the Add-in-card PLL bandwidth and peaking are within the limits allow by the PCI Express specifications.
- Current solution supports Clock patterns. Under development for Q0-Q9.



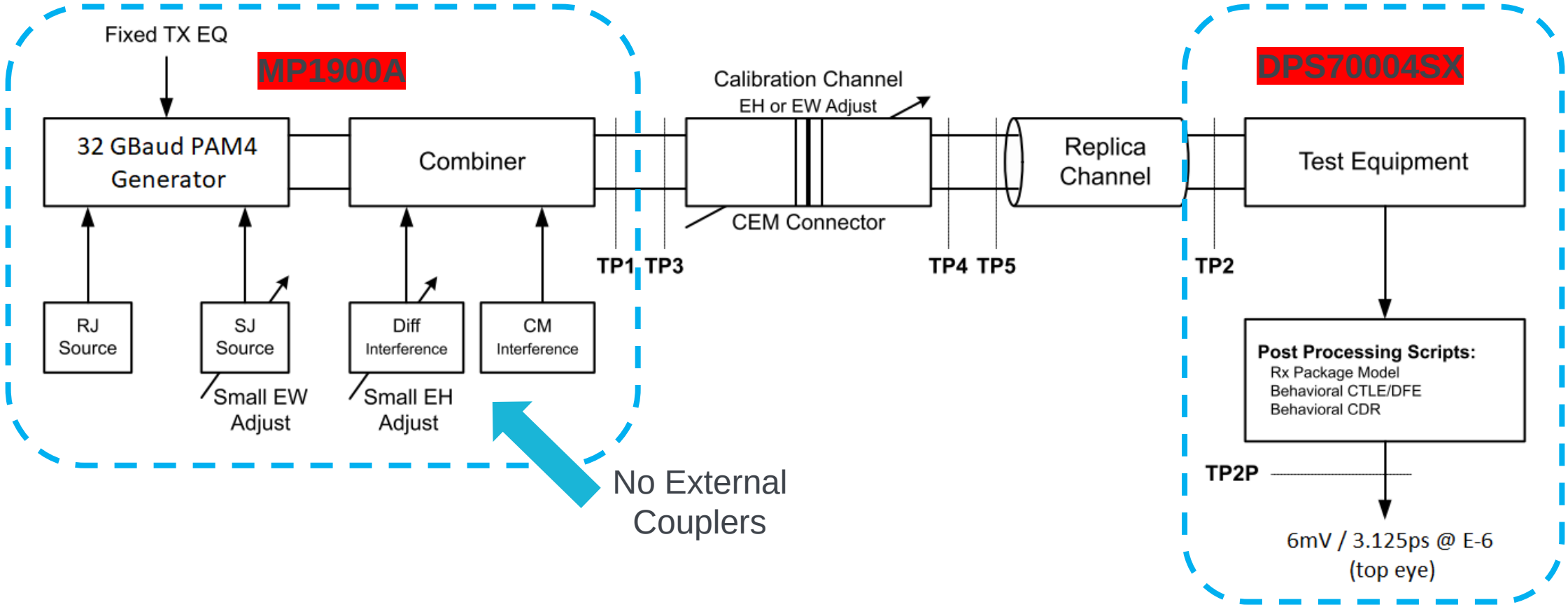


PLL Bandwidth - HW Requirements

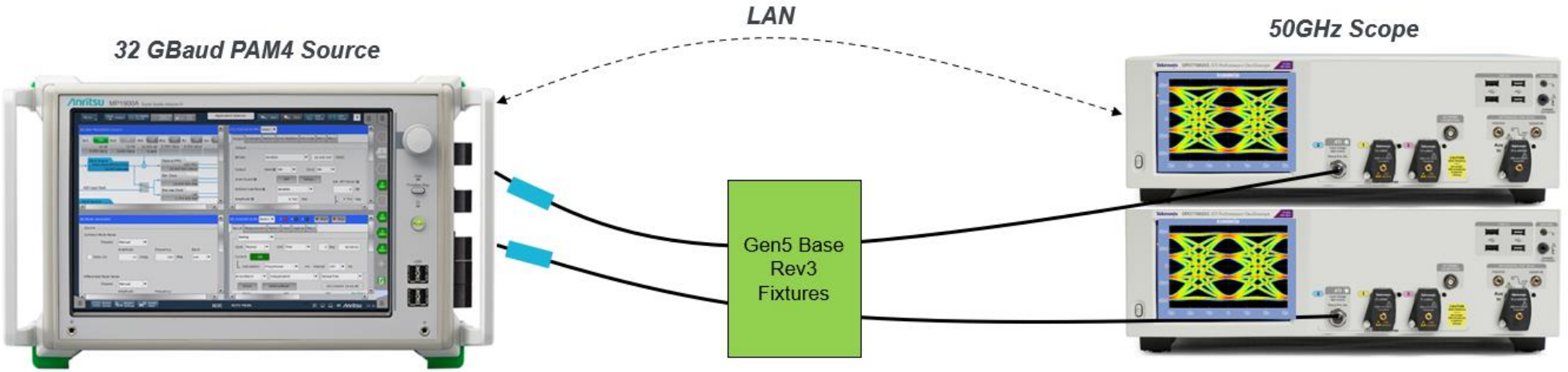
- **Real Time Scope**
  - Min BW 50GHz- DPS75004SX – Dual Stack 50GHz SX scope
  - Sample Rate ≥ 128GS/s with a max of 2x interpolation
- **BERT**
  - Anritsu MP1900A
- **Test Fixtures**
  - BASE
    - NA
  - CEM
    - PCI-SIG 6.0 CEM Fixture Kit

PCIe Gen6 Testing Summary

Multi-level Gen6 Stressed Eye Diagram



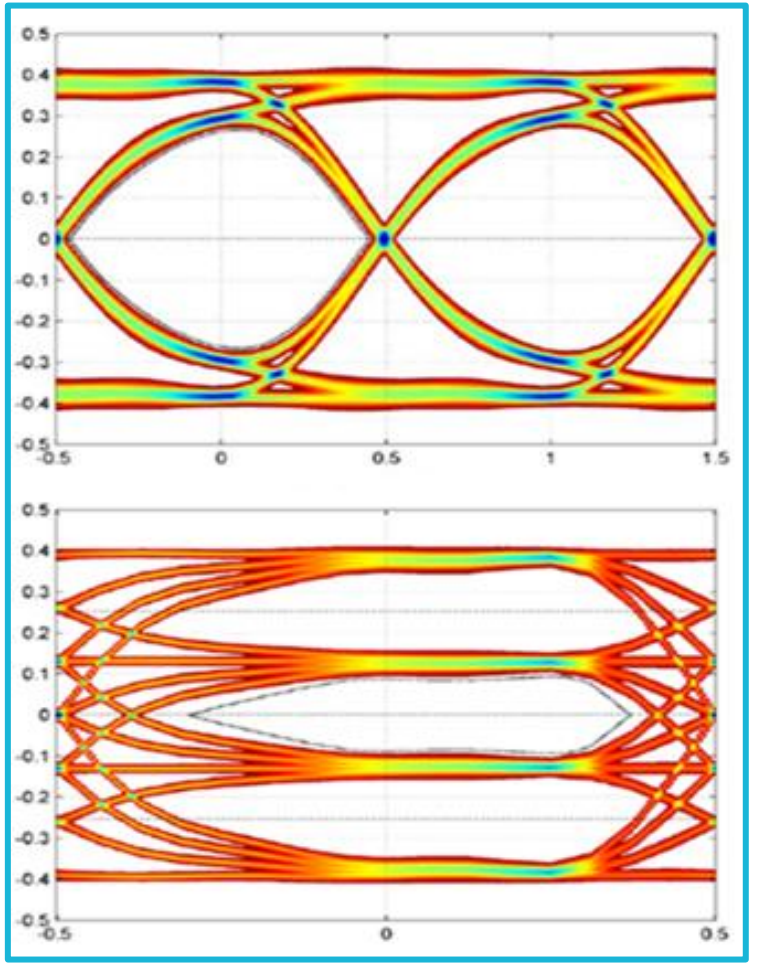
PAM4 Stressed Eye Feasibility Study



- **Source:** PAM4 PPG (Anritsu MP1900A)
  - 64 GT/s (32 GBaud PAM4) – Step Response
  - Tx EQ Pre Cursor 1 & 2 optimized
- **Channel:** 33.1dB @ 16GHz
  - Gen5 Base Rx Fixtures
- **Scope:** Tektronix Real Time (DPO75004SX)
  - 50 GHz with 200 GS/s
  - Root Complex package embedded
- **Post Processing:** Seasim 1.0.6
  - CTLE/DFE
  - Sj, Rj, & Crosstalk (DMI)

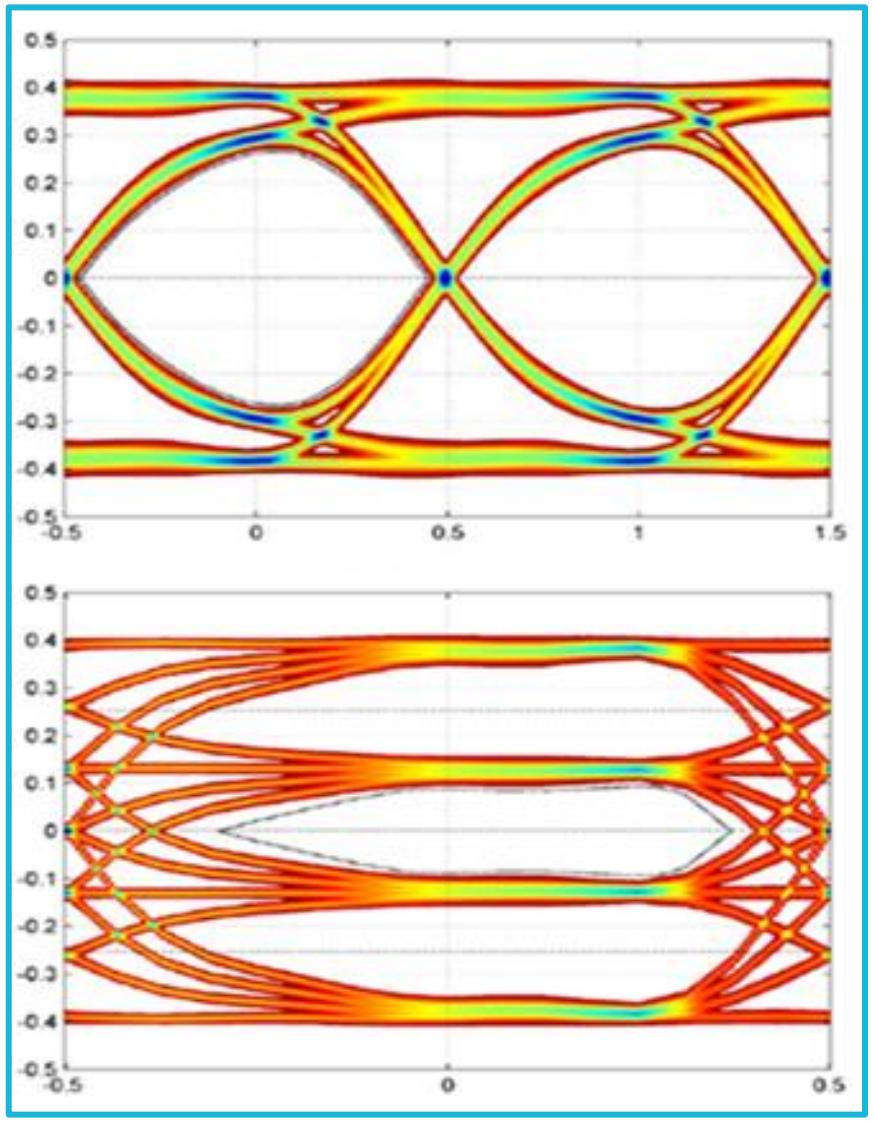
Tx and Rx Test Challenges at 64 GT/s PAM4

Repeatable stressed eye calibration for PAM4 signaling	Validation & compliance across 6 data rates for legacy NRZ & new PAM4 signaling	Noise from measurement equipment must be accurately characterized and removed
JTOL and BER Rx testing in the presence of SSC	Updating post-processing tools to support 64 GT/s	Back-channel equalization challenges with PAM4 signals with ~ 28dB insertion loss
PCI-SIG compliance tool (**SigTest**) does not support PAM4 analysis	Measurement sensitivity to instrumentation **noise**	New Tx Equalizer tap and method



Receiver Challenges at 64 GT/s PAM4

- Repeatable stressed eye calibration for PAM4 signaling
- Validation & compliance across 6 data rates for legacy NRZ & new PAM4 signaling
- Noise from measurement equipment must be accurately characterized and removed
- JTOL and BER Rx testing in the presence of SSC
- Updating post-processing tools to support 64 GT/s
- Back-channel equalization challenges with PAM4 signals with ~ 28dB insertion loss



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Q&A

THANK YOU