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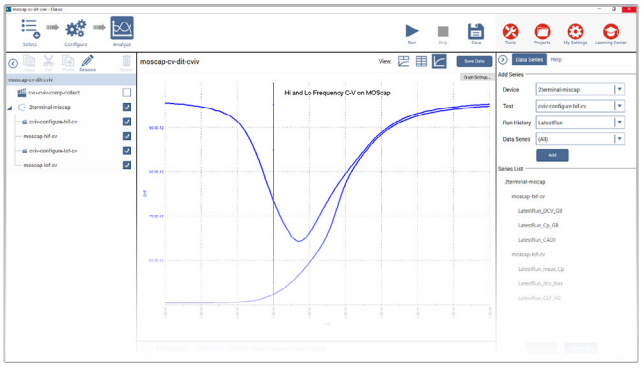
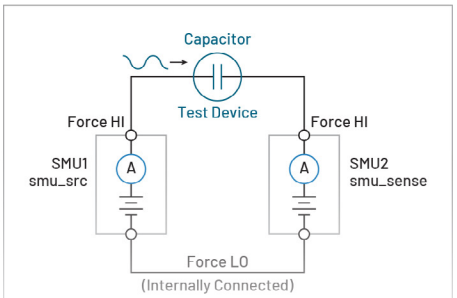
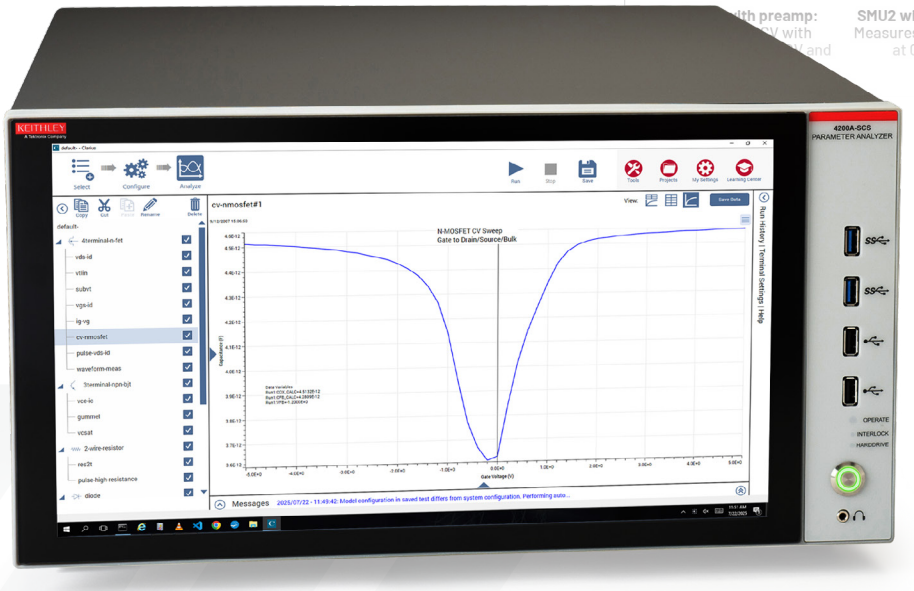
C-V Testing for Components and Semiconductor Devices

APPLICATIONS GUIDE







C-V Testing for Components and Semiconductor Devices

Capacitance-Voltage (C-V) testing is widely used to determine a variety of semiconductor parameters, such as doping concentration and profiles, carrier lifetime, oxide thickness, interface trap density, and more. This C-V testing applications guide features a collection of application notes focused on C-V testing methods and techniques using the 4200A-SCS Parameter Analyzer. The 4200A-SCS provides three C-V methods: Multi-frequency C-V (1 kHz – 10 MHz), Very Low Frequency C-V (10 mHz – 10 Hz,) and Quasi-static C-V measurements.

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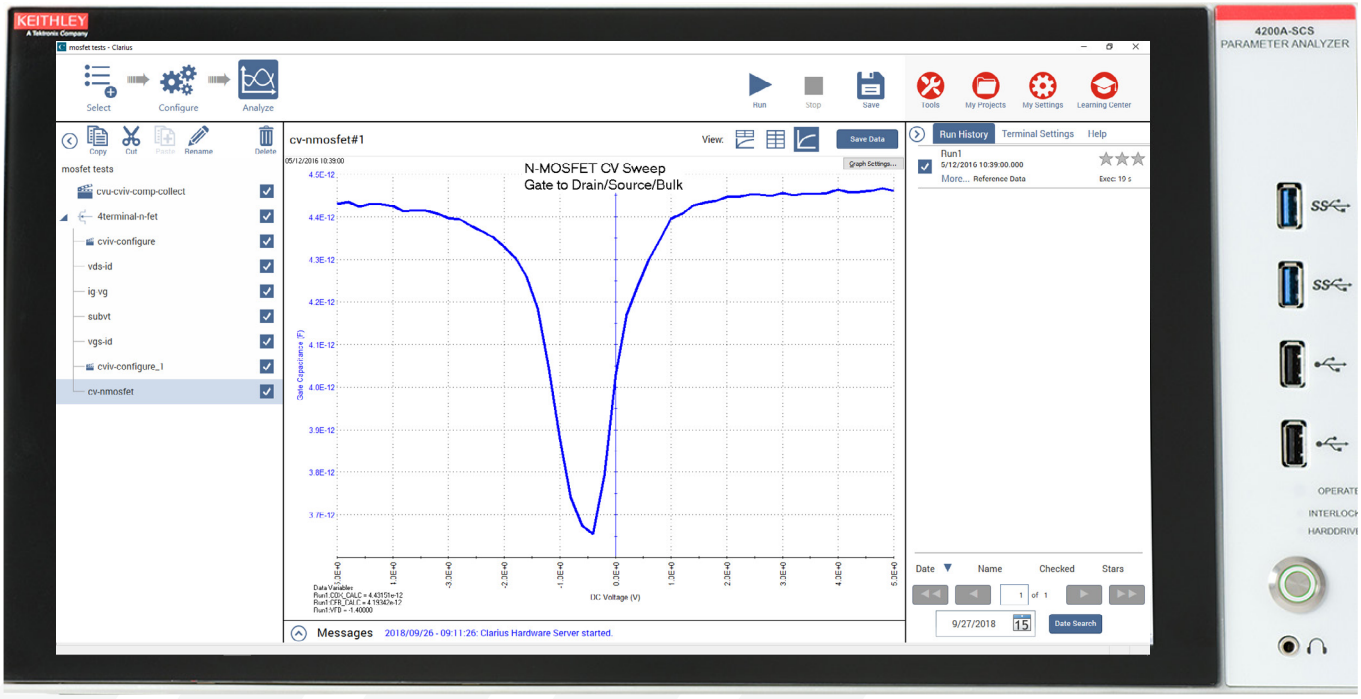
Making Optimal Capacitance and AC Impedance Measurements with the 4200A-SCS Parameter Analyzer



Introduction

Capacitance-voltage (C-V) and AC impedance measurements are commonly performed on many types of devices for a wide variety of applications. For example, C-V measurements are used to determine these device parameters:

- Gate oxide capacitance of MOSCAPs
- MOSFET input and output capacitance
- Built-in potential of solar cell
- Majority carrier concentration of a diode
- Capacitance between terminals of a BJT
- Oxide thickness, doping density, and threshold voltage from a MIS capacitor

Both the 4215-CVU and 4210-CVU are multi-frequency (1 kHz to 10 MHz) AC impedance measurement modules for the 4200A-SCS Parameter Analyzer (see **Figure 1**) that enables the user to make C-V measurements easily.The differences between the two CVUs are the number of test frequencies and the AC drive voltage. The 4215-CVU has 10,000 discreet frequencies with 1 kHz resolution and the 4210-CVU has 37 discreet frequencies. The AC drive voltage range of the 4215-CVU is 10 mV to 1 V rms and the range of the 4210-CVU is 10 mV to 100 mV rms.

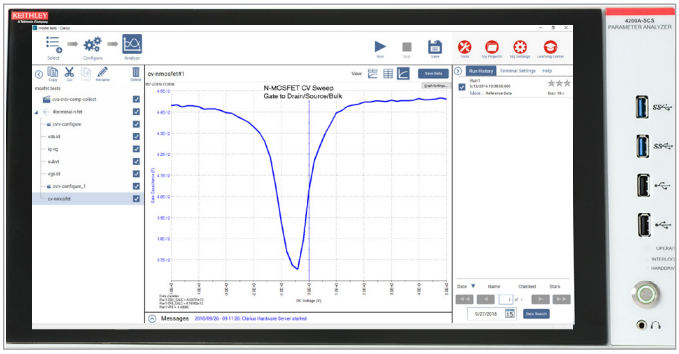


Figure 1. 4200A-SCS Parameter Analyzer

The CVUs are designed with unique circuitry and are controlled by the Clarius software to support features and diagnostic tools that ensure the most accurate results. Some of the CVU's built-in tools include real-time measurement mode, open/short compensation, parameter extraction formulator, filtering, timing controls, and the ability to switch the AC ammeter terminal in the software.

These tools, along with using proper cabling and C-V measurement techniques, allow the user to make highly sensitive capacitance measurements.

This application note describes how to make optimal capacitance measurements using proper measurement techniques and the CVU Capacitance Voltage Unit.

CVU Measurement Overview

Figure 2 shows a simplified model of the 4210-CVU and 4215-CVU. The capacitance of a device is determined by sourcing an AC voltage and measuring AC current and phase while a DC voltage is applied or swept across the device.

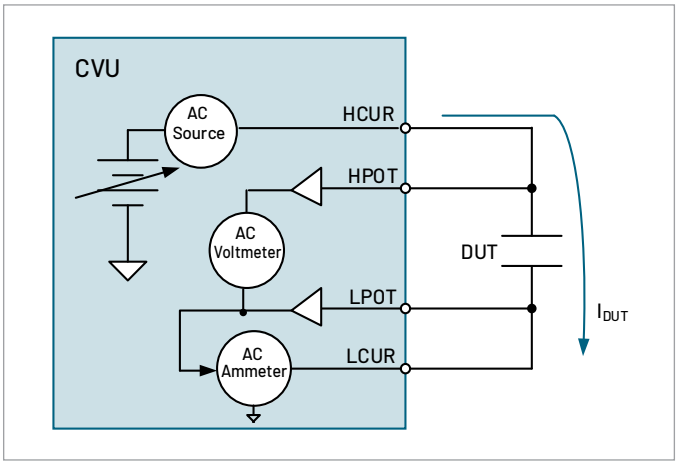


Figure 2. Simplified CVU diagram

The time domain AC values are processed into the frequency domain to produce the phasor form of the impedance. The device capacitance is calculated from the AC impedance and the test frequency using this equation:

$$C_{DUT} = \frac{I_{DUT}}{2\pi f V_{ac}}$$

The CVU measures capacitance using the auto-balance bridge (ABB) method. The ABB is used to nullify an AC signal of known frequency on one terminal (LPOT if the AC ammeter is on LCUR) of a DUT to guard out stray impedances. This AC ground keeps the LPOT terminal of the CVU at 0 VAC, so that all the AC current in the test circuit flows to the AC ammeter and not through any parallel capacitances in the test circuit.

Depending on the test settings, which include the frequency, AC drive voltage, and current range, the CVU can measure capacitances in the sub-picofarad to millifarad ranges. The user-specified test frequency depends on the device being tested and the parameters being derived. The range of test frequencies is from 1 kHz to 10 MHz. The DC bias function is ±30 V (60 V differential).

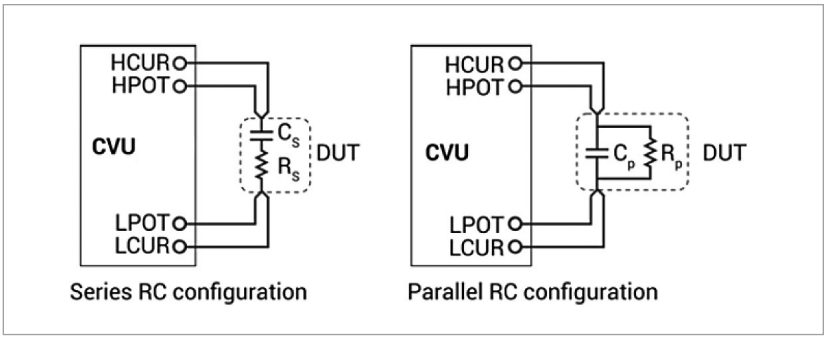


Figure 3. Simplified measurement models

Measurement Models and Parameters

Typical models of a measurement DUT are usually a series or parallel resistance-capacitance (RC) circuit. As shown in the simplified models in **Figure 3**, the CVU can measure the DUT as a series configuration (R_SC_S) or as a parallel configuration (R_PC_P).

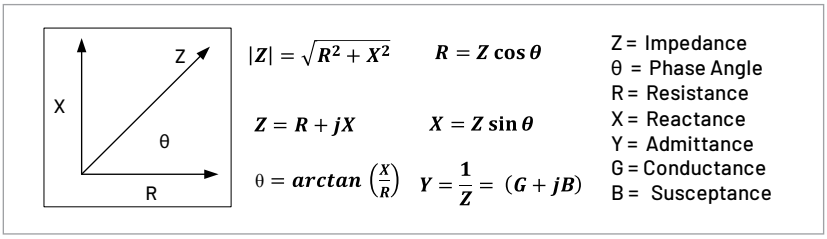


Figure 4. Vector Diagram for Impedance

The CVU can measure and display these parameters:

- Impedance and phase angle (Z, Theta)
- Resistance and reactance (R+jX)
- Parallel capacitance and conductance (C_P–G_P)
- Series capacitance and resistance (C_S–R_S)
- Parallel capacitance and dissipation factor (C_P–D)
- Series capacitance and dissipation factor (C_S–D)
- Admittance and phase angle (Y, theta)

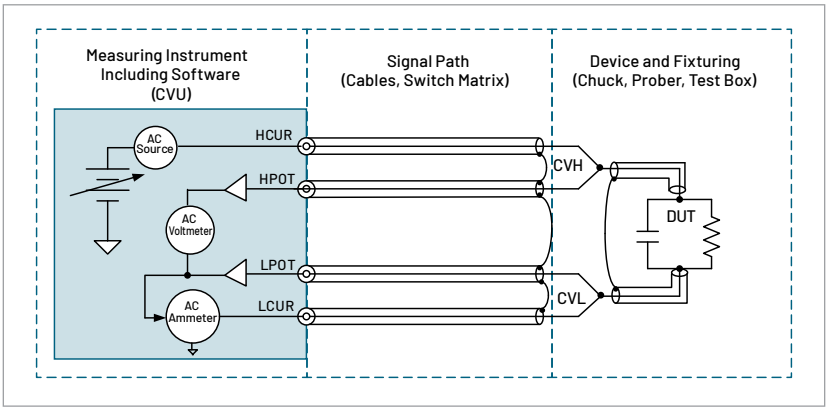


Figure 5. C-V measurement system

By using the built-in Formulator tool in Clarius, other parameters such as inductance can be easily extracted from the measured data. The vector diagram for Impedance in **Figure 4** shows the fundamental equations for impedance.

AC Impedance Measurement System

A C-V measurement system, as shown in **Figure 5**, can be quite complicated because the configuration includes the measuring instrument and software, the cabling of the signal path, test fixturing, and the device. To make optimal measurements, the test settings and timing parameters of the CVU need to be set appropriately. Proper cabling, probers, and test fixtures must be used, and then connection compensation must be performed. Finally, the device itself

can cause problem measurements. The next few sections will discuss hardware and software considerations for making good capacitance measurements.

Cabling and Connections

This section describes using the proper cabling and connections, AC guarding of the chuck and device terminals, and configuring the AC ammeter terminal.

Proper Cabling

For the best measurement results, use only the supplied red SMA cables for making connections to the CVU. The following accessories are supplied:

(4) CA-447A SMA to SMA 1.5 m cables (red)

(4) CS-1247 SMA to BNC Adaptors

(2) CS-701A BNC Tees

(1) Torque wrench to tighten SMA cable connections

The supplied accessories allow connecting to a test fixture or prober with BNC or SMA connections. The CVU, as well as the supplied accessories configured for two-wire sensing, are shown in **Figure 6**. A CS-1247 SMA-to-BNC Adaptor is connected to each CA-447A SMA-to-SMA Cable. HCUR and HPOT terminals are connected by a CS-701A BNC tee to form CVH, and LCUR and LPOT are connected together to form CVL. Using the supplied torque wrench, tighten the SMA cable connections to ensure good contacts. The red SMA cables are 100 Ω. Two 100 Ω cables in parallel are 50 Ω, which is standard for high frequency sourcing and measuring applications.

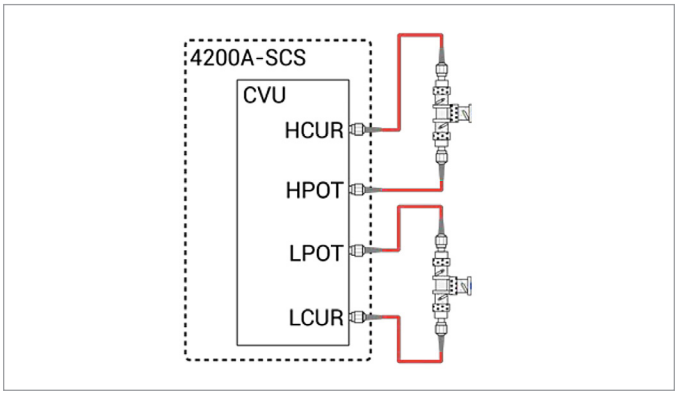


Figure 6. CVU connections for two-wire sensing

An example of four-wire sensing to the DUT is shown in **Figure 7**. In this case, the HCUR and HPOT terminals are connected to one end of the device, and the LPOT and LCUR terminals are connected to the other end of the device. To improve the bandwidth, connect the outside shields of the coax cables to the metal test fixture. Use four-wire connections to the device to facilitate sensitive measurements by sensing the voltage as close as possible to the device. The outside shields of each of the four coax cables must be connected as close as possible to the device to minimize the loop area of the shields. The outside shields of the coax cables also get connected to the metal test fixture to reduce noise and coupling from external sources. This reduces the inductance and helps to avoid resonance effects, which can be burdensome at frequencies higher than 1 MHz.

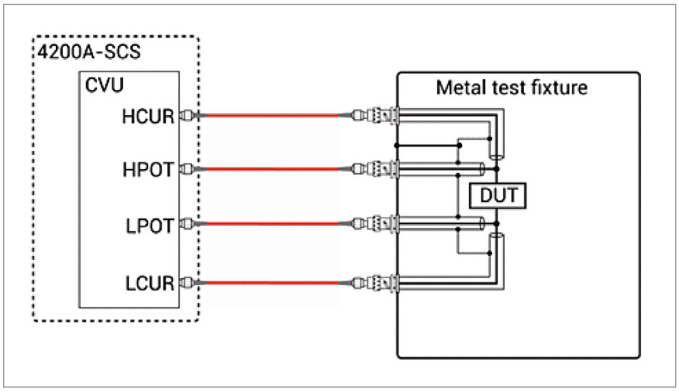


Figure 7. Proper connections from the CVU to a DUT

Figure 8 shows a ground jumper connecting the commons of two prober cable assemblies. Keithley Instruments has a series of 4210-MMPC Multi-Measurement Cable Kits for various probers that enable the common connections of various manipulators.

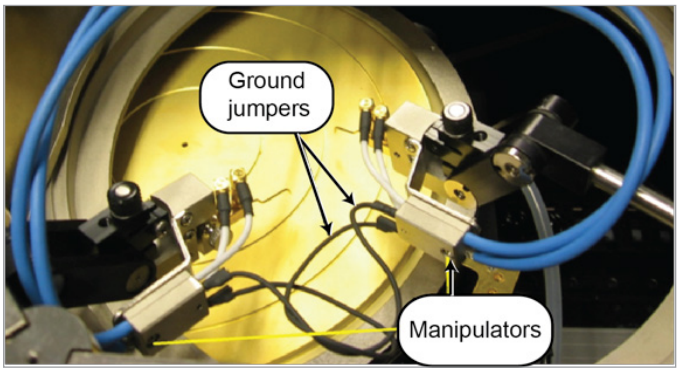


Figure 8. Ground jumper connecting the commons of two manipulators

In general, proper cabling is crucial to making successful capacitance measurements. Here are some potential cabling problems:

- Mismatched length on different CVU terminals
- Improper cable impedance (not using red SMA cables)
- Shield connections of all the cables not connected or not connected close enough to the DUT
- Bent, crimped or flattened cables
- SMA cable connectors not making good contact
- Not choosing the proper cable length in the Configure view of the Clarius software

Guarding the Chuck

Guarding can reduce the effects of parallel impedance, or stray capacitance, on capacitance measurement accuracy. The guard terminal is the outside shield of the coax connectors of the CVU. This guard terminal of the CVU should not be confused with the 4200A-SCS's GNDU terminal, which is connected to chassis ground.

When making C-V measurements between two terminals on the top of the wafer, it may be necessary to guard the chuck to reduce parallel capacitance between the terminals of the DUT and the chuck. In **Figure 9**, the stray capacitance is reduced by connecting the guard, the shields of the coax cables, to the chuck. For C-V measurements on devices that use the backside of the wafer as a contact, such as is the case for MOSCAPs, the chuck cannot be connected to guard.

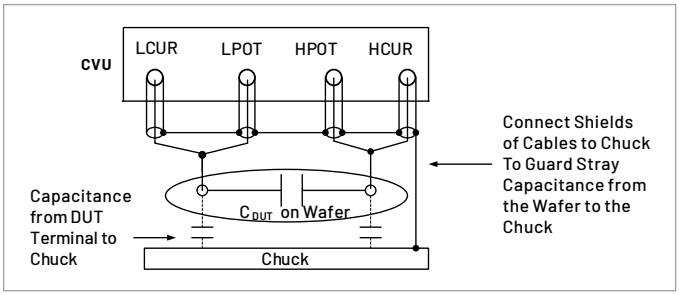


Figure 9. Connecting the CVU guard to the chuck

Guarding Device Terminals

To measure the capacitance between two terminals on a device with three or more terminals, it is important to guard the third terminal to prevent unwanted capacitances from affecting the measurement accuracy. This is best illustrated through an example. As shown in **Figure 10**, the CVU is connected to measure the capacitance between the Base and Emitter (C_{BE}) of a BJT.

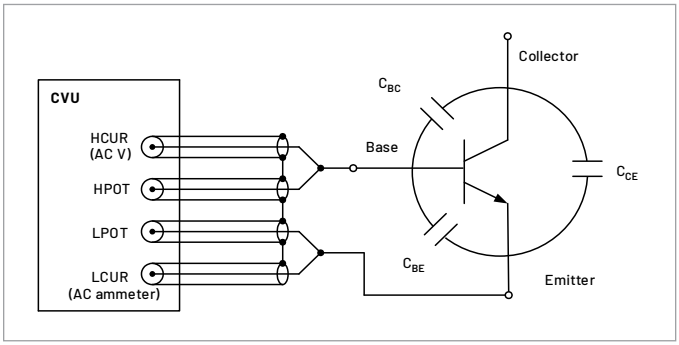


Figure 10. Measuring the base-emitter capacitance (CBE)

However, the series combination of capacitance between the other terminals (C_{BC} and C_{CE}) is in parallel with C_{BE} and creates an AC leakage path that can lead to erroneous readings. This parallel capacitance from the other terminals will affect the measurement (C_{MEAS}) as follows:

$$C_{MEAS} = C_{BE} + \left(\frac{C_{BC} \cdot C_{CE}}{C_{BC} + C_{CE}}\right)$$

To prevent the stray capacitance from affecting the measurement accuracy, the Collector is guarded by connecting it to the outside shield of the coax cable, which is at 0 VAC. This is illustrated in **Figure 11**. This AC guard routes the leakage capacitance current away from the AC current measurement terminal (LCUR), so that only the AC current due to C_{BE} is measured.

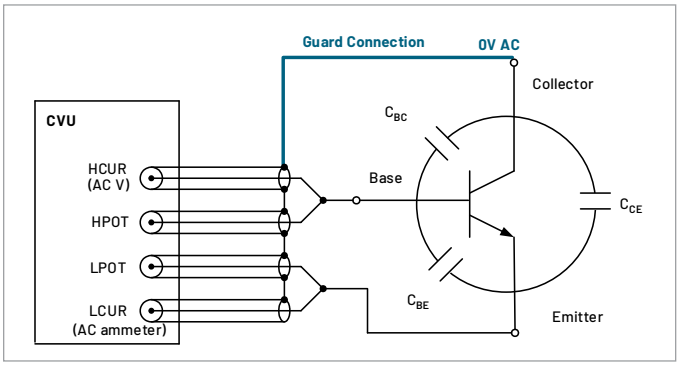


Figure 11. Guarded C-V measurement of BJT

Using the 4200A-CVIV Multi-Switch to Guard Device Terminals

Guarded C-V measurements can be automated using the optional 4200A-CVIV Multi-Switch, shown in **Figure 12**. The CVIV enables the user to switch automatically between I-V (SMU) and C-V (CVU) measurements on a device, as well as connect C-V guard to any terminal on the DUT.

Figure 12. 4200A-CVIV Multi-Switch

Figure 13 shows the CVHI, CVLO, and CV Guard terminals of the CVU connected to the three terminals of the BJT through the outputs of the 4200A-CVIV. In this example, the CV Guard is switched through Channel 3 of the 4200A-CVIV to the collector terminal of the BJT so that the base-emitter capacitance can be measured between CVHI and CVLO.

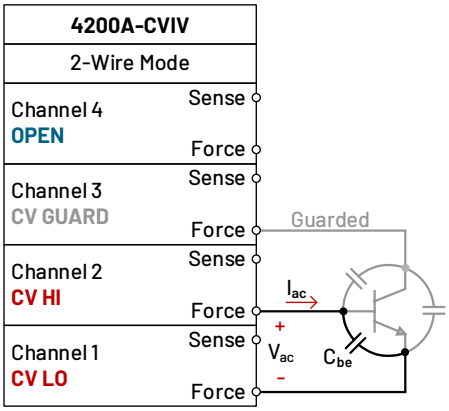


Figure 13. Connections from the 4200A-CVIV to a BJT for guarded measurements

The Clarius software allows users to change the output of the 4200A-CVIV automatically so that any of the terminals of the device can be guarded. **Figure 14** shows the CVIV Multi-Switch Channel Config settings in Clarius.

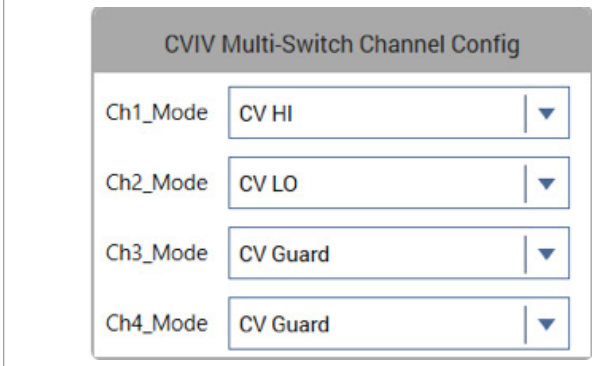


Figure 14. *cviv-configure* settings for base-emitter capacitance measurements on a BJT

AC Ammeter Connections

By default, the LCUR terminal of the CVU is the AC Ammeter connection, and the HCUR terminal is the AC Source Voltage terminal (as shown in **Figure 2**). However, users have the option to change the function of the terminals in the Advanced Terminal Settings window in the Clarius software as shown in **Figure 15**. Without the need to change cables manually, lift the prober needles, or physically change the test setup, it's easy to eliminate potential measurement problems by changing the terminal settings in the software.

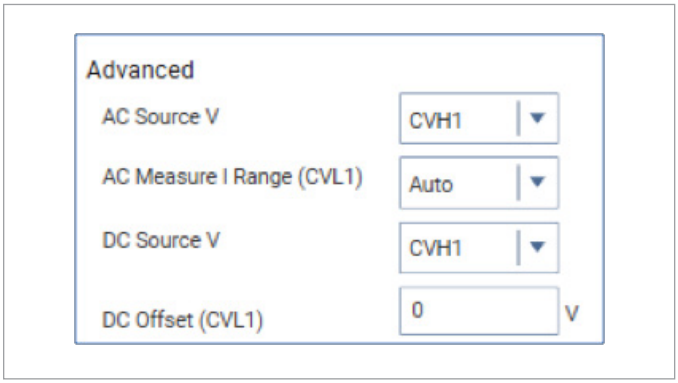


Figure 15. Advanced terminals settings

This feature allows measuring the AC current on the least noisy terminal, which will provide a more useful measurement. It's also possible to change the terminal

to which the DC voltage is applied. The DC voltage can be combined on the same terminal as the AC ammeter, which is ideal for connections to the gate of a MOS capacitor.

To avoid noisy measurements and stray capacitance, always connect the AC ammeter terminal to the terminal of the device that has the least amount of capacitance to ground. In the example shown in **Figure 16**, the LCUR (AC ammeter) connection is made to Pad 1 because it has less parasitic capacitance to common than Pad 2. In many cases, the user will not know which pad has the least capacitance to ground, but it's easy to check by reversing the HCUR and LCUR leads in the Advanced Terminal Settings tab and seeing if that produces better results.

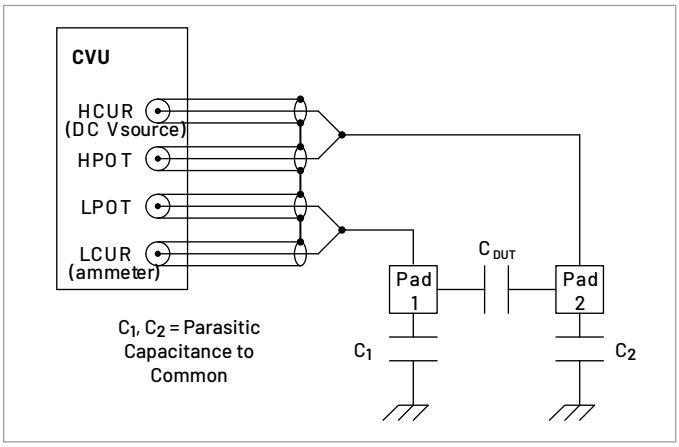


Figure 16. CVU measurements with parasitic capacitance to common

Connection Compensation

The CVU is designed to be connected to a prober or test fixture via interconnect cables and adaptors and may be possibly routed through a 4200A-CVIV Multi-Switch or switch matrix to the DUT. This cabling and switch matrix will add parasitic inductance and stray capacitance to the measurements. To correct for offset errors caused by these connections, the Clarius software has a built-in tool to perform compensation. Connection Compensation is a two-part process:

1. Acquire the CVU compensation data for open and short corrections. To perform the corrections in Clarius, select ***Tools*** and then select ***CVU Connection Compensation***. Select ***Measure Open*** or ***Measure Short***. When compensation data is acquired, it is taken at all test frequencies.
2. Enable the correction on the Terminal Settings pane of a CVU test.

Open Correction

Open correction is an offset correction for measuring small capacitances or high impedances. Probes must be up or the device removed from the test fixture during the correction. The outside shields of the cables must be tied together during the open correction, as shown in **Figure 17**.

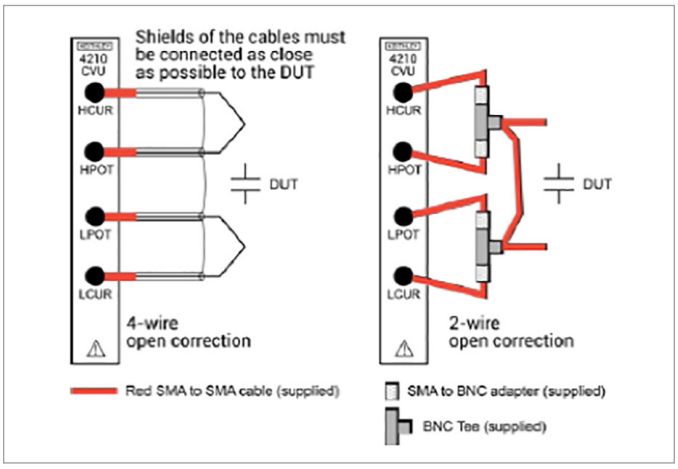


Figure 17. Connections for open connection compensation for the 4210-CVU and 4215-CVU

An example that shows the effects of Open Compensation is illustrated in the C-V curves for a MOSFET in **Figure 18**. These graphs show the C-V sweeps between the gate and the drain/source/bulk tied together generated with and without Open Compensation. The purple curve is without compensation and the blue curve is with compensation. The difference between the two curves is about 0.23 pF.

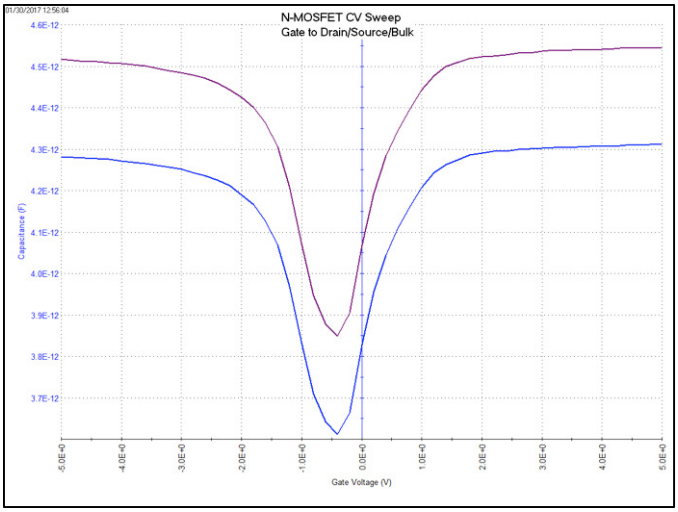


Figure 18. C-V measurements on a MOSFET with and without Open Compensation

Short Correction

Short correction is an offset correct for large capacitance, low impedance, and inductance measurements. Short compensation removes the effect of offsets caused by series resistance and parasitic inductance. Connect a short between all the output terminals, keeping the shields tied together. Use a BNC or SMA barrel to connect the cables together or short the probes together on a metal contact.

Timing Settings

To make successful C-V measurements, it's important to choose the appropriate timing parameters in the Clarius software. Adjustments to timing parameters can help prevent noisy measurements and allow acquiring readings in equilibrium. Timing adjustments are made in the CVU Advanced Test Settings window in the Configure view, which is shown in **Figure 19**. The following adjustments can allow for making quiet or settled readings:

Quiet Readings

- Use the Speed mode settings to adjust the measurement window. The longer the measurement time, or window, the less noisy measurements will be. First, try using the Quiet speed mode. If necessary, use the Custom speed which enables the user to set the time of the measurement window. The time of the measurement window can be calculated as follows: Measurement Window = (A/D Aperture Time) * (FilterFactor2 or Filter Count)
- Further information on making very sensitive capacitance measurements can be found in the Keithley Instruments application note, "Making Femtofarad (1e-15f) Capacitance Measurements with the 4215-CVU Capacitance Voltage Unit."

Settled Readings

- Sweep Delay time allows the device to charge up to equilibrium before taking a measurement.
- Apply a bias voltage for a specified Hold Time at the beginning of a sweep to allow the device to charge up to the first voltage step of the sweep prior to the start of the sweep.

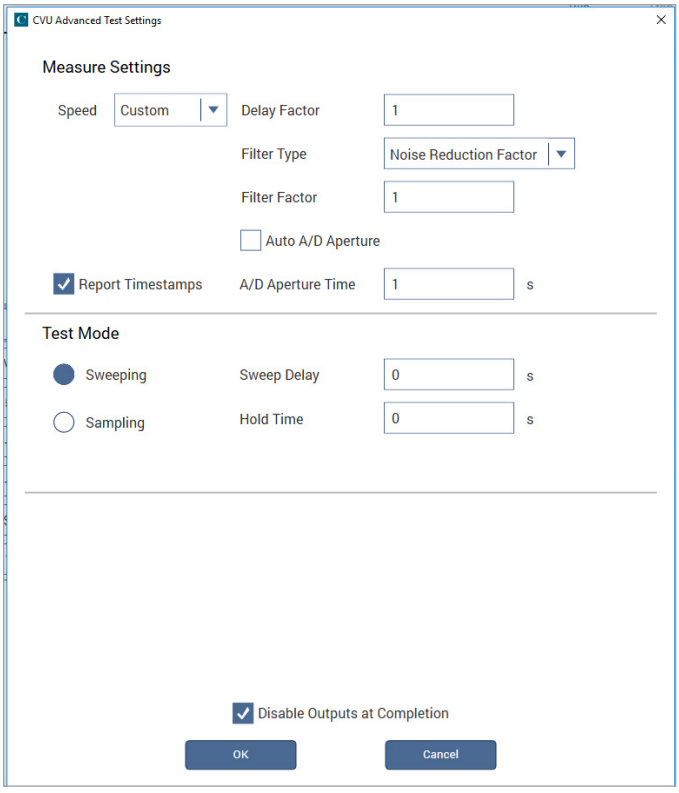


Figure 19. CVU Advanced Test Settings window

Equilibrium Conditions

The condition of a device when the internal capacitance is fully charged after an applied step voltage is referred to as the "equilibrium" condition. If C-V measurements are made before the device is in equilibrium, inaccurate results may occur. There are two ways to verify if a device is in equilibrium:

1. Check the shape of the C-V curve when sweeping from either direction. For example, the C-V curve of a MOSCAP should look the same from accumulation to inversion or from inversion to accumulation. For testing MOSCAPs, further information on choosing Hold and Sweep Delay times can be found in the Keithley application note, "C-V Characterization of MOS Capacitors using the 4200A-SCS Parameter Analyzer."
2. Set up a test in the Sampling mode to apply a voltage bias and graph the capacitance vs. time of the device. Observe from the graph the time it takes for the device to charge up. For example, the graph in **Figure 20** shows a curve of the capacitance vs. time, measured between the emitter and base of a BJT. The applied voltage was 0.5 VDC. From the graph, the equilibrium time is about 13 seconds. Because the equilibrium time is very long for this device, it may be a bad device. This is the process to use to determine the equilibrium time.

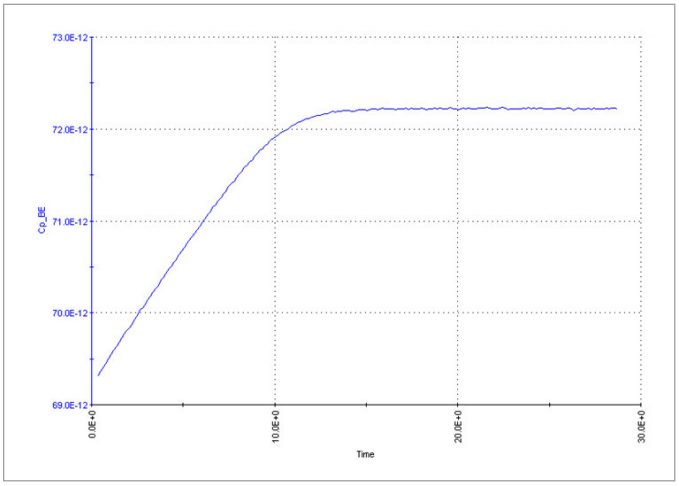


Figure 20. Equilibrium time measurement example

Dissipation Factor and Choosing the Correct Measure Model

One way of determining the confidence in capacitance measurements is to check the dissipation factor (D), which is defined as the ratio between the reactance and the resistance of a simple parallel capacitance model. Here is the equation for parallel and series models:

$$D = \frac{Reactance}{Resistance} = \frac{1}{2\pi f R_P C_P} = 2\pi f R_S C_S$$

where:

R_P = the parallel resistance of the test device in Ω

C_P = the parallel capacitance of the test device in F

f = the test frequency in Hz

R_S = the series resistance of the test device in Ω

C_S = the series capacitance of the test device in F

The parallel capacitance (C_P) and series capacitance (C_S) are related by the following equation:

$$C_P = C_S \left(\frac{1}{1 + D^2}\right)$$

With the CVU, it's possible to measure the dissipation factor by selecting the C_P-D Measure Parameter in the Advanced Test Settings window, as shown in **Figure 21**.

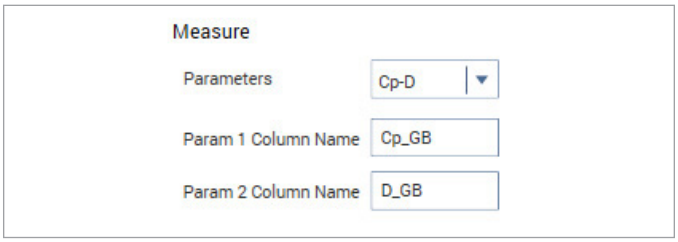


Figure 21. Selecting the C_P-D measurement parameter

Ideally, C_P and C_S should be equal. This will occur if D=0. Even if D is small (<0.1), there is effectively no difference between C_P and C_S. However, if D is large (>0.1), then it's necessary either to determine the correct model or troubleshoot the measurements.

If C_P and C_S are not equal and D is large, it's possible to determine which model, series or parallel, is correct. Separately measure C_P and C_S as a function of voltage or frequency. If either of the C-V or C-f curves are flat for C_P or C_S, then that is the correct model (series or parallel) to use. If none of the curves are flat, then it's necessary to troubleshoot the measurements to figure out the source of the problem. The problem might be a leaky device, connection issues (cabling), or a device issue such as AC leakage between the pads (may need to use AC guarding).

Troubleshooting

When troubleshooting capacitance measurements, the CVU has built-in tools that can help. In addition to using Cable Compensation, adjusting the AC Ammeter Connections, and setting the appropriate Timing Parameters as previously discussed, other tools in Clarius such as Confidence Check, Real-Time Measurements, Status Codes, and Status Indicators are available.

Confidence Check

Confidence Check is a diagnostic tool that allows checking the integrity of open and short connections. This is especially important if making measurements through a switch. To enable Confidence Check, select Tools at the top of the Clarius screen.

To verify an open circuit, lift the probes or remove the device from the test fixture. Select Check Open. Follow the instructions and select OK. When the open check is complete, the dialog box displays the results of the test. This process can be repeated to test for a Short after a short is connected. If either test fails, the results include suggestions for troubleshooting. In the example shown in **Figure 22**, the Open test passed and the Short test failed.

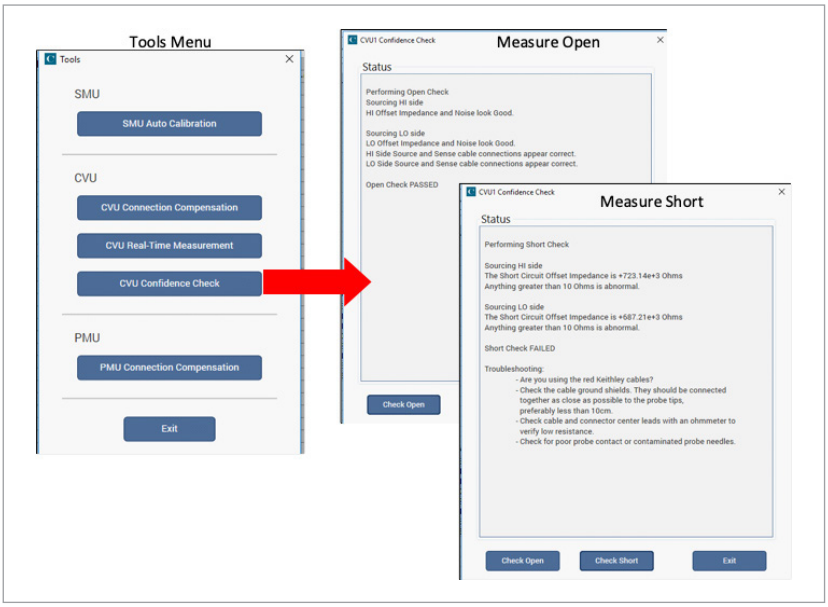


Figure 22. CVU Confidence Check Open and Short Dialog boxes

Real-Time Measurements

The CVU Real-Time Measurement Mode in the Tools menu provides a direct, real-time user interface to the CVU to help in system setup and debugging. The Real-Time Measurement window is shown in F**igure 23**. For example, it can be used to confirm that contact has been made from the CVU to the pads on a wafer. Follow these steps to generate real-time measurements:

- Go to the **Tools** menu
- Select **CVU Real-Time Measurement**
- Set up the desired parameter settings
- Select **Run**
- Select **Stop** to quit taking readings.

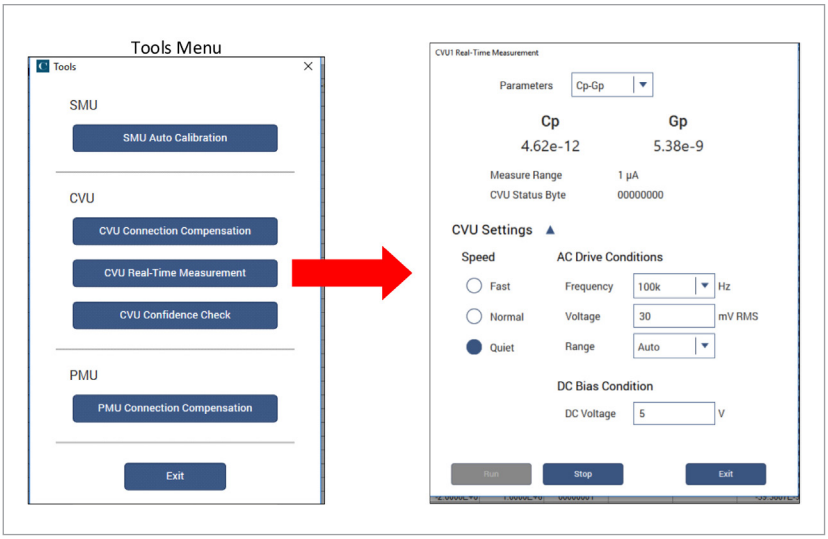


Figure 23. Real-Time Measurements window

Status Indicators

The CVU status code indicates the current measurement range, including an overflow condition, for each reading and flags any errors. When enabled, a data column labeled CVU1S will appear in the Sheet in the Analyze View. Enable status code by selecting Report Status, located in the Advanced Terminal Settings tab in the Configure view.

When a measurement error occurs, the entire row of data in the Sheet related to the measurement changes color. The data values in the flagged data become color-coded, as shown in **Figure 24**, to identify the error type:

- Red: Measurement Time Out
- Magenta: Measurement Overflow
- Yellow: Auto-Balance Bridge (ABB) not locked

	Cp_GB	Gp_GB	DCV_GB	F_GB	CVU1S
1	-68.9487E-12	1.4925E-3	5.0000E+0	1.0000E+6	09000001
2	-68.8932E-12	1.4925E-3	4.8000E+0	1.0000E+6	09000001
3	-68.8374E-12	1.4926E-3	4.6000E+0	1.0000E+6	09000001
4	-69.1123E-12	1.4921E-3	4.4000E+0	1.0000E+6	09000001

Figure 24. Example of flagged measurement errors appearing in the Sheet

ABB Unlock Errors

The CVU uses the auto-balancing bridge (ABB) technique to achieve accurate impedance measurements. The ABB creates a virtual ground at the DUT to minimize measurement error. Every CVU measurement is made with ABB active. The ABB always attempts to lock the low side of the DUT to virtual ground.

If the ABB fails to lock, the measurement is made but may be out of specification. If this occurs, the returned data is flagged and shown in yellow on the Analyze sheet. Here are the common reasons that the ABB fails to lock:

- The cable lengths connected to the CVU terminals are not the same
- HPOT or LPOT terminals are disconnected
- Excessive noise in the LPOT terminal
- High frequency sources
- Physical cable lengths do not match the cable length set in Clarius
- Improperly torqued SMA cables
- Too much parasitic noise

Error Symptoms

Table 1 provides some troubleshooting tips for various measurement problems.

Table 1. C-V Measurement Troubleshooting Table

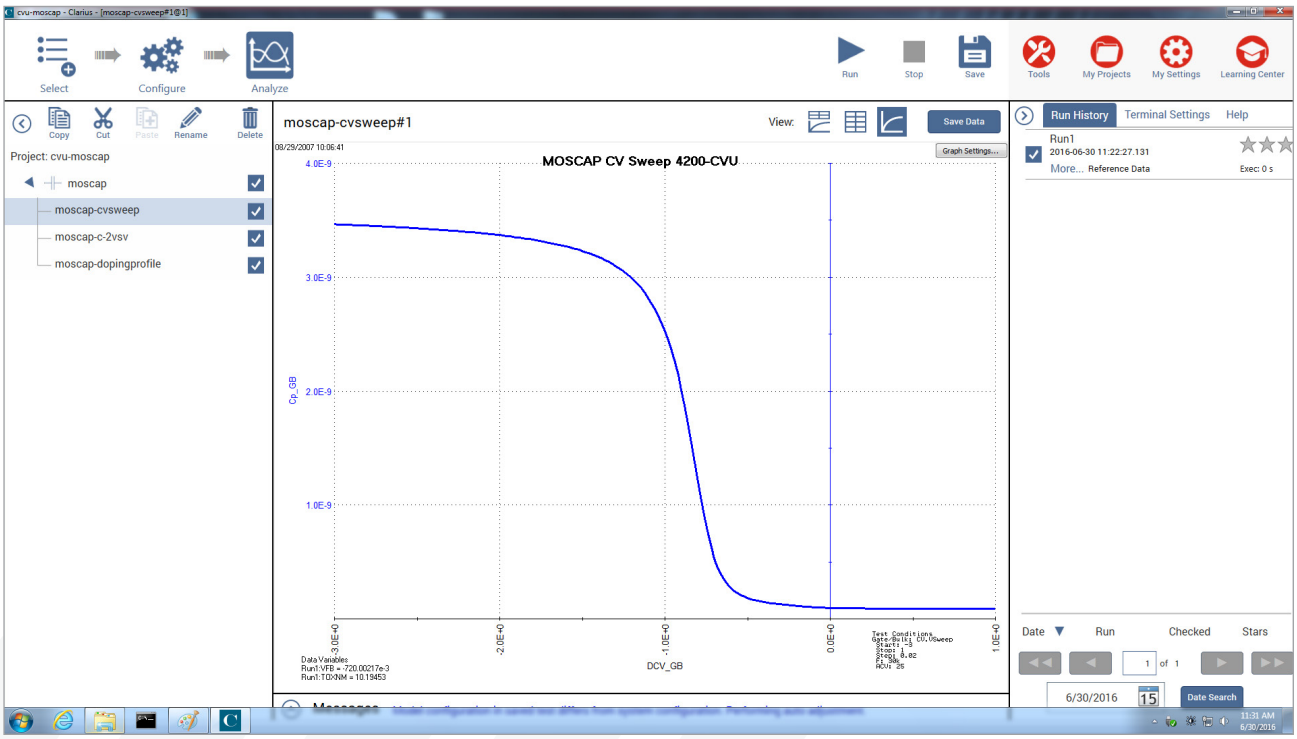
Error Symptoms	Possible Causes	Suggestions to Minimize or Avoid Errors
Capacitance too high	Cabling and connections capacitance	Use Open Connection Compensation, minimize stray capacitance
	Light left ON or lid open	Turn off light
	Unwanted capacitance from other terminals	Use guarding
	Short or leaky device	Try another DUT, use Confidence Check for verification, check if dissipation factor <0.1
Capacitance too low	Device not in equilibrium	Increase delay or hold time
	Poor or no contact to device	Re-verify connections and use Confidence Check to check for Open. May need to improve contact between wafer and chuck.
	Open device	Try another device to verify if the problem is the device or something else. Use Confidence Check.
	Coax cable shields not connected	Connect shields as close as possible to the device.
Noisy Measurements	Environment	Use Quiet or Custom Speed Modes. Increase or reduce test frequency depending on magnitude of capacitance. Verify prober contact to device.
	CVL and CVH connections inverted	Try switching terminals in the Advanced Test Settings Window.
	Device not shielded	Enclose device in shielded test fixture that is connected to outside shields of coax cables.
"Tails" on end of C-V sweep	Device not in equilibrium	Set PreSoak voltage to first voltage point in sweep and use sufficient Hold Time to allow device to charge up.
	Leaky device	Try measuring the leakage current using the SMU, reduce the DC voltage.

Conclusion

Good capacitance measurements can be easily achieved using the CVU's built-in measurement tools, proper cabling and connections, and appropriate measurement techniques. Some of the many built-in tools include compensation, timing parameters, and confidence check.

Tektronix®

C-V Characterization of MOS Capacitors Using the 4200A-SCS Parameter Analyzer



Introduction

Maintaining the quality and reliability of gate oxides of MOS structures is a critical task in a semiconductor fab. Capacitance-voltage (C-V) measurements are commonly used in studying gate-oxide quality in detail. These measurements are made on a two-terminal device called a MOS capacitor (MOS cap), which is basically a MOSFET without a source and drain. C-V test results offer a wealth of device and process information, including bulk and interface charges. Many MOS device parameters, such as oxide thickness, flatband voltage, threshold voltage, etc., can also be extracted from the C-V data.

Using a tool such as the Keithley 4200A-SCS Parameter Analyzer equipped with the 4210-CVU or 4215-CVU Integrated C-V Option for making C-V measurements on MOS capacitors can simplify testing and analysis. The 4200A-SCS is an integrated measurement system that can include instruments for both I-V and C-V measurements, as well as software, graphics, and mathematical analysis capabilities. The software incorporates C-V tests, which include a variety of complex formulas for extracting common C-V parameters.

This application note discusses how to use a Keithley 4200A-SCS Parameter Analyzer equipped with the 4210-CVU or 4215-CVU Integrated C-V Option to make C-V measurements on MOS capacitors. It also addresses the basic principles of MOS caps, performing C-V measurements on MOS capacitors, extracting common C-V parameters, and measurement techniques. The Keithley Clarius software that controls the 4200A-SCS incorporates many tests and projects specific to C-V testing. Each project is paired with the formulas necessary to extract common C-V parameters, such as oxide capacitance, oxide thickness, doping density, depletion depth, Debye length, flatband capacitance, flatband voltage, bulk potential, threshold voltage, metal-semiconductor work function difference, and effective oxide charge. This completeness is in sharp contrast to other commercially available C-V solutions, which typically require the user to research and enter the correct formula for each parameter manually.

Overview of C-V Measurement Technique

By definition, capacitance is the change in charge (Q) in a device that occurs when it also has a change in voltage (V):

$$C \equiv \frac{\Delta Q}{\Delta V}$$

One general practical way to implement this is to apply a small AC voltage signal (millivolt range) to the device under test, and then measure the resulting current. Integrate the current over time to derive Q and then calculate C from Q and V.

C-V measurements in a semiconductor device are made using two simultaneous voltage sources: an applied AC voltage signal (dV_{ac}) and a DC voltage (V_{dc}) that is swept in time, as illustrated in **Figure 1**.

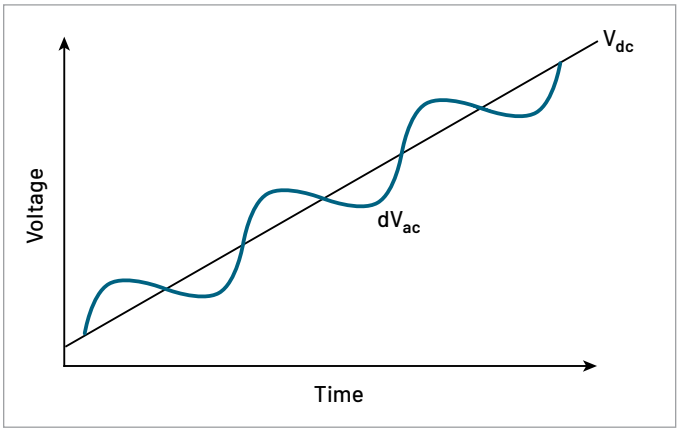


Figure 1. AC and DC voltage of C-V Sweep Measurement

The magnitude and frequency of the AC voltage are fixed; the magnitude of the DC voltage is swept in time. The purpose of the DC voltage bias is to allow sampling of the material at different depths in the device. The AC voltage bias provides the small-signal bias so the capacitance measurement can be performed at a given depth in the device.

Basic Principles of MOS Capacitors

Figure 2 illustrates the construction of a MOS capacitor. Essentially, the MOS capacitor is just an oxide placed between a semiconductor and a metal gate. The semiconductor and the metal gate are the two plates of the capacitor. The oxide functions as the dielectric. The area of the metal gate defines the area of the capacitor.

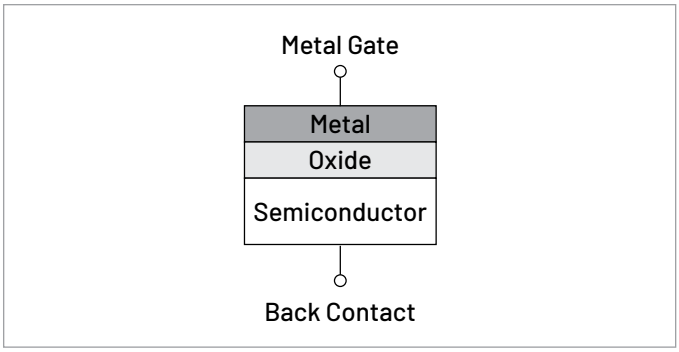


Figure 2. MOS capacitor

The most important property of the MOS capacitor is that its capacitance changes with an applied DC voltage. As a result, the modes of operation of the MOS capacitor change as a function of the applied voltage. **Figure 3** illustrates a high frequency C-V curve for a p-type semiconductor substrate. As a DC sweep voltage is applied to the gate, it causes the device to pass through accumulation, depletion, and inversion regions.

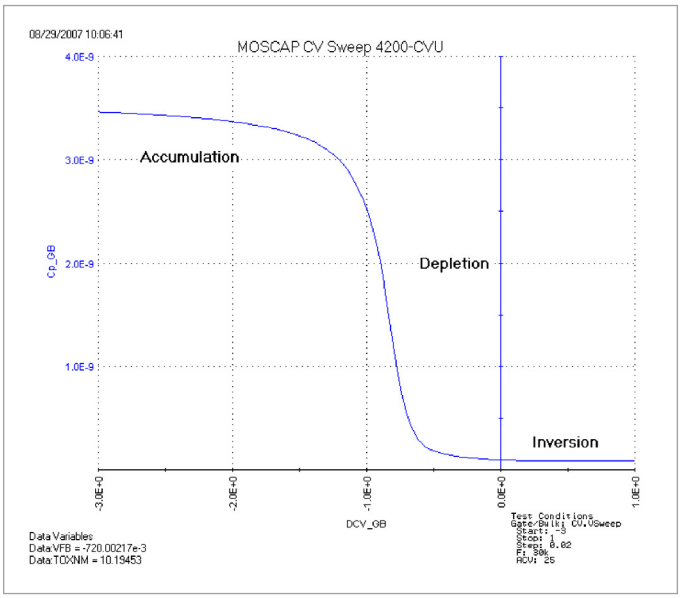


Figure 3. C-V curve of a p-type MOS capacitor measured with the CVU

The three modes of operation, accumulation, depletion and inversion, will now be discussed for the case of a p-type semiconductor, then briefly discussed for an n-type semiconductor at the end of this section.

Accumulation Region

With no voltage applied, a p-type semiconductor has holes, or majority carriers, in the valence band. When a negative voltage is applied between the metal gate and the semiconductor, more holes will appear in the valence band at the oxide-semiconductor interface. This is because the negative charge of the metal causes an equal net positive charge to accumulate at the interface between the semiconductor and the oxide. This state of the p-type semiconductor is called accumulation.

For a p-type MOS capacitor, the oxide capacitance is measured in the strong accumulation region. This is where the voltage is negative enough that the capacitance is essentially constant and the C-V curve is almost flat. This is where the oxide thickness can also be extracted from the oxide capacitance. However, for a very thin oxide, the slope of the C-V curve doesn't flatten in accumulation and the measured oxide capacitance differs from the actual oxide capacitance.

Depletion Region

When a positive voltage is applied between the gate and the semiconductor, the majority carriers are replaced from the semiconductor-oxide interface. This state of the semiconductor is called depletion because the surface of the semiconductor is depleted of majority carriers. This area of the semiconductor acts as a dielectric because it can no longer contain or conduct charge. In effect, it becomes an insulator.

The total measured capacitance now becomes the oxide capacitance and the depletion layer capacitance in series, and as a result, the measured capacitance decreases. This decrease in capacitance is illustrated in **Figure 3** in the depletion region. As a gate voltage increases, the depletion region moves away from the gate, increasing the effective thickness of the dielectric between the gate and the substrate, thereby reducing the capacitance.

Inversion Region

As the gate voltage of a p-type MOS-C increases beyond the threshold voltage, dynamic carrier generation and recombination move toward net carrier generation. The positive gate voltage generates electron-hole pairs and attracts electrons (the minority carriers) toward the gate. Again, because the oxide is a good insulator, these minority carriers accumulate at the substrate-to-oxide/well-to-oxide interface. The accumulated minority-carrier layer is called the inversion layer because the carrier polarity is inverted. Above a certain positive gate voltage, most available minority carriers are in the inversion layer, and further gate-voltage increases do not further deplete the semiconductor. That is, the depletion region reaches a maximum depth.

Once the depletion region reaches a maximum depth, the capacitance that is measured by the high frequency capacitance meter is the oxide capacitance in series with the maximum depletion capacitance. This capacitance is often referred to as minimum capacitance. The C-V curve slope is almost flat.

NOTE: The measured inversion-region capacitance at the maximum depletion depth depends on the measurement frequency. Therefore, C-V curves measured at different frequencies may have different appearances. Generally, such differences are more significant at lower frequencies and less significant at higher frequencies.

n-type Substrate

The C-V curve for an n-type MOS capacitor is analogous to a p-type curve, except that (1) the majority carriers are electrons instead of holes; (2) the n-type C-V curve is essentially a mirror image of the p-type curve; (3) accumulation occurs by applying a positive voltage to the gate; and (4) the inversion region occurs at negative voltage.

Performing C-V Measurements with the CVU

To simplify testing, a project has been created for the 4200A-SCS that makes C-V measurements on a MOS capacitor and extracts common measurement parameters such as oxide thickness, flatband voltage, threshold voltage, etc. The *MOS Capacitor C-V Project* (*cvu-moscap*) is included with all 4200A-SCS systems in the Clarius application. **Figure 4** is a screen shot of the project, which has three tests that generate a C-V sweep *(moscap-cvsweep)*, a $1/C^2$ vs. Gate Voltage curve *(moscap-c-2vsv)*, and a doping profile *(moscap-dopingprofile)*. **Figure 4** also illustrates a C-V sweep generated with the *moscap-cvsweep* test. All of the extracted C-V parameters in these test modules are defined in the next section of this application note.

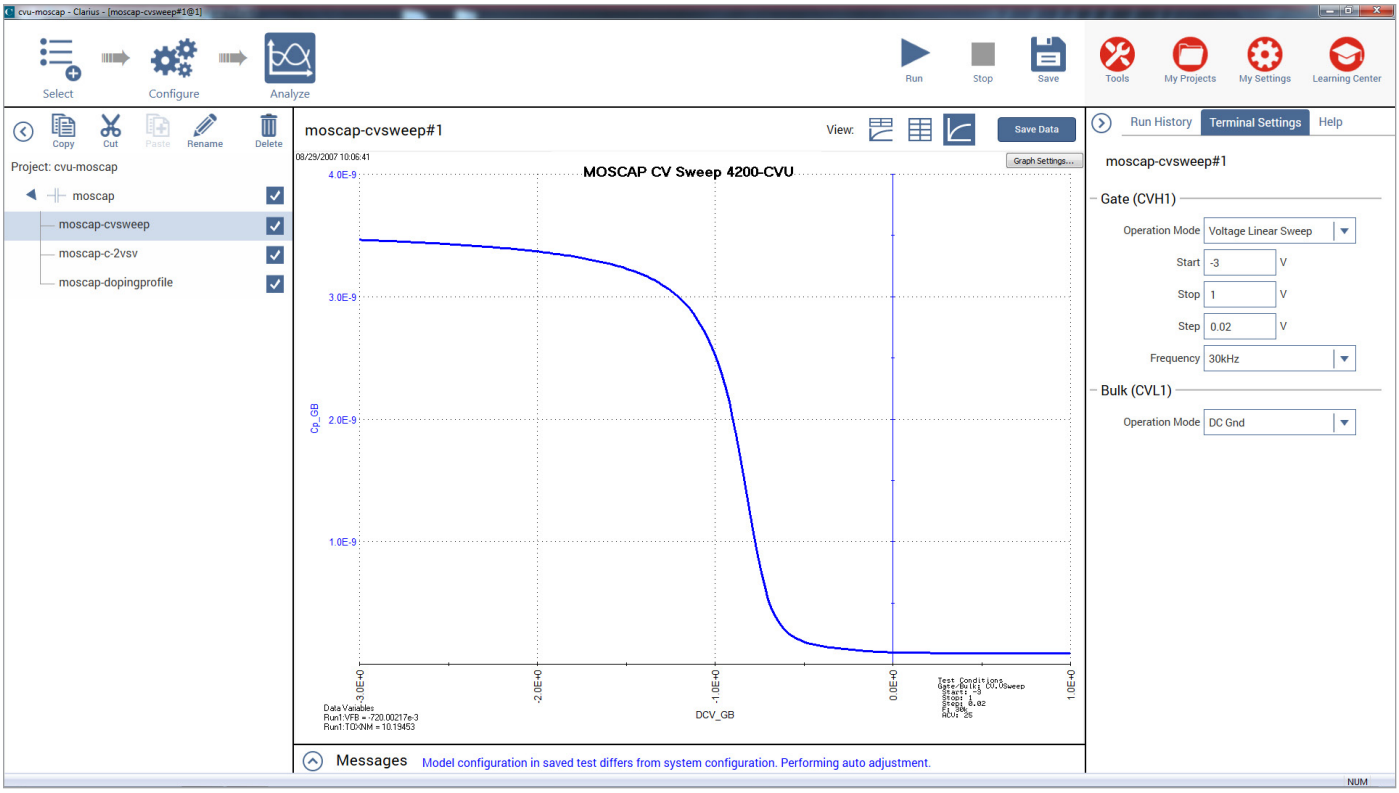


Figure 4. C-V sweep created with *moscap-cvsweep* test for the 4200A.

MOS Capacitor C-V Sweep (moscap-cvsweep) Test

This test performs a capacitance measurement at each step of a user-configured linear voltage sweep. A C-V graph is generated from the acquired data, and several device parameters are calculated using the Formulator, which is a tool in the 4200A-SCS's software that provides a variety of computational functions, common mathematical operators, and common constants. **Figure 5** shows the window of the Formulator. These derived parameters are listed in the Analyze view of the test.

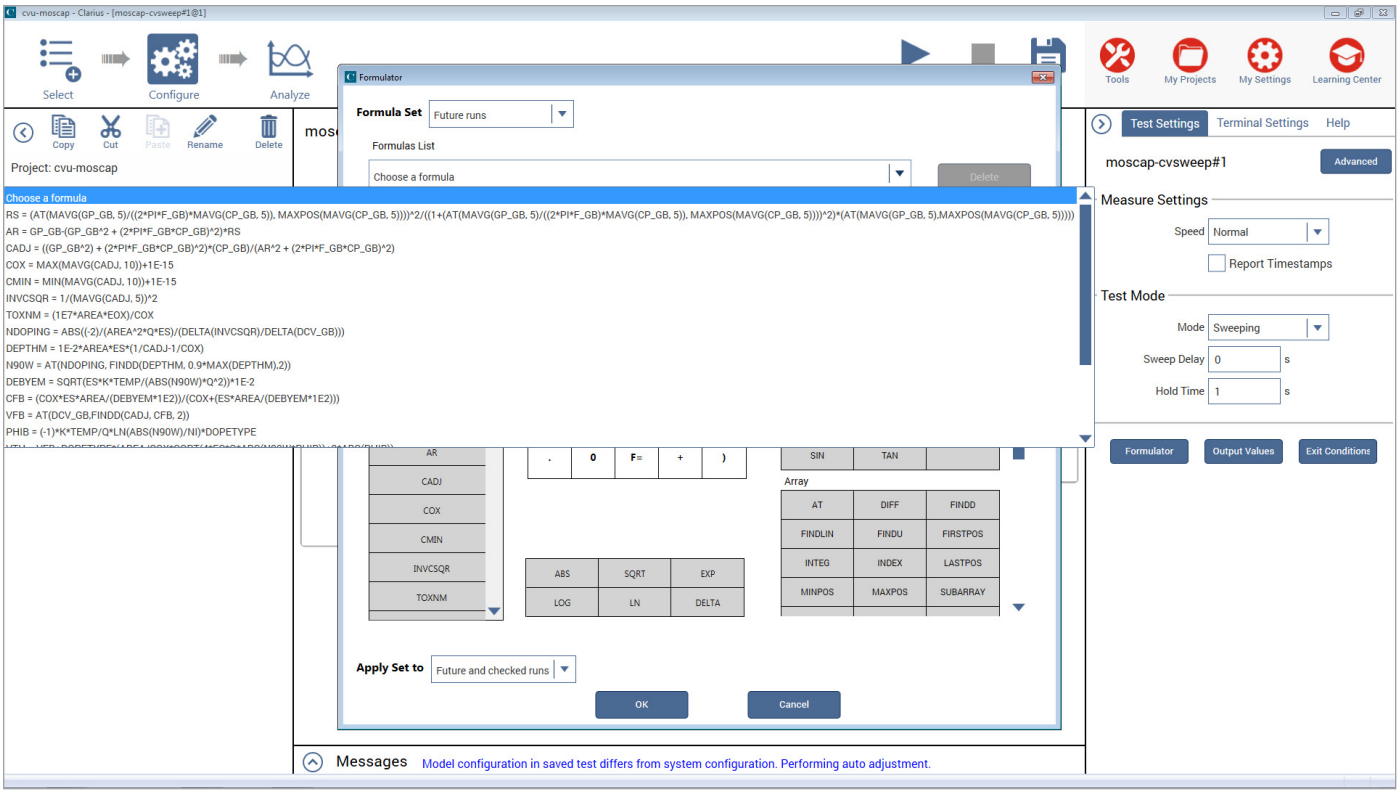


Figure 5. Formulator window with parameters derived

MOS Capacitor I/C² vs. Gate Voltage Sweep (moscap-c-2vsv) Test

This test performs a C-V sweep and displays the capacitance ($1/C^2$) as a function of the gate voltage (V_G). This sweep can yield important information about doping profile because the substrate doping concentration (N_{SUB}) is inversely related to the reciprocal of the slope of the $1/C^2$ vs. V_G curve. A positive slope indicates acceptors and a negative slope indicates donors. The substrate doping concentration is extracted from the slope of the $1/C^2$ curve and is displayed on the graph. **Figure 6** shows the results of executing this test module.

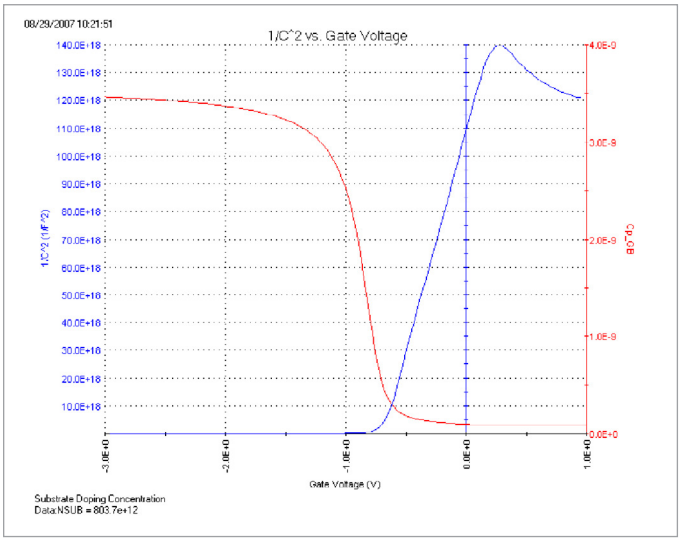


Figure 6. $1/C^2$ vs. gate voltage plot generated with the CVU

MOS Capacitor Doping Profile (moscap-dopingprofile) Test

This test performs a doping profile, which is a plot of the doping concentration vs. depletion depth. The difference in capacitance at each step of the gate voltage is proportional to the doping concentration. The depletion depth is computed from the high frequency capacitance and oxide capacitance at each measured value of the gate voltage. The results are plotted on the graph as shown in **Figure 7.**

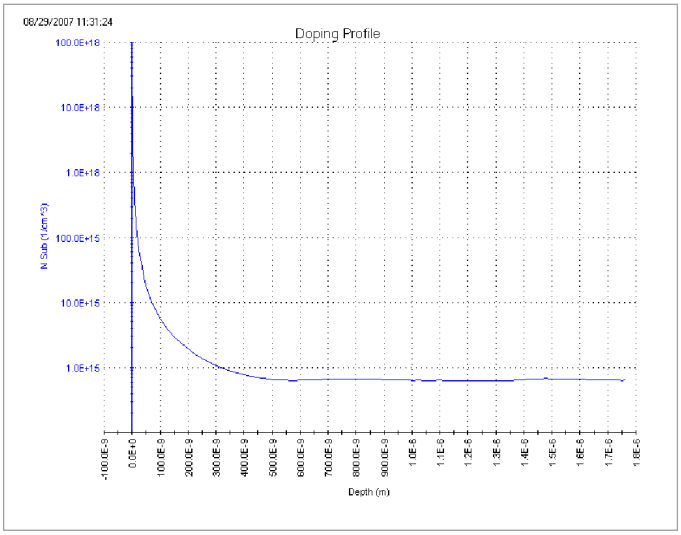


Figure 7. Doping profile extracted from C-V data taken with the CVU

Connections to the CVU

To make a C-V measurement, a MOS cap is connected to the CVU as shown in **Figure 8**. In the test, both the CVU ammeter and the DC voltage appear at the HCUR/HPOT terminals. See the next section, "Measurement Optimization," for further information on connecting the CVU to the device on a wafer.

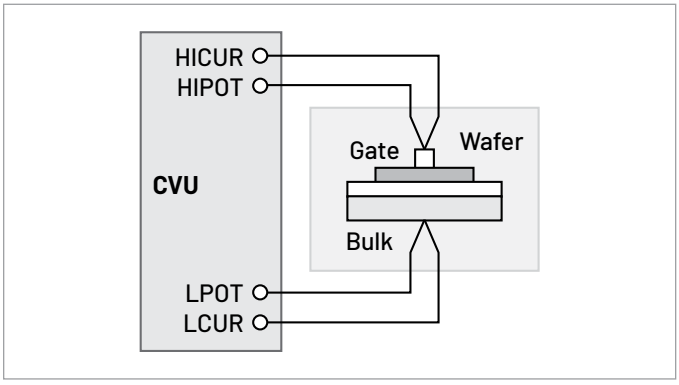


Figure 8. Basic configuration to test MOS capacitor with the CVU

Measurement Optimization

Successful measurements require compensating for stray capacitance, measuring at equilibrium conditions, and compensating for series resistance.

Offset Correction for Stray Capacitance

C-V measurements on a MOS capacitor are typically performed on a wafer using a prober. The CVU is designed to be connected to the prober via interconnect cables and adaptors and may possibly be routed through a switch matrix. This cabling and switch matrix will add stray capacitance to the measurements.

To correct for stray capacitance, the Clarius software has a built-in tool for offset correction, which is a two-part process: the corrections for open and/or short are performed first, and then they can be enabled within a test.

To perform the corrections, select Tools and select CVU Connection Compensation. For an Open correction, select Measure Open. Probes must be up during the correction. Open is typically used for high impedance measurements (<10pF or >1MΩ).

For a Short correction, select Measure Short. Short the probe to the chuck. A short correction is generally performed for low impedance measurements (>10nF or <10Ω).

After the corrections are performed, they must be enabled in the test. To enable corrections, select the CVU Open and/or Short checkboxes in the Terminal Settings pane (**Figure 9**).

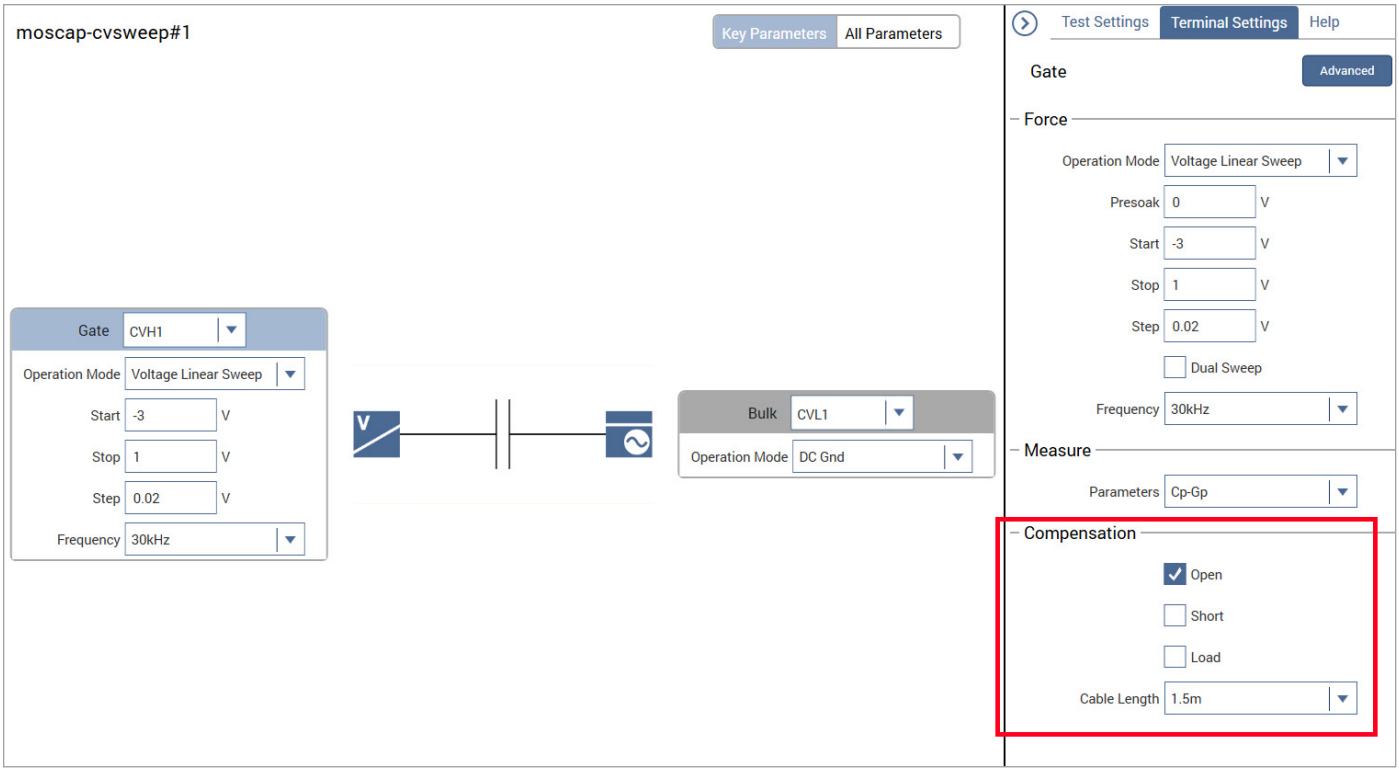


Figure 9. CVU compensation window

Measuring at Equilibrium Conditions

A MOS capacitor takes time to become fully charged after a voltage step is applied. C-V measurement data should only be recorded after the device is fully charged. This condition is called the equilibrium condition. Therefore, to allow the MOS capacitor to reach equilibrium: (1) allow a sufficient Hold Time in the Test Settings panel to enable the MOS capacitor to charge up while applying a "PreSoak" voltage, and (2) allow a sufficient Sweep Delay Time before recording the capacitance after each voltage step of a voltage sweep. The appropriate Hold and Delay Times are determined experimentally by generating capacitance vs. time plots and observing the time for the capacitance to settle.

Although C-V curves swept from different directions may look different, allowing adequate Hold and Delay Times minimizes such differences. One way to determine sufficient Hold and Delay Times is to generate a series of C-V curves in both directions. Change the Hold and Delay Times for each pair of inversion → accumulation and accumulation → inversion curves until the curves look essentially the same for both sweep directions.

Hold and Delay Times When Sweeping from Inversion → Accumulation. When the C-V sweep starts in the inversion region and the starting voltage is initially applied, a MOS capacitor is driven into deep depletion. Thereafter, if the starting voltage is maintained, the initial high frequency C-V curve climbs toward and ultimately stabilizes to the minimum capacitance at equilibrium. However, if the initial Hold Time is too short, the MOS capacitor cannot adequately recover from deep depletion, and the measured capacitance will be smaller than the minimum capacitance at equilibrium. Set the "PreSoak" voltage to the first voltage in the voltage sweep and allow a sufficient Hold Time for the MOS capacitor to reach equilibrium.

However, once the MOS capacitor has reached equilibrium after applying the "PreSoak" voltage, an inversion → accumulation C-V sweep may be performed with small delay times. This is possible because minority carriers recombine relatively quickly as the gate voltage is reduced. Nonetheless, if the Delay Time is too short, non-equilibrium occurs, and the capacitance in the inversion region is slightly higher than the equilibrium value. This is illustrated by the upper dotted line in **Figure 10.**

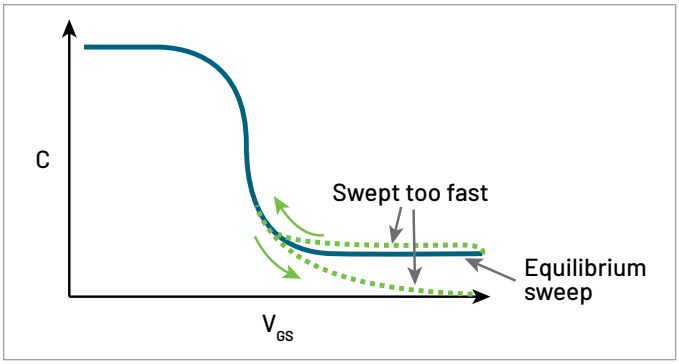


Figure 10. Effects of performing a C-V sweep too quickly

Hold and Delay Times When Sweeping from Accumulation → Inversion. When the C-V sweep starts in the accumulation region, the effects of Hold and Delay Times in the accumulation and depletion regions are fairly subtle. However, in the inversion region, if the Delay Time is too small (i.e., the sweep time is too fast), there's not enough time for the MOS capacitor to generate minority carriers to form an inversion layer. On the high frequency C-V curve, the MOS capacitor never achieves equilibrium and eventually becomes deeply depleted. The measured capacitance values fall well below the equilibrium minimum value. The lower dotted line in **Figure 10** illustrates this phenomenon.

Using the preferred sequence. Generating a C-V curve by sweeping from inversion to accumulation is faster and more controllable than sweeping from accumulation to inversion. **Figure 11** illustrates a preferred measurement sequence.

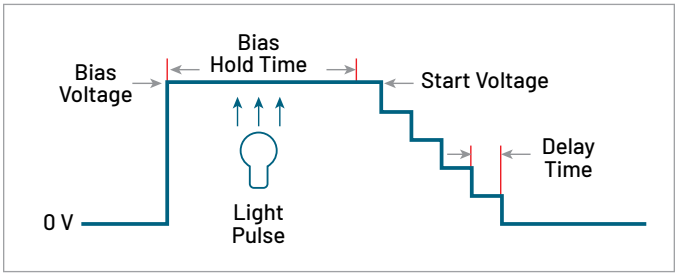


Figure 11. Preferred C-V measurement Sequence

The device is first biased at the "PreSoak" voltage for the specified Hold Time. The bias or "PreSoak" voltage should be the same as the sweep start voltage to avoid a sudden voltage change when the sweep starts. During biasing, if necessary, a short light pulse can be applied to the sample to help generate minority carriers. However, before the sweep starts, all lights should be turned off. All measurements should be performed in total darkness because the semiconductor material may be light sensitive. During the sweep, the Delay Time should be chosen to create the optimal balance between measurement speed and measurement integrity, which requires adequate equilibration time.

Compensating for series resistance

After generating a C-V curve, it may be necessary to compensate for series resistance in measurements. The series resistance (R_{SERIES}) can be attributed to either the substrate (well) or the backside of the wafer. For wafers typically produced in fabs, the substrate bulk resistance is fairly small (<10Ω) and has negligible impact on C-V measurements. However, if the backside of the wafer is used as an electrical contact, the series resistance due to oxides can significantly distort a measured C-V curve. Without series compensation, the measured capacitance can be lower than the expected capacitance, and C-V curves can be distorted. Tests for this project compensate for series resistance using the simplified three-element shown in **Figure 12**. In this model, C_{OX} is the oxide capacitance and C_A is the capacitance of the accumulation layer. The series resistance is represented by R_{SERIES}.

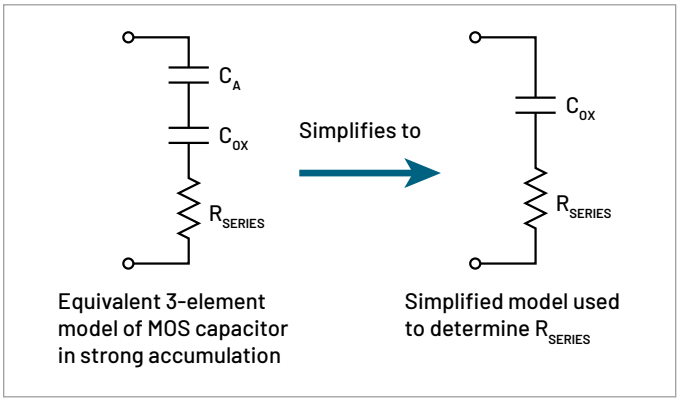


Figure 12. Simplified model to determine series resistance

The corrected capacitance (C_{ADJ}) and corrected conductance (G_{ADJ}) are calculated from the following formulas [1]:

$$C_{ADJ} = \frac{(G^2 + (2\pi fC)^2)C}{a_R^2 + (2\pi fC)^2}$$

$$G_{ADJ} = \frac{(G^2 + (2\pi fC)^2)a_R}{a_R^2 + (2\pi fC)^2}$$

where:

$a_R = G - (G^2 + (2\pi fC)^2)R_S$

C_{ADJ} = series resistance compensated parallel capacitance

C = measured parallel capacitance

G_{ADJ} = series resistance compensated conductance

G = measured conductance

f = test frequency

R_S = series resistance

The series resistance (R_S) may be calculated from the capacitance and conductance values that are measured while biasing the DUT (device under test) in the accumulation region as follows:

$$R_S = \frac{\left(\frac{G}{2\pi fC}\right)^2}{\left[1 + \left(\frac{G}{2\pi fC}\right)^2\right]G}$$

where:

R_S = series resistance

G = measured conductance

C = measured parallel capacitance (in strong accumulation)

f = test frequency

NOTE: The preceding equations for compensating for series resistance require that the CVU be using the parallel model (Cp-Gp).

For this project, these formulas have been added into the Formulator so the capacitance and conductance can be automatically compensated for the series resistance.

Extracting MOS Device Parameters From C-V Measurements

This section describes the device parameters that are extracted from the C-V data taken in the three test modules in the *MOS Capacitor C-V Project*. The parameters are derived in the Formulator and the calculated values appear in the Sheet tab in the Analyze view of each test as shown in **Figure 13**.

moscap-cvsweep#1 View: Save Data

Run1 Formulas List RS= (AT(MAVG(GP_GB, 5)/((2*PI*F_GB)*MAVG(CP_GB, 5)), MAXPOS(MAVG(CP_GB, 5))))^2/((1+(AT(MAVG Formulator

	Cp_GB	Gp_GB	DCV_GB	F_GB	RS	AR	CADJ	COX	CMIN	INVCSQR	TOX
1	3.4645E-9	36.4846E-6	-3.0000E+0	30.0000E+3	85.3264E+0	-19.4742E-9	3.4754E-9	3.4698E-9	90.0692E-12	#REF	
2	3.4633E-9	36.4740E-6	-2.9800E+0	30.0000E+3		-4.7268E-9	3.4741E-9			#REF	
3	3.4621E-9	36.4524E-6	-2.9600E+0	30.0000E+3		158.2666E-12	3.4729E-9			82.9086E+15	
4	3.4609E-9	36.4374E-6	-2.9400E+0	30.0000E+3		10.4458E-9	3.4717E-9			82.9667E+15	
5	3.4597E-9	36.4159E-6	-2.9200E+0	30.0000E+3		13.5522E-9	3.4705E-9			83.0257E+15	
6	3.4585E-9	36.3938E-6	-2.9000E+0	30.0000E+3		17.2661E-9	3.4693E-9			83.0848E+15	
7	3.4572E-9	36.3689E-6	-2.8800E+0	30.0000E+3		19.1980E-9	3.4680E-9			83.1443E+15	
8	3.4559E-9	36.3514E-6	-2.8600E+0	30.0000E+3		28.4679E-9	3.4667E-9			83.2056E+15	
9	3.4547E-9	36.3206E-6	-2.8400E+0	30.0000E+3		23.3835E-9	3.4655E-9			83.2676E+15	
10	3.4534E-9	36.3083E-6	-2.8200E+0	30.0000E+3		39.6584E-9	3.4641E-9			83.3307E+15	
11	3.4521E-9	36.2819E-6	-2.8000E+0	30.0000E+3		40.3526E-9	3.4628E-9			83.3955E+15	
12	3.4507E-9	36.2581E-6	-2.7800E+0	30.0000E+3		45.5286E-9	3.4614E-9			83.4610E+15	
13	3.4493E-9	36.2374E-6	-2.7600E+0	30.0000E+3		55.0267E-9	3.4600E-9			83.5275E+15	
14	3.4480E-9	36.2034E-6	-2.7400E+0	30.0000E+3		48.0724E-9	3.4587E-9			83.5952E+15	
15	3.4465E-9	36.1833E-6	-2.7200E+0	30.0000E+3		58.5557E-9	3.4572E-9			83.6643E+15	
16	3.4451E-9	36.1589E-6	-2.7000E+0	30.0000E+3		63.6099E-9	3.4558E-9			83.7338E+15	
17	3.4436E-9	36.1332E-6	-2.6800E+0	30.0000E+3		69.5090E-9	3.4543E-9			83.8057E+15	
18	3.4421E-9	36.1037E-6	-2.6600E+0	30.0000E+3		70.9472E-9	3.4528E-9			83.8791E+15	
19	3.4406E-9	36.0822E-6	-2.6400E+0	30.0000E+3		81.4972E-9	3.4513E-9			83.9541E+15	
20	3.4390E-9	36.0475E-6	-2.6200E+0	30.0000E+3		80.0865E-9	3.4497E-9			84.0308E+15	
21	3.4375E-9	36.0144E-6	-2.6000E+0	30.0000E+3		79.6444E-9	3.4481E-9			84.1090E+15	
22	3.4358E-9	35.9866E-6	-2.5800E+0	30.0000E+3		86.8085E-9	3.4464E-9			84.1885E+15	
23	3.4342E-9	35.9480E-6	-2.5600E+0	30.0000E+3		82.0969E-9	3.4448E-9			84.2691E+15	
24	3.4325E-9	35.9198E-6	-2.5400E+0	30.0000E+3		88.1696E-9	3.4431E-9			84.3510E+15	

Run1 Calc Run Settings

Figure 13. Extracted C-V parameters shown in the Sheet

Oxide thickness

For a relatively thick oxide (>50Å), extracting the oxide thickness is fairly simple. The oxide capacitance (C_{OX}) is the high frequency capacitance when the device is biased for strong accumulation. In the strong accumulation region, the MOS-C acts like a parallel-plate capacitor, and the oxide thickness (T_{OX}) may be calculated from C_{OX} and the gate area using the following equation:

$$T_{OX(nm)} = \frac{(10^7)A\varepsilon_{OX}}{C_{OX}}$$

where:

T_{OX} = oxide thickness (nm)

A = gate area (cm²)

ε_{OX} = permittivity of the oxide material (F/cm)

C_{OX} = oxide capacitance (F)

10^7 = units conversion from cm to nm

Flatband capacitance and flatband voltage

Application of a certain gate voltage, the flatband voltage (V_{FB}), results in the disappearance of band bending. At this point, known as the flatband condition, the semiconductor band is said to become flat. Because the band is flat, the surface potential is zero (with the reference potential being taken as the bulk potential deep in the semiconductor). Flatband voltage and its shift are widely used to extract other device parameters, such as oxide charges.

V_{FB} can be identified from the C-V curve. One way is to use the flatband capacitance method. For this method, the ideal value of the flatband capacitance (C_{FB}) is calculated from the oxide capacitance and the Debye length. The concept of Debye length is introduced later in this section. Once the value of C_{FB} is known, the value of V_{FB} can be obtained from the C-V curve data, by interpolating between the closest gate-to-substrate (V_{GS}) values [2].

The Debye length parameter (λ) must also be calculated to derive the flatband voltage and capacitance. Based on the doping profile, the λ calculation requires one of the following doping concentrations: N at 90% of W_{MAX} (refer to Nicollian and Brews), a user-supplied N_A (bulk doping concentration for a p-type, acceptor, material), or a user-supplied N_D (bulk doping concentration for an n-type, donor, material).

NOTE: The flatband capacitance method is invalid when the interface trap density (D_{IT}) becomes very large (10^{12}–10^{13} or greater). However, the method should give satisfactory results for most users. When dealing with high D_{IT} values, consult the appropriate literature for a more suitable method.

The flatband capacitance is calculated as follows:

$$C_{FB} = \frac{C_{OX}(\varepsilon_S A/\lambda)(10^2)}{C_{OX} + (\varepsilon_S A/\lambda)(10^2)}$$

where:

C_{FB} = flatband capacitance (F)

C_{OX} = oxide capacitance (F)

ε_S = permittivity of the substrate material (F/cm)

A = gate area (cm^2)

10^2 = units conversion from m to cm

λ = extrinsic Debye length, which is calculated as follows:

$$l = \left(\frac{\varepsilon_S kT}{q^2 N}\right)^{1/2}(10^{-2})$$

where:

λ = extrinsic Debye length

ε_S = permittivity of the substrate material (F/cm)

kT = thermal energy at room temperature (293K) (4.046×10^{-21}J)

q = electron charge (1.60219×10^{-19}C)

$N_X = N$ at 90% W_{MAX} or N90W (refer to Nicollian and Brews; see References) or, when input by the user, $N_X = N_A$ or $N_X = N_D$

10^{-2} = units conversion from cm to m

The extrinsic Debye length is an idea borrowed from plasma physics. In semiconductors, majority carriers can move freely. The motion is similar to a plasma. Any electrical interaction has a limited range. The Debye length is used to represent this interaction range. Essentially, the Debye length indicates how far an electrical event can be sensed within a semiconductor.

Threshold voltage

The turn-on region for a MOSFET corresponds to the inversion region on its C-V plot. When a MOSFET is turned on, the channel formed corresponds to strong generation of inversion charges. It is these inversion charges that conduct current. When a source and drain are added to a MOS-C to form a MOSFET, a p-type MOS-C becomes an n-type MOSFET, also called an n-channel MOSFET. Conversely, an n-type MOS-C becomes a p-channel MOSFET.

The threshold voltage (V_{TH}) is the point on the C-V curve where the surface potential (ϕ_S) equals twice the bulk potential (ϕ_B). This curve point corresponds to the onset of strong inversion. For an enhancement-mode MOSFET, V_{TH} corresponds to the point where the device begins to conduct. The physical meaning of the threshold voltage is the same for both a MOS-C C-V curve and a MOSFET I-V curve. However, in practice, the numeric V_{TH} value for a MOSFET may be slightly different due to the particular method used to extract the threshold voltage.

The threshold voltage of a MOS capacitor can be calculated as follows:

$$V_{TH} = V_{FB} \pm \left[\frac{A}{C_{OX}} \sqrt{4\varepsilon_s q |N_{BULK}\phi_B|} + 2|\phi_B| \right]$$

where:

V_{TH} = threshold voltage (V)

V_{FB} = flatband potential (V)

A = gate area (cm^2)

C_{OX} = oxide capacitance (F)

ε_S = permittivity of the substrate material (F/cm)

q = electron charge (1.60219×10^{-19}C)

N_{BULK} = bulk doping (cm^{-3})(Note: The Formulator name for N_{BULK} is N90W.)

ϕ_B = bulk potential (V)(Note: The Formulator name for ϕ_B is PHIB.)

The bulk potential is calculated as follows:

$$\phi_B = - \frac{kT}{q} \ln \left(\frac{N_{BULK}}{N_i} \right) (DopeType)$$

where:

ϕ_B = bulk potential (V)(Note: The Formulator name for ϕ_B is PHIB.)

k = Boltzmann's constant (1.3807×10^{-23}J/K)

T = test temperature (K)

q = electron charge (1.60219×10^{-19}C)

N_{BULK} = Bulk doping (cm^{-3})(Note: The Formulator name for N_{BULK} is called N90W.)

N_i = Intrinsic carrier concentration ($1.45 \times 10^{10} cm^{-3}$)

DopeType = +1 for p-type materials and –1 for n-type materials

Metal-semiconductor work function difference

The metal-semiconductor work function difference (W_{MS}) is commonly referred to as the work function. It contributes to the shift in V_{FB} from the ideal zero value, along with the effective oxide charge [3][4]. The work function represents the difference in work necessary to remove an electron from the gate and from the substrate. The work function is derived as follows:

$$W_{MS} = W_M - \left[W_S + \frac{E_{BG}}{2} - \phi_B \right]$$

where:

W_{MS} = work function

W_M = metal work function (V)*

W_S = substrate material work function, electron affinity (V)*

E_{BG} = substrate material bandgap (V)*

ϕ_B = bulk potential (V)(Note: The Formulator name for ϕ_B is PHIB)

*The values for W_M, W_S, and E_{BG} are listed in the Formulator as constants. The user can change the values depending on the type of materials.

The following example calculates the work function for silicon, silicon dioxide, and aluminum:

$$W_{MS} = 4.1 - \left[4.15 + \frac{1.12}{2} - \phi_B \right]$$

Therefore,

$$W_{MS} = -0.61 + \phi_B$$

and

$$W_{MS} = -0.61 - \frac{kT}{q} \ln \left(\frac{N_{BULK}}{N_i} \right) (DopeType)$$

where:

W_{MS} = work function

k = Boltzmann's constant (1.3807×10^{-23}J/K)

T = test temperature (K)

q = electron charge (1.60219×10^{-19}C)

N_{BULK} = bulk doping (cm^{-3})

DopeType = +1 for p-type materials and –1 for n-type materials

For example, for an MOS capacitor with an aluminum gate and p-type silicon ($N_{BULK} = 10^{16} cm^{-3}$), W_{MS} = –0.95V. Also, for the same gate and n-type silicon ($N_{BULK} = 10^{16} cm^{-3}$), W_{MS} = –0.27V. Because the supply voltages of modern CMOS devices are lower than those of earlier devices and

because aluminum reacts with silicon dioxide, heavily doped polysilicon is often used as the gate material. The goal is to achieve a minimal work-function difference between the gate and the semiconductor, while maintaining the conductive properties of the gate.

Effective and total bulk oxide charge

The effective oxide charge (Q_{EFF}) represents the sum of oxide fixed charge (Q_F), mobile ionic charge (Q_M), and oxide trapped charge (Q_{OT}):

$$Q_{EFF} = Q_F + Q_M + Q_{OT}$$

Q_{EFF} is distinguished from interface trapped charge (Q_{IT}), in that Q_{IT} varies with gate bias and Q_{EFF} does not [5] [6]. Simple measurements of oxide charge using C-V measurements do not distinguish the three components of Q_{EFF}. These three components can be distinguished from one another by temperature cycling [7]. Also, because the charge profile in the oxide is not known, the quantity (Q_{EFF}) should be used as a relative, not an absolute, measure of charge. It assumes that the charge is located in a sheet at the silicon–silicon dioxide interface.

From Nicollian and Brews, Eq. 10.10, we have:

$$V_{FB} - W_{MS} = -\frac{Q_{EFF}}{C_{OX}}$$

where:

V_{FB} = flatband potential (V)

W_{MS} = metal-semiconductor work function (V)

Q_{EFF} = effective oxide charge (C)

C_{OX} = oxide capacitance (F)

Note that C_{OX} here is per unit of area. So that:

$$Q_{EFF} = \frac{C_{OX}(W_{MS} - V_{FB})}{A}$$

where:

Q_{EFF} = effective oxide charge (C)

C_{OX} = oxide capacitance (F)

W_{MS} = metal–semiconductor work function (V)

V_{FB} = flatband potential (V)

A = gate area (cm²)

For example, assume a 0.01cm², 50pF, p-type MOS-C with a flatband voltage of –5.95V; its N_{BULK} of 10^{16}cm^{-3} corresponds to a W_{MS} of –0.95 V. For this example, Q_{EFF} can be calculated to be 2.5×10^{-8}C/cm², which in turn causes the threshold voltage to shift ~5V in the negative direction. Note that in most cases where the bulk charges are positive, there is a shift toward negative gate voltages. The effective oxide charge concentration (N_{EFF}) is computed from effective oxide charge (Q_{EFF}) and the electron charge as follows:

$$N_{EFF} = \frac{Q_{EFF}}{q}$$

where:

N_{EFF} = effective oxide charge density (cm^{-2})

Q_{EFF} = effective oxide charge (C)

q = electron charge (1.60219×10^{-19}C)

Substrate doping concentration

The substrate doping concentration (N) is related to the reciprocal of the slope of the $1/C^2$ vs. V_G curve. The doping concentration is calculated and displayed below the graph in the *moscap-c-2vsv* test as follows:

$$N_{SUB} = \frac{2}{q\varepsilon_S A^2 \left(\frac{\Delta 1/C^2}{\Delta V_G}\right)}$$

where:

N_{SUB} = substrate doping concentration

q = electron charge (1.60219×10^{-19}C)

A = gate area (cm²)

ε_S = permittivity of the substrate material (F/cm)

V_G = gate voltage (V)

C = measured capacitance (F)

Doping concentration vs. depth (doping profile)

The doping profile of the device is derived from the C-V curve based on the definition of the differential capacitance as the differential change in depletion region charges produced by a differential change in gate voltage [8].

The standard doping concentration (N) vs. depth (w) analysis discussed here does not compensate for the onset of accumulation, and it is accurate only in depletion. This method becomes inaccurate when the depth is less than two Debye lengths. The doping concentration used in the doping profile is calculated as:

$$N = \left| \frac{-2}{q\varepsilon_s A^2 \frac{d(1/C^2)}{dV}} \right|$$

The *moscap-dopingprofile* test computes the depletion depth (w) from the high frequency capacitance and oxide capacitance at each measured value of the gate voltage (V_G) [9]. The Formulator computes each (w) element of the calculated data array as shown:

$$W = A\varepsilon_S \left(\frac{1}{C} - \frac{1}{C_{OX}} \right) (10^2)$$

where:

W = depth (m)

A = the gate area (cm²)

C = the measured capacitance (F)

ε_S = the permittivity of the substrate material (F/cm)

C_{OX} = the oxide capacitance (F)

10^2 = units conversion from cm to m

Once the doping concentration and depletion depth are derived, a doping profile can be plotted. This is done in the Graph of the *MOS Capacitor Doping Profile* (*moscap-dopingprofile)* test.

Summary

When equipped with the 4210-CVU or 4215-CVU option, the 4200A-SCS is a very useful tool for making both C-V and I-V measurements on MOS capacitors and deriving many of the common MOS parameters. In addition to the *MOS Capacitor C-V Project*, the 4200A-SCS includes other projects specifically for testing MOS capacitors. The *MOS Capacitor Lifetime Test Project* is used for determining generation velocity and lifetime testing (Zerbst plot) of MOS capacitors. *The MOS Capacitor Mobile Ion Project* determines the mobile charge of a MOS cap using the bias-temperature stress method. In addition to making C-V measurements, the SMUs can make I-V measurements on MOS caps, including leakage current and breakdown testing.

References

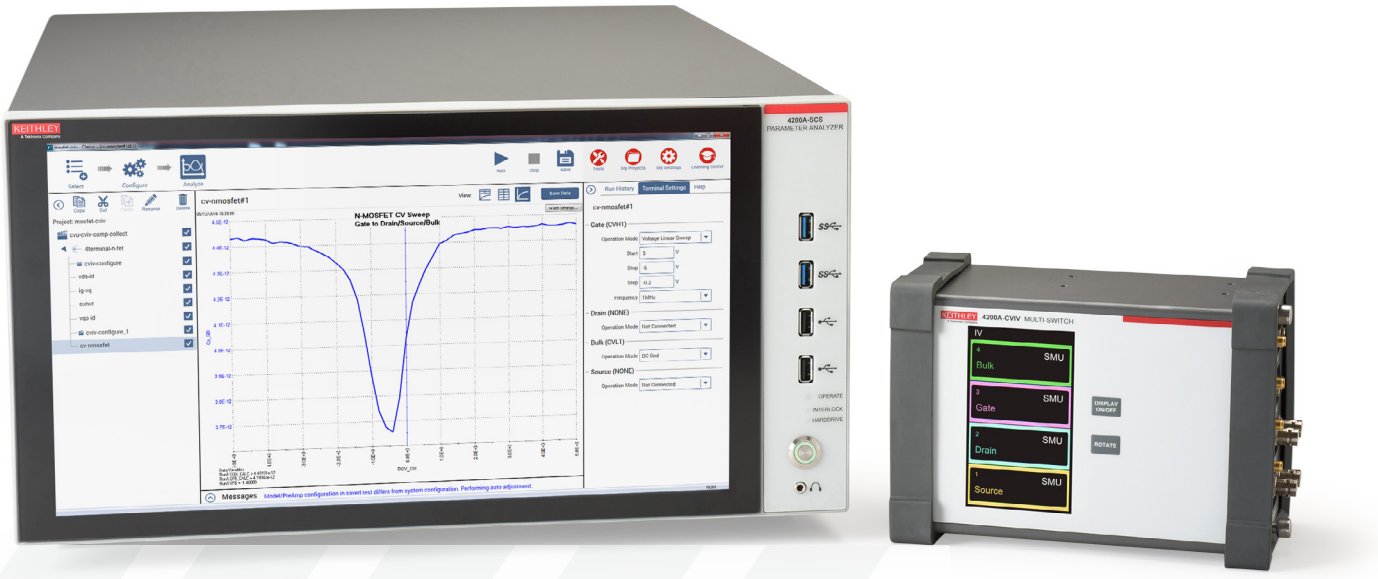
1. E. H. Nicollian and J. R. Brews, *MOS Physics and Technology* (New York: Wiley, 1982), 224.
2. *Ibid.*, 487–488
3. Nicollian and Brews, 462–477.
4. S.M. Sze, *Physics of Semiconductor Devices*, 2nd edition. (New York: Wiley, 1985), 395–402.
5. Nicollian and Brews, 424–429.
6. Sze, 390–395.
7. Nicollian and Brews, 429 (Figure 10.2).
8. Nicollian and Brews, 380–389.
9. Nicollian and Brews, 386.

Additional Suggested Reading

D.K. Schroder, *Semiconductor Material and Device Characterization*, 2nd edition. (New York, Wiley, 1998).

Tektronix®

Switching Between C-V and I-V Measurements Using the 4200A-CVIV Multi-Switch and 4200A-SCS Parameter Analyzer



Introduction

Full parametric characterization of a semiconductor device usually requires an array of tests to gather all of the device's important parameters. Current-voltage (I-V) tests are used to determine device parameters like transfer characteristics, leakages, and breakdown voltages. Capacitance-voltage (C-V) tests are used to determine device parameters like doping concentrations, interface charges, and threshold voltages. It is very common to perform both I-V and C-V tests on the same device, but the two test types require different test equipment and cabling. These differences make it difficult to perform I-V and C-V measurements on the same device quickly because changing test types typically requires recabling
the entire system.

When configured with 4200-SMU, 4201-SMU, 4210-SMU, or 4211-SMU Source Measure Units (SMUs) and the 4210-CVU or 4215-CVU Capacitance Voltage Unit, the 4200A-SCS Parameter Analyzer is capable of performing both I-V and C-V measurements. However, the SMUs use triaxial cables and the CVU uses SMA coaxial cables. Combining the 4200A-SCS Parameter Analyzer with the 4200A-CVIV Multi-Switch eliminates these difficulties because the 4200A-CVIV is capable of switching between I-V and C-V measurements with no need to change cables or lift probe tips. The 4200A-CVIV is shown in **Figure 1**. The Clarius software that runs on the 4200A-SCS makes it simple to control the Multi-Switch and creates a faster, more efficient device testing workflow for any application that requires making I-V and C-V

Figure 1. 4200A-CVIV Multi-Switch.

measurements on the same device.

Note: Although this application note describes I-V and C-V switching with the 4200A-SCS, beginning with Clarius V1.4 or higher, each CVIV channel can be used as a bias tee by combining the CVU measurements with the SMU bias. With the bias tee capability, C-V measurements can be made at ±200 V or 400 V differential.

4200A-CVIV Operation

The 4200A-CVIV Multi-Switch is a four-channel multiplexed switching accessory for the 4200A-SCS that allows users to switch seamlessly between I-V and C-V measurements. It accepts four SMUs, one for each channel, and one CVU as inputs. Changing the output mode for each of the four channels reconfigures the internal switches of the 4200A-CVIV to route the desired signals to the output terminals. **Figure 2** shows a simplified I-V and C-V switching diagram of the 4200A-CVIV.

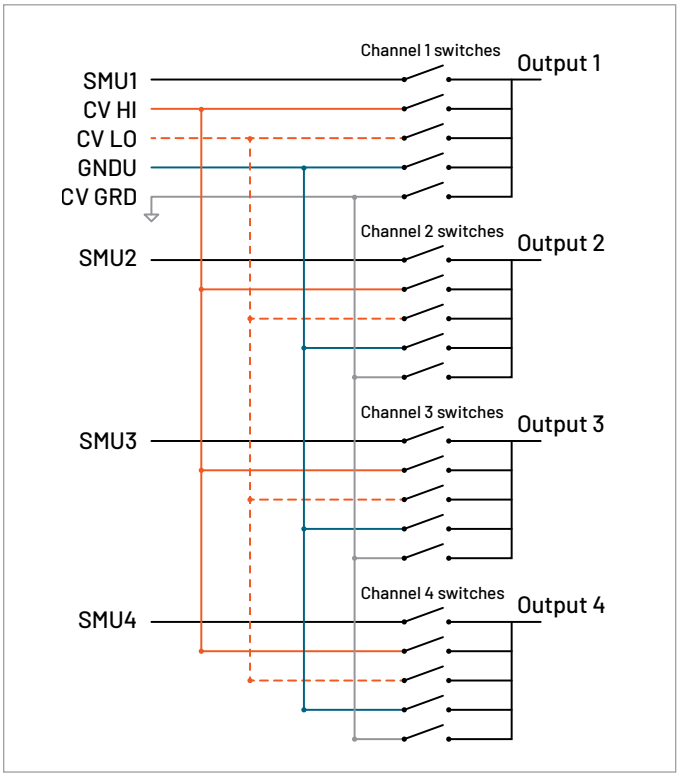


Figure 2. A simplified switching diagram for the 4200A-CVIV. All of the channels are shown in two-wire mode and in the OPEN position.

The 4200A-CVIV has six different output modes for each channel used for I-V and C-V switching. (There are additional output modes used for bias tee operation). The I-V and C-V switching output modes are described as follows:

- **SMU** – The SMU signal paths in the 4200A-CVIV are not multiplexed and cannot be switched between channels. Each SMU channel is directly associated with the channel to which it is connected. For example, setting Channel 3 to **SMU** will pass the signal from the SMU connected to Channel 3 to the output terminals for Channel 3.
- **CV HI and CV LO** – The CVU signal path in the 4200A-CVIV is fully multiplexed and can be assigned to any of the output channels. **CV HI or CV LO** can be assigned to any channel or any combination of channels to perform the desired C-V measurement. For example, setting Channel 1 to **CV HI** and Channels 2 and 3 to **CV LO** will configure the Multi-Switch to perform a C-V measurement on the device connected between Channel 1 and Channels 2/3.
- **CV GUARD** – This mode of the 4200A-CVIV can be used to remove undesired capacitances from C-V measurements. The CVU guard is the outside shield of the CVU coaxial cable. For example, setting Channel 4 to **CV GUARD** will configure the Multi-Switch to guard out capacitance from the device terminal connected to Channel 4.
- **GNDU** – The ground unit can be switched to any one of the four output channels. NOTE: Must have 4200A-CVIV Hardware Version 2.0 or higher and Clarius V1.4 or higher.
- **OPEN** – Configuring any channel to **OPEN** will open all of the output relays connected to that channel.

The 4200A-CVIV is controlled using the Clarius software application that comes with the 4200A-SCS Parameter Analyzer. Switch configurations are controlled by placing the *cviv-configure* Action from the Action Library into the project tree.

The *cviv-configure* Action is used to switch the channel output configuration, two-wire/four-wire CVU setting, and the names of the test and channels to be shown on the 4200A-CVIV display. A *cviv-configure* Action must be used any time the configuration of the 4200A-CVIV needs to change. **Figure 3** shows an example of the *cviv-configure* Action populated with settings to switch the CVU output terminals to a MOSFET.

The *cvu-cviv-comp-collect* Action performs CVU connection compensation through a 4200A-CVIV on a user-defined configuration. Open, Short, and Load correction compensations can be acquired. Connection

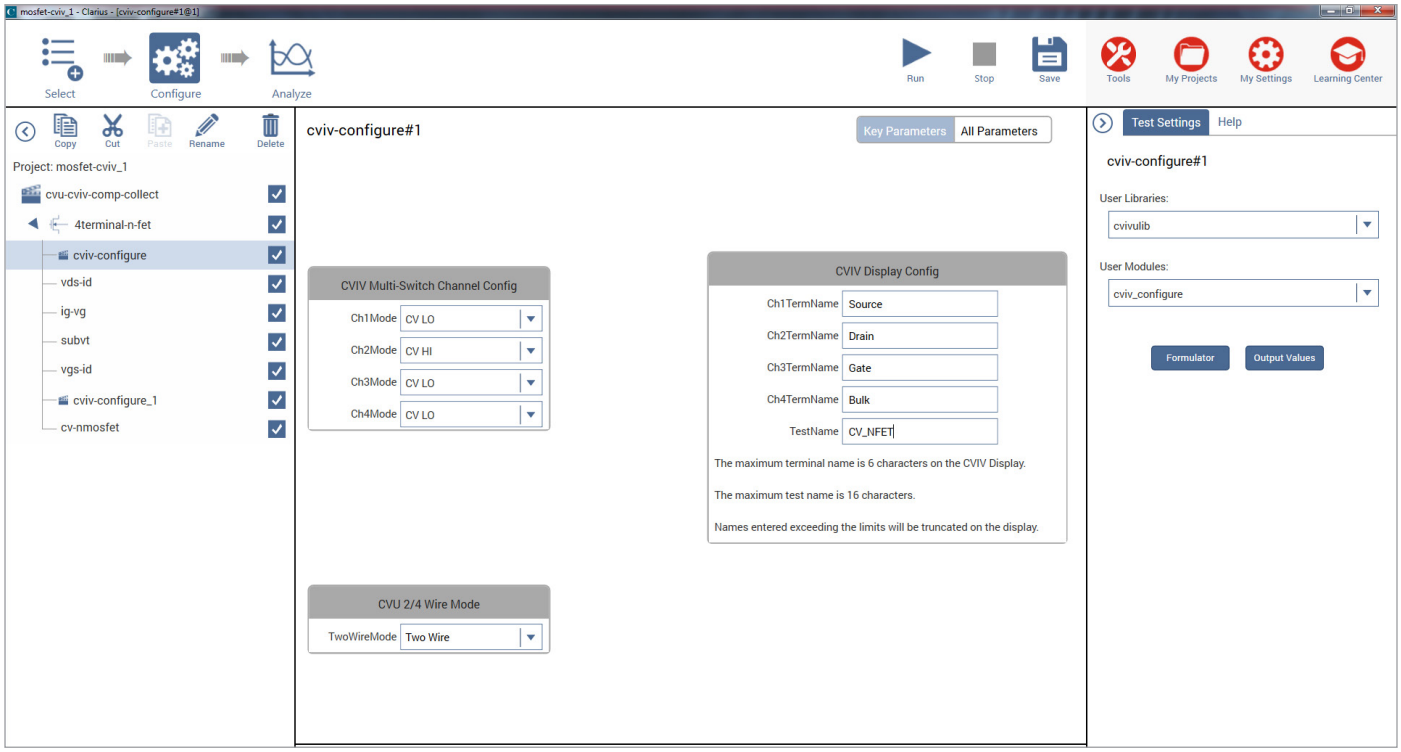


Figure 3. The *cviv-configure* Action options.

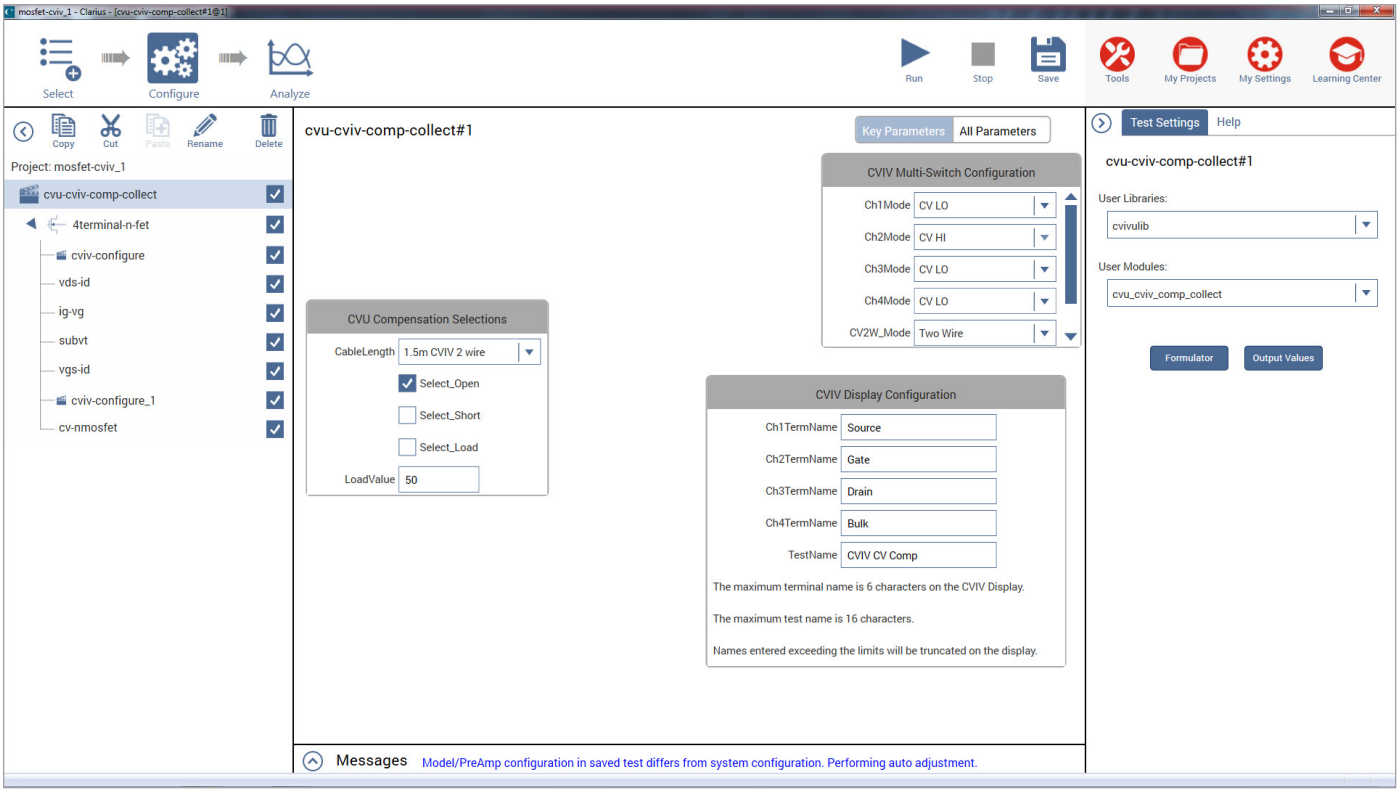


Figure 4. The *cvu-cviv-comp-collection* Action configured to perform an Open Compensation.

compensation corrects for offset and gain errors caused by the connections between the CVU and the device under test. The compensation for each particular switch configuration is automatically stored so that when a particular configuration is recalled using the *cviv-configure* Action, the compensation will automatically be applied if it is enabled within a C-V measurement test. **Figure 4** shows the *cvu-cviv-comp-collect* Action setup to perform an Open compensation.

Figure 5 shows a screen capture of a project called *Diode Tests* that is used to make I-V and C-V measurements on a diode that is connected to the outputs of Channels 1 and 2. First, compensation is performed using the *cvu-cviv-comp-collect* Action. Then the *cviv-configure-iv* Action connects SMU1 and SMU2 to Channels 1 and 2 so that the forward and reverse I-V measurements can be made in the two tests that follow. When the *cviv-configure-cv* Action is executed, the SMUs are disconnected from the outputs and the CVU HI and LO terminals are connected to Channels 1 and 2. Finally, a C-V sweep is made on the diode.

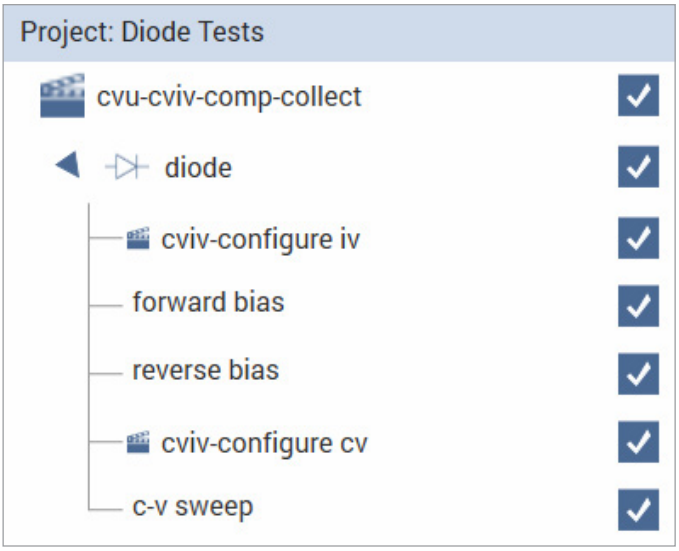


Figure 5. The project tree structure for a diode test that uses the 4200A-CVIV to switch between I-V and C-V measurements

C-V/I-V Switching for Device Characterization

Both I-V and C-V measurements play a role in the parametric characterization of semiconductor devices. Two-terminal devices require simple I-V sweeps to characterize their DC performance and C-V sweeps to determine the capacitance between their two terminals at different bias levels. For example, full characterization of a diode requires I-V measurements to acquire the forward I-V curve, reverse leakage curve, and reverse breakdown voltage. C-V measurements are used to acquire the diode's doping profile and charge density information.

Two-terminal Devices

Two channels of the 4200A-CVIV are used to connect to the diode for I-V and C-V measurements. Since diodes have very low impedance forward active characteristics, it's best practice to perform measurements in four-wire mode to prevent measurement inaccuracies due to losses in cabling. Four-wire mode, also called remote sense, forces a test current through one set of cables and measures a voltage directly at the device under test with another set of cables. This technique helps remove the effects of cable impedance from the measurements.

Figure 6 shows the device connections and 4200A-CVIV settings for an I-V test on a diode. All of the DC I-V characteristics of the diode are collected in this configuration. The connections to the diode are made with triaxial cables, Model 4200-TRX-.75 (75cm or approximately 30 inches). These shielded cables are used to ensure that both very low current I-V measurements and high frequency AC measurements can be made with high accuracy. The device can be a packaged part in a test fixture or located directly on a wafer in a probe station.

The gray capacitor in **Figure 6** (C_d) is the parasitic capacitance of the PN junction. The I-V test does not provide information about this parasitic capacitance. A C-V test is necessary to characterize the capacitance of the device. **Figure 7** shows the device connections and 4200A-CVIV settings for a C-V test on a diode. All of the connections are identical to the I-V test. When the *cviv-configure* Action is executed in the Clarius software, the output is switched from the SMUs to the CVU terminals.

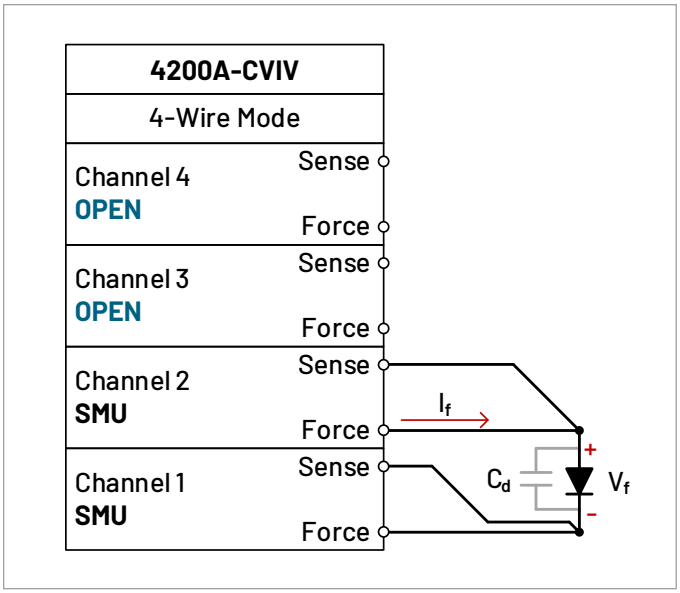


Figure 6. Configuration for I-V characterization of a diode using the 4200A-CVIV.

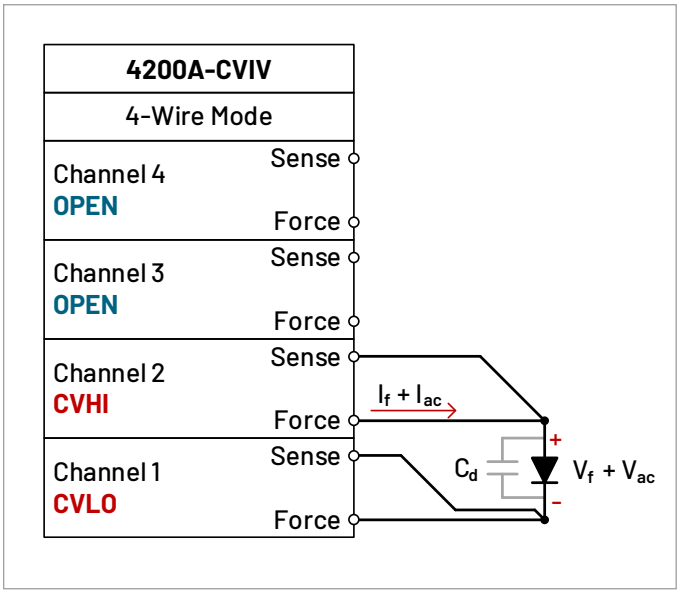


Figure 7. Configuration for C-V characterization of a diode using the 4200A-CVIV.

Three-terminal Devices

Three-terminal devices require more complicated I-V characterization and often capacitance measurements between multiple combinations of terminals. For example, bipolar junction transistors (BJTs) are three-terminal devices that require multiple SMUs to measure their transfer characteristics and produce useful data, such as Gummel plots. The 4200A-CVIV, when coupled with three SMUs and one CVU in the 4200A-SCS, can make these measurements.

Figure 8 shows the device connections, and 4200A-CVIV settings, for an I-V test on a BJT. The configuration is shown in two-wire mode, also known as local sense, but remote sensing should be used for high current BJTs. All of the connections to the BJT are made with the 4200-TRX-.75 triaxial cables. The device can be a packaged part in a test fixture or located directly on a wafer in a probe station.

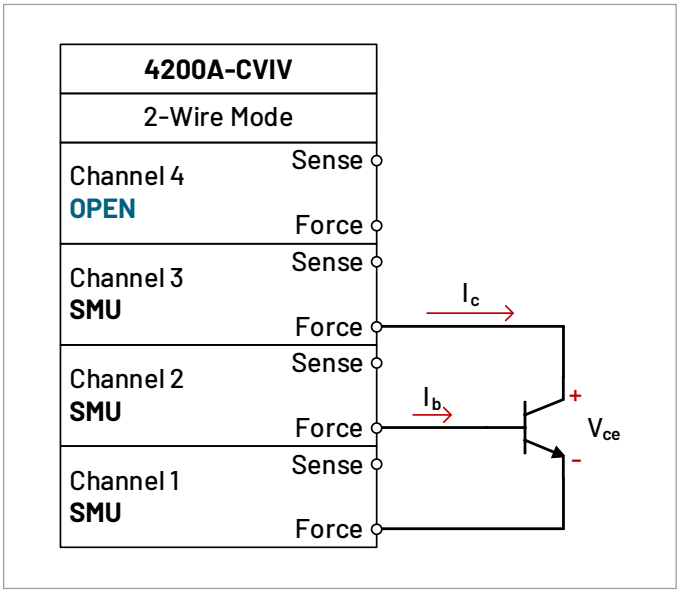


Figure 8. Configuration for I-V characterization of a BJT using the 4200A-CVIV.

Once the I-V measurements are complete, the 4200A-CVIV can be seamlessly switched to measure the parasitic capacitances of the BJT junctions without changing cables or removing connections to the device. **Figure 9** shows the parasitic capacitances between the BJT's terminals to be measured.

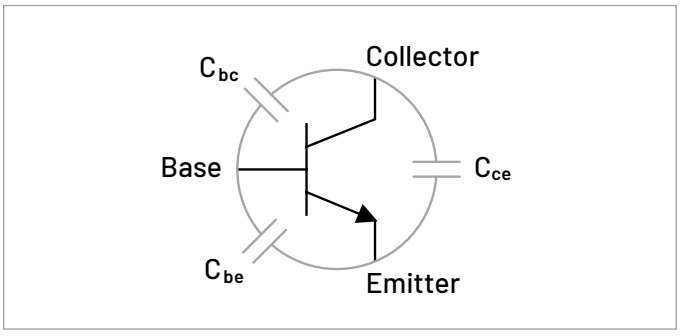


Figure 9. Parasitic capacitances of a bipolar junction transistor (BJT).

To measure the capacitance between two terminals, it is necessary to guard the third terminal to remove the effects of the additional parasitic capacitors. F or example, to measure the base-emitter capacitance (C_{be}), the collector is connected to guard. The 4200A-CVIV provides this guard signal with the CV GUARD setting. **Figure 10** shows the *cviv-configure* settings that instruct the 4200A-CVIV to use the CV GUARD signal. In this example, the CV HI terminal is connected to base (b) through Channel 2, CV LO is connected to the emitter (e) through Channel 1, and CV GUARD is connected to the collector (c) through Channel 3.

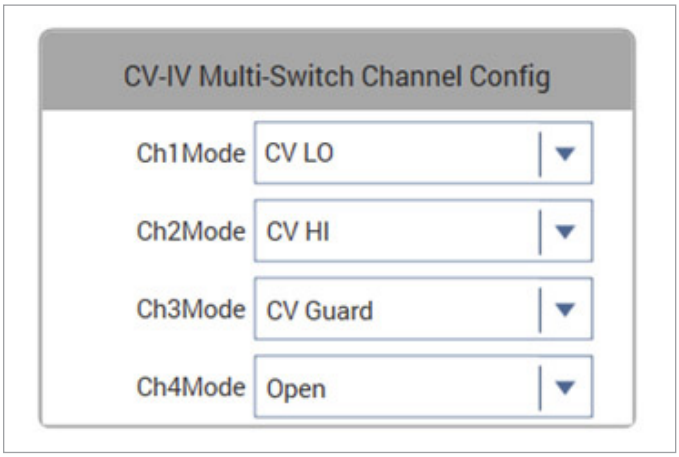


Figure 10. *cviv-configure* settings for a base-emitter capacitance measurement on a BJT.

Figure 11 shows the device connections, and 4200A-CVIV settings, for a guarded capacitance measurement on the C_{be} of a BJT.

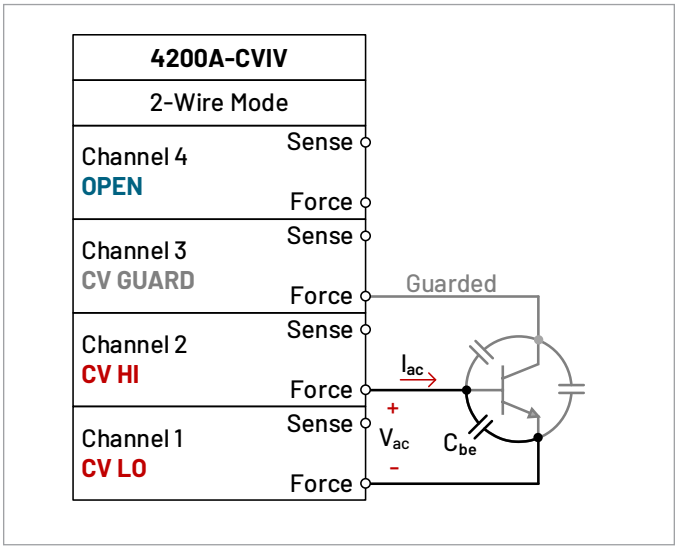


Figure 11. Base-emitter capacitance measurement on a BJT using the 4200A-CVIV.

The same technique is used to measure the base-collector capacitance or the collector-emitter capacitance of the BJT. The 4200A-CVIV can be controlled by the Clarius software to make all of these measurements automatically without moving cables between the terminals. The Clarius software includes a project (*cvu-bjt-cviv*) that is configured to measure these three parasitic capacitances present in a BJT using the CVU and the 4200A-CVIV to switch the CVU between terminals of the device.

Four-terminal Devices

Four-terminal devices, such as a MOSFET with a separate bulk connection, have more terminal-to-terminal parasitic capacitances, and more potential I-V and C-V measurement combinations than lower terminal count components. The 4200A-CVIV, when fully configured with four SMUs and one CVU, addresses these measurements with flexible configurability.

Figure 12 shows the device connections, and 4200A-CVIV settings, for an I-V test on a four-terminal MOSFET. The configuration is shown in two-wire mode, also known as local sense, but remote sensing should be used for high current MOSFETs. All of the connections to the MOSFET are made with 4200-TRX-.75 triaxial cables. The device can be a packaged part in a test fixture or located directly on a wafer in a probe station.

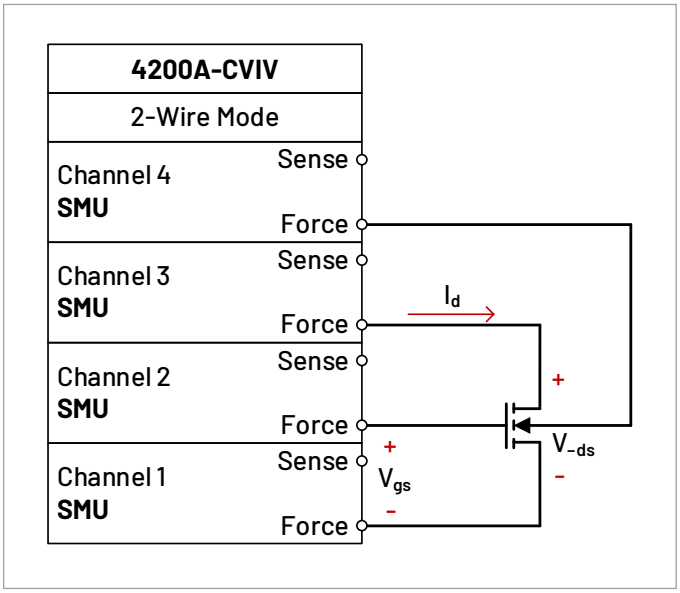


Figure 12. I-V characterization of a four-terminal MOSFET using the 4200A-CVIV.

Capacitance measurements are often made on MOSFETs to explore their basic operation and various parameters. Given that the high frequency operation and switching speeds of a MOSFET are dependent on the capacitance of the device, capacitance measurements are often made on various parasitic capacitances of the device, as shown in **Figure 13**. For example, the capacitance between the gate and channel (C_{gd} and C_{gs}) is important because it creates the charges necessary for operating the devices. This gate-channel capacitance depends on the applied voltage and the operating region.

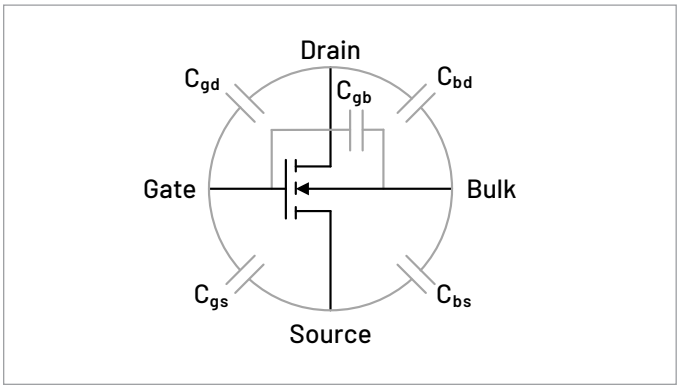


Figure 13. Parasitic capacitances of a MOSFET.

The C-V characteristics of the capacitor formed between the gate and the source, drain, and bulk of the MOSFET structure can be used to determine characteristics of the MOSFET like the threshold voltage, oxide thickness, oxide capacitance, and doping density. **Figure 14** shows the most common way of configuring this measurement. The source, drain, and bulk terminals are physically tied together and a C-V sweep is performed between the gate and the other three terminals.

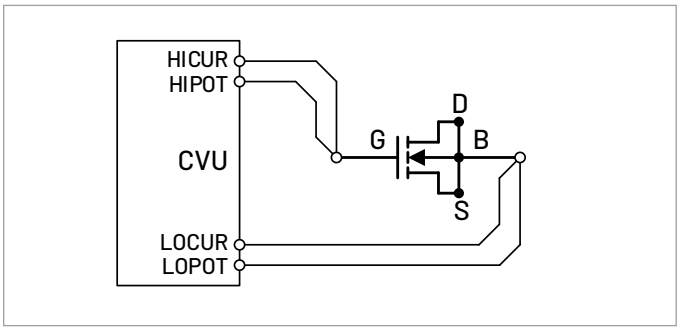


Figure 14. C-V test configuration for a MOSFET.

The CVHI, CVLO, and CV GUARD signals of the 4200A-CVIV can each be assigned to more than one pin at a time. This removes the need to tie the source, drain, and bulk together physically at the device to perform this measurement; instead, the connections are made internal to the 4200A-CVIV. **Figure 15** shows the device connections, and 4200A-CVIV settings, for this C-V test on a four-terminal MOSFET. Channels 1, 3, and 4 are all assigned to CVLO in this configuration. **Figure 16** shows the equivalent circuit of this 4200A-CVIV configuration.

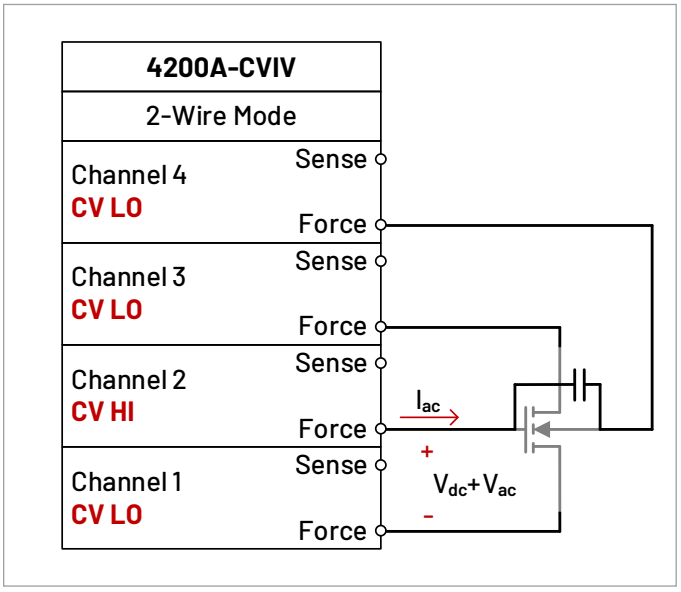


Figure 15. C-V characterization of a four-terminal MOSFET using the 4200A-CVIV.

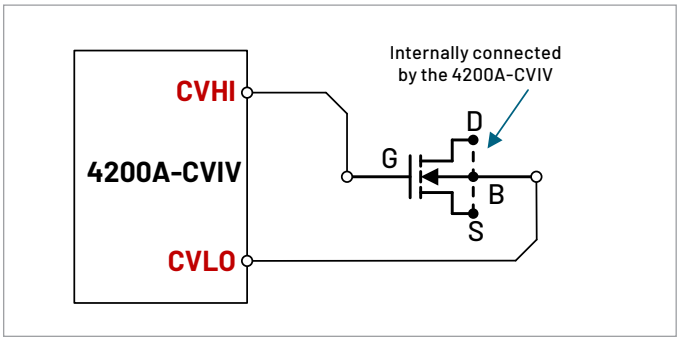


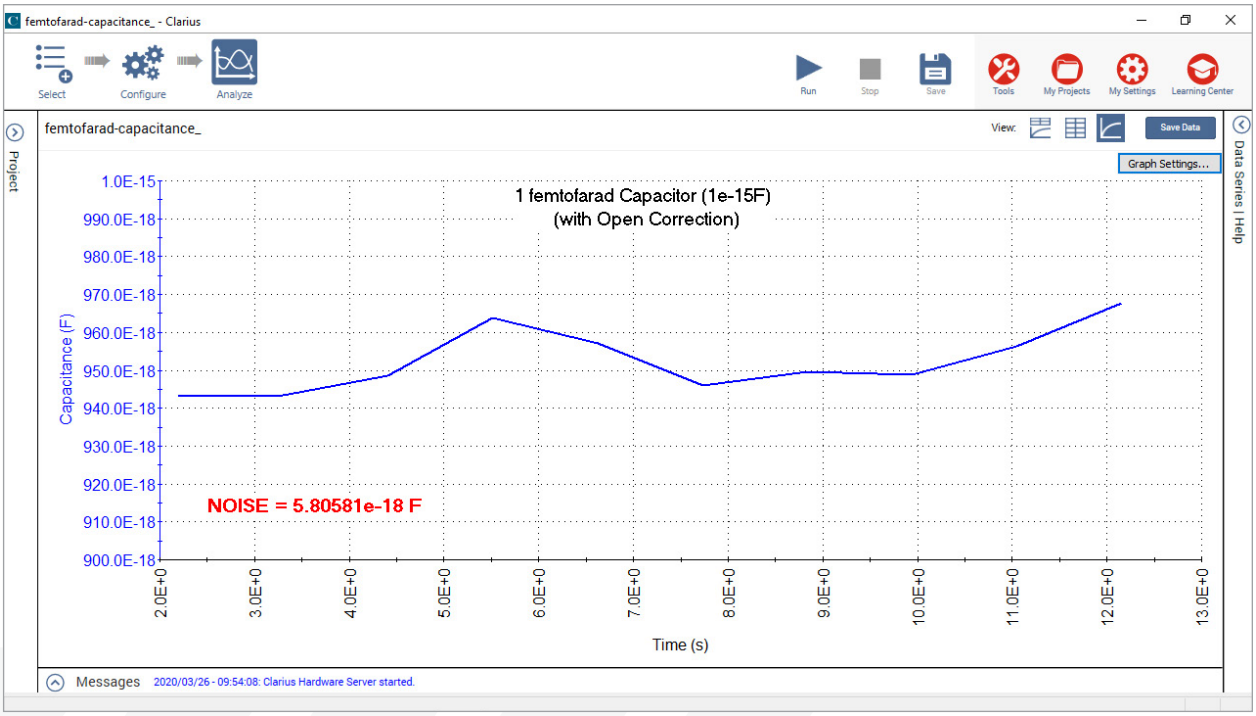
Figure 16. 4200A-CVIV two-terminal MOSFET C-V test equivalent circuit.

Conclusion

The 4200A-CVIV Multi-Switch makes it easy to perform I-V and C-V measurements on the same device without the need to change cables, which could potentially introduce errors or damage devices. The 4200A-SCS and Clarius software make it simple to control the 4200A-CVIV and integrate C-V and I-V testing together into a single project that executes seamlessly and continuously.

Tektronix®

Making Femtofarad (1e-15F) Capacitance Measurements with the 4215-CVU Capacitance Voltage Unit



Introduction

Typical semiconductor capacitances are in the picofarad (pF) or nanofarad (nF) ranges. Many commercially available LCR or capacitance meters can measure these values using proper measurement techniques including compensation. However, some applications require very sensitive capacitance measurements in the femtofarad (fF), or 1e-15, range. These applications include measuring metal-to-metal capacitance, interconnect capacitance on a wafer, MEMS devices such as switches, or capacitance between terminals on nano devices. These very small capacitances are very difficult to measure without using the proper instrumentation and measurement techniques.

Using a tool such as the Keithley 4200A-SCS Parameter Analyzer equipped with the optional 4215-CVU Capacitance Voltage Unit (CVU) enables the user to measure a wide range of capacitances, including very low values of capacitance, <1 pF. The CVU is designed with unique circuitry and is controlled by the Clarius+ software to support features and diagnostic tools that ensure the most accurate results. Using this CVU with proper techniques can enable the user to achieve very low capacitance measurements with tens of attofarads (1e-18F) noise levels.

This application note explains how to make femtofarad capacitance measurements using the 4215-CVU Capacitance Voltage Unit. This includes making proper connections and using the proper test settings in the Clarius software for the best results. Further information on making capacitance measurements, including cabling and connections, timing settings, guarding, and compensation, can be found in the Keithley application note, ***Making Optimal Capacitance and AC Impedance Measurements with the 4200A-SCS Parameter Analyzer.***

Making Connections to the Device

Making the proper connections to the device under test (DUT) is crucial for making sensitive low capacitance measurements.

For the best results, use only the supplied red SMA cables for making connections from the CVU to the DUT. The red SMA cables have characteristic impedance of 100 Ω. Two 100 Ω cables in parallel have characteristic impedance of 50 Ω, which is standard for high frequency sourcing and measuring applications. The supplied accessories allow connecting to a test fixture or prober with BNC or SMAs connections. Using the supplied torque wrench, tighten the SMA cable connections to ensure good contacts.

The CVU configured for two-wire sensing is shown in **Figure 1**. The HCUR and HPOT terminals are connected to a BNC tee to form CVH (HI), and the LCUR and LPOT terminals are connected to form CVL (LO).

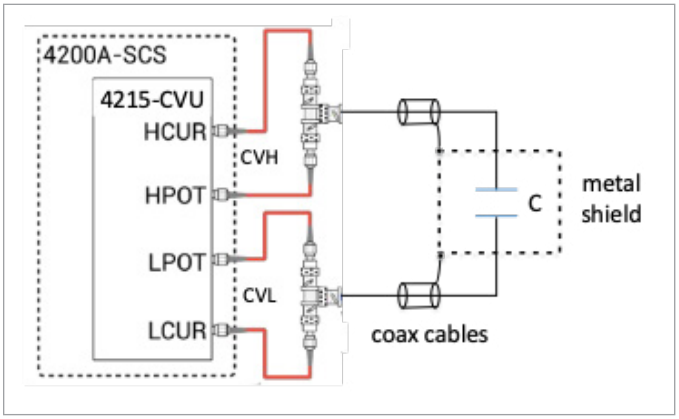


Figure 1. CVU connections for two-wire sensing.

An example of four-wire sensing to the DUT is shown in **Figure 2**. In this case, the HCUR and HPOT terminals are connected to one end of the device, and the LPOT and LCUR terminals are connected to the other end of the device. Four-wire connections to the device facilitate sensitive measurements by measuring the voltage as close as possible to the device.

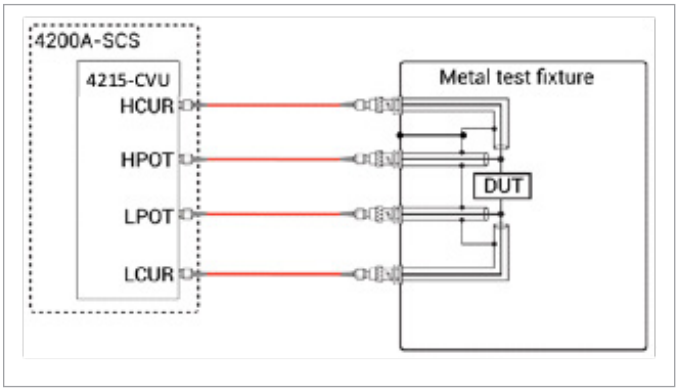


Figure 2. CVU connections for four-wire sensing.

For either two- or four-wire sensing, the outside shields of the coax cables must be connected as close as possible to the device to minimize the loop area of the shields. This reduces the inductance and helps to avoid resonance effects, which can be burdensome at frequencies higher than 1 MHz.

Keep all cables securely mounted to avoid any movement. Any movement that occurs in the time between executing the offset measurements and the actual DUT measurements can slightly change the loop inductance and impact the compensated data.

When measuring very small capacitances, shielding the DUT becomes important to reduce measurement uncertainties due to interference. Sources of interference could be AC signals or even physical movement. The metal shield should enclose the DUT and be connected to the outside shell of the coax cables.

For low capacitance measurements, it is best to use four-wire sensing, however, optimal measurements with two-wire sensing is achievable if the cables are short and compensation is used.

Configuring the Clarius+ Software for Femtofarad Measurements

Setting up the measurements in the Clarius software involves selecting the femtofarad project in the Library, configuring the test settings, and executing the measurements.

Selecting the *femtofarad-capacitance* Project in the Library

A project for making very small capacitance measurements is included in the Projects Library in the Clarius software. From the Select view, type in "femtofarad" in the search bar. The ***femtofarad-capacitance*** project will appear in the window as shown in **Figure 3**. Select Create to open the project in the project tree.

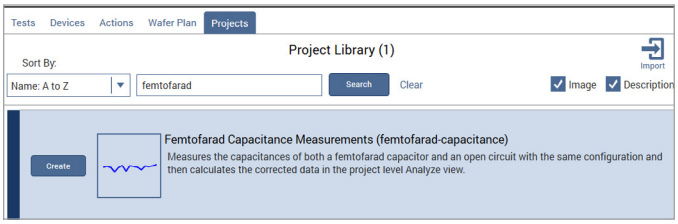


Figure 3. Femtofarad capacitance measurement project in Library.

Configuring the test settings

Once the project is created, the ***femtofarad-capacitance*** project appears in the project tree as shown in **Figure 4**.

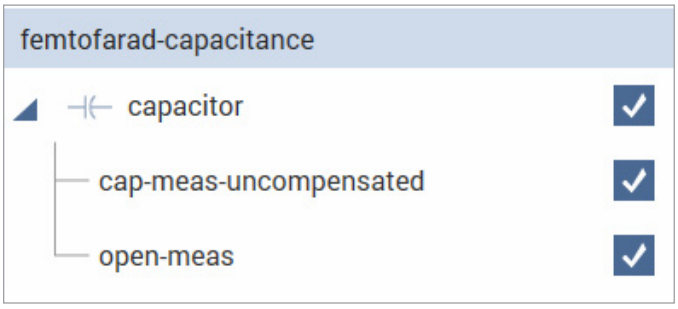


Figure 4. femtofarad-capacitance project tree.

This project has two tests: 1) the ***cap-measure-uncompensated*** test, which is used to measure the capacitance of the DUT and, 2) the ***open-meas*** test, which is used to acquire the capacitance of the cabling and connections. Because of the sensitivity of these capacitance measurements, the open circuit measurements are taken with the exact settings used to measure the DUT. The open circuit measurements are then

subtracted from the capacitance measurements of the DUT. This method enables good measurement results of extremely low capacitance.

For successful low capacitance measurements, it is important to adjust the measure and timing settings appropriately in the Configure view window. Here are some suggestions for making optimal adjustments:

Measure Settings: Some of the settings that the user can control are the current measure range, AC drive voltage, and the test frequency. These are important to the measurement because they are involved in the equation of determining the device capacitance. The CVU calculates the device capacitance from Iac, Vac, and the test frequency using the following equation:

$$C = \frac{Iac}{2\pi f Vac}$$

where: ***C*** = the device capacitance (F)
Iac = AC current measured by the CVU (A rms)
f = test frequency (Hz)
Vac = AC drive voltage (V rms)

By observing the relationship in these equations, the optimal settings for the current measure range, AC drive voltage, and test frequency can be deduced.

The CVU has three current measurement ranges: 1 µA, 30 µA, and 1 mA. For the lowest capacitance measurements with the least noise, use the lowest current range, the 1 µA range.

The level of the AC drive voltage can affect the signal-to-noise ratio of the measurement. While the AC noise level stays relatively constant, using a higher AC drive voltage generates a larger AC current, thus improving the signal-to-noise ratio. So, it's best to use an AC drive voltage as high as possible. In this project, a 1 V AC drive voltage was used.

For very low capacitance measurements, using a test frequency of about 1 MHz is ideal. With test frequencies much higher than 1 MHz, transmission line effects increase the difficulty in making successful measurements. At lower test frequencies, the measurements will lose resolution since the test frequency and current are proportional. Therefore, noisier measurements will result.

Timing Settings: The timing settings can be adjusted in the Test Settings window. The Speed mode setting enables the user to adjust the measurement window. For very low capacitance measurements, use the Custom Speed mode to set the measurement time to achieve the desired accuracy and noise levels. Basically, the longer the measurement time, or window, the less noisy the measurements will be. The noise is inversely proportional to the square root of the measurement time as shown in the following equation:

$$Noise = \frac{1}{\sqrt{MeasTime}}$$

The noise can be obtained by calculating the standard deviation of the capacitance measurements. This calculation can be done automatically using the Formulator in the Clarius software. The ***cap-meas-uncompensated*** test automatically calculates the noise and returns the value to the Sheet.

The measurement window can be adjusted using the Custom speed mode in the Test Settings window shown in **Figure 5**.

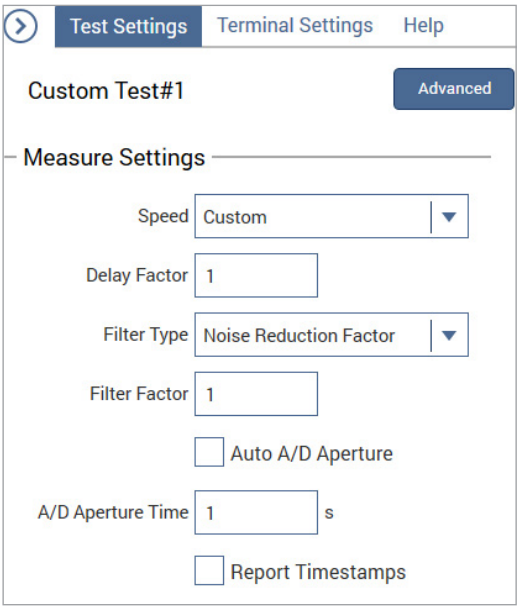


Figure 5. Custom Speed mode in Test Settings window.

The time of the measurement window can be calculated as follows:

Measurement Window = (A/D Aperture Time) * (FilterFactor² or Filter Count)

Table 1 lists the CVU noise as a function of the measure window generated with a 1 fF capacitor connected to the terminals of the CVU in a two-wire configuration. The noise was calculated by taking the standard deviation of 15 readings with measurements taken with settings of 0 V DC, 1 MHz, and 1 V AC drive voltage. This data verifies that as the measurement time increases the noise decreases. Notice that measurement times of 1 s and above have noise in the attofarad, or 1 E–18F, range. Experimentation may be required in each test environment to determine the optimal measurement time for a test.

Measurement Time (s)	Noise (rms)
0.001	1.18E-16
0.002	9.90E-17
0.005	9.17E-17
0.01	7.43E-17
0.02	6.84E-17
0.05	2.98E-17
0.1	2.24E-17
0.2	1.49E-17
0.5	1.15E-17
1	6.13E-18
2	5.00E-18
5	3.99E-18
10	2.77E-18

Table 1. Measurement Time vs Noise of 1 fF capacitor.

Executing the Measurements

Once the hardware and software are configured, the measurements can be executed. Ideally, the 4200A-SCS should be warmed up for at least one hour prior to taking measurements.

Follow these four steps to take compensated measurements and repeat the results.

1. **Measure the Capacitance of the Device.** Select the ***cap-meas-uncompensated*** test in the project tree. In the Configure view, adjust the test settings based on the device and application. Run the test.
2. **Measure the Open Circuit.** Select the ***open-meas*** test in the project tree. Adjust the test settings to be exactly like the test settings in the ***cap-meas-uncompensated*** test including the number of data points and voltage steps. Disconnect only the CVH (HCUR and HPOT) cables. Make sure the unterminated cables are capped. Run the open test.
3. **Analyze the Results.** Select the ***femtofarad-capacitance*** project in the project tree and select Analyze view. A screen capture displaying the compensated 1 fF measurements is shown in **Figure 6**.

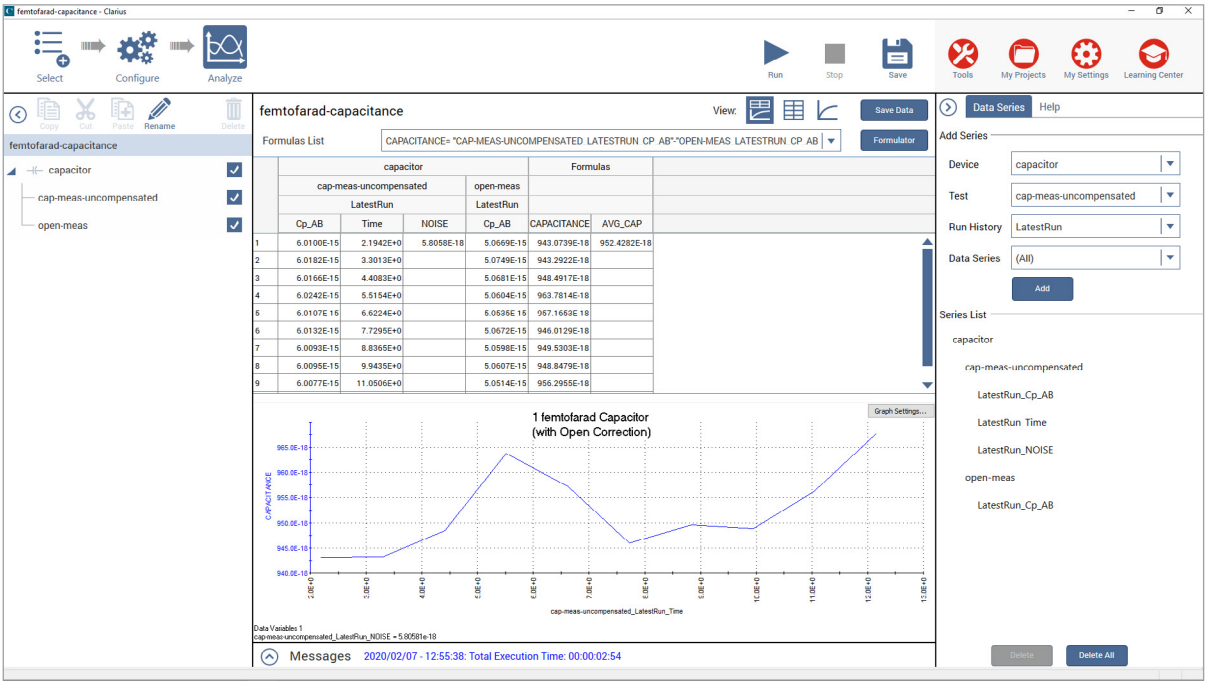


Figure 6. Screen capture of the Analyze view Sheet and Graph showing 1 fF measurement.

Notice the most recent capacitance and open measurements appear in the Sheet along with the noise calculation. The Data Series from all the tests in the project tree appear on the right-hand side of the screen. As shown in **Figure 7**, the Series List of the Latest Run measurements from the ***cap-meas-uncompensated*** and ***open-meas*** tests are selected. This means that each time the test is executed, the latest data will be populated in the Sheet.

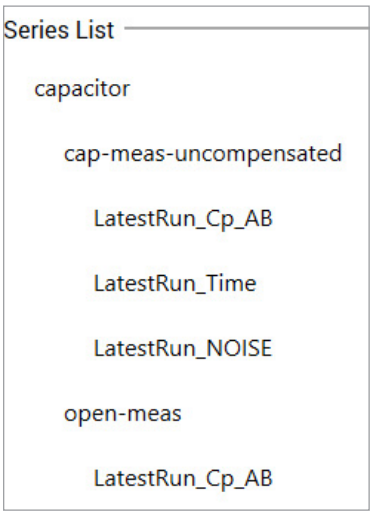


Figure 7. Data Series from tests.

A formula has been set up in the Formulator that automatically calculates the compensated capacitance measurements by subtracting the ***open-meas*** test data from the ***cap-meas-uncompensated*** test data in the Project level Analyze view Sheet. The graph displays the compensated capacitance as a function of time. The CAPACITANCE column in the Sheet lists the compensated measurements along with the average capacitance of all the readings. **Figure 8** shows the Latest Run Sheet data with the capacitance measurements (Cp-AB), time, noise, open measurements, compensated measurements (CAPACITANCE), and average capacitance (AVG_CAP).

	capacitor				Formulas	
	cap-meas-uncompensated			open-meas		
	LatestRun			LatestRun		
	Cp_AB	Time	NOISE	Cp_AB	CAPACITANCE	AVG_CAP
1	6.0100E-15	2.1942E+0	5.8058E-18	5.0669E-15	943.0739E-18	952.4282E-18
2	6.0182E-15	3.3013E+0		5.0749E-15	943.2922E-18	
3	6.0166E-15	4.4083E+0		5.0681E-15	948.4917E-18	
4	6.0242E-15	5.5154E+0		5.0604E-15	963.7814E-18	
5	6.0107E-15	6.6224E+0		5.0535E-15	957.1653E-18	
6	6.0132E-15	7.7295E+0		5.0672E-15	946.0129E-18	
7	6.0093E-15	8.8365E+0		5.0598E-15	949.5303E-18	
8	6.0095E-15	9.9435E+0		5.0607E-15	948.8479E-18	
9	6.0077E-15	11.0506E+0		5.0514E-15	956.2955E-18	
10	6.0222E-15	12.1576E+0		5.0544E-15	967.7908E-18	

Figure 8. Test data shown in the Analyze view Sheet.

4. **Repeating the measurements.** The measurements can be repeated from the project level by selecting Run. The compensated readings will automatically be calculated. However, the ***open-meas*** test must be unchecked as shown in **Figure 9**. Acquired open measurements should be repeated periodically if the data appears to move unexpectedly. This could indicate temperature variations or cable movements.

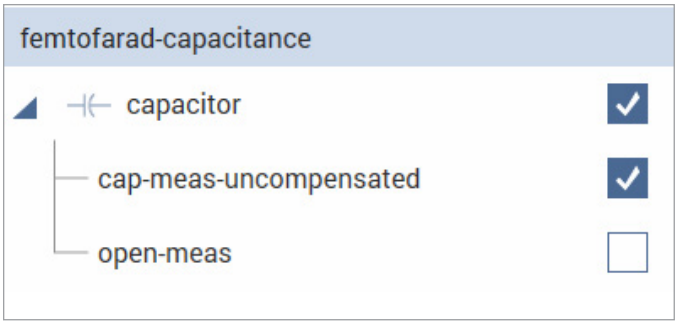


Figure 9. Uncheck the *open-meas* test to repeat measurements from the project level Analyze view.

Conclusion

Femtofarad level capacitances can be measured with the 4215-CVU using the Library project, proper connections, and appropriate measurement techniques and settings. Using the 4215-CVU with the appropriate measurement window can enable noise levels in the tens of attofarads range and below.

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Automating High and Low Frequency C-V Measurements and Interface Trap Density (DIT) Calculations of MOS Capacitors using the 4200A-SCS Parameter Analyzer

Introduction

Capacitance-voltage (C-V) measurements are commonly used in studying gate-oxide quality. These measurements are made on a two-terminal device called a MOS capacitor (MOS cap), which is basically a MOSFET without a source and drain. C-V test data on MOS capacitors offers a wealth of device and process information, including bulk and interface charges. Many MOS capacitor parameters, such as oxide thickness, flatband voltage, threshold voltage, etc., can be extracted from the high frequency C-V data. However, one parameter, the interface trap density (DIT), is typically derived from both the high and low frequency C-V measurements. Typically performing both types of C-V sweeps requires two different measuring instruments with two different types of cable sets requiring the user to physically change prober connections between measurements. However, using the Keithley 4200A-SCS Parameter Analyzer with the appropriate modules enables the user to make both high and low frequency measurements without recabling.

When configured with two source measure units (SMUs) with preamps and a capacitance voltage unit (CVU), the 4200A-SCS Parameter Analyzer can perform both high and low frequency C-V measurements. The 4200A-CVIV Multi-Switch enables the user to automatically switch between high and low frequency measurements without having to change cables or lift the probe tips. The Clarius software that is included with the 4200A-SCS has an extensive library with built-in tests for making C-V measurements on MOS capacitors including a project that combines both high and low frequency measurements. This project extracts many common C-V parameters including the interface trap density (DIT).

This application note discusses how to use the 4200A-SCS Parameter Analyzer to measure and to automatically switch between high and low frequency C-V measurements on MOS capacitors. Basic information on MOS capacitors and common parameter extractions is also discussed.

The MOS Capacitor

Figure 1 illustrates the construction of a MOS capacitor. Essentially, a MOS capacitor is just an oxide placed between a semiconductor and a metal gate. The semiconductor and metal gate are the two plates of the capacitor. The oxide functions as the dielectric. The area of the metal gate defines the area of the capacitor.

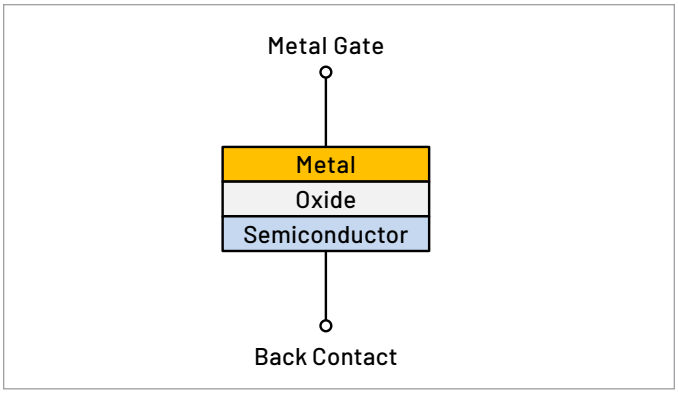


Figure 1. MOS capacitor.

An important property of the MOS capacitor is that its capacitance changes with an applied DC voltage. As a result, the modes of operation of the MOS capacitor change as a function of the applied voltage. Further information on MOS capacitors and making C-V measurements on them can be found in the Keithley application note, ***"C-V Characterization of MOS Capacitors Using the 4200A-SCS Parameter Analyzer".***

Hardware Requirements for Automating High and Low Frequency C-V Measurements

To automate between high and low frequency C-V measurements, the 4200A-SCS Parameter Analyzer must be configured with at least the options listed in **Table 1**.

Qty	Module	Description	Purpose
2	4200-SMU, 4201-SMU, 4210-SMU, or 4211-SMU	Source Measure Units (SMU)	Measures very low frequency (VLF) C-V
2	4200-PA	Preamps for SMUs	Measuring high impedance requires measuring very small current
1	4215-CVU or 4210-CVU	Capacitance Voltage Unit (CVU)	Measures high frequency C-V
1	4200A-CVIV	Multi-Switch	Enables automatic switching between low frequency and high frequency measurements

Table 1. Required modules.

Additional cabling is necessary to connect between the output of the 4200A-CVIV and the probe station. We recommend using the 4200-TRX-.75 Triax Cables on the output of the CVIV. These shielded cables are used to ensure that both very low current and high frequency AC measurements can be made with high accuracy.

Installing and Configuring the 4200A-CVIV

Installing and configuring the 4200A-CVIV consists of making connections to its input terminals and output terminals and updating the 4200A-CVIV configuration in the KCON application.

Input and output connections

The CVU and the preamps of the SMUs are connected to the input terminals of the 4200A-CVIV as shown in **Figure 2**. SMU1 and SMU2 are connected to CH1 and CH2. Either two additional SMUs or channel blocks (included with the CVIV) are connected to CH3 and CH4 inputs.

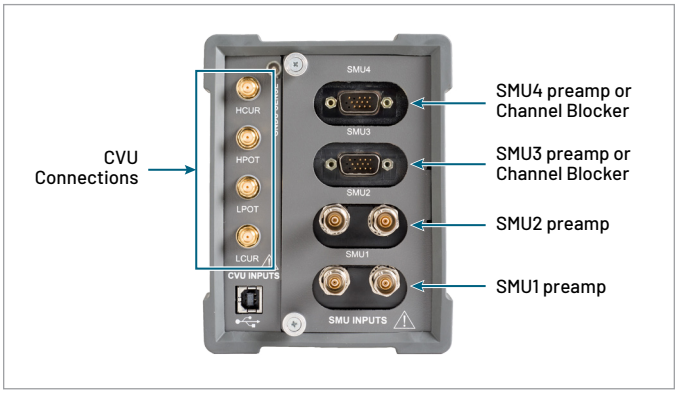


Figure 2. Input connections on the 4200A-CVIV.

The output terminals of the CVIV are connected to the prober. CH1 is connected to the gate of the MOS capacitor and is used to measure the capacitance. CH2 is connected to the substrate, or chuck, and is used to apply the DC voltage. More information on making proper connections to make optimal C-V measurements can be found in the Keithley application notes listed in Appendix B.

Configuring the Setup in KCON

After the SMUs and CVU are connected to the CVIV, make sure the CVIV is connected to the 4200A-SCS with the supplied USB cable. Close the Clarius application and open the KCON application on the desktop. At the top of the screen, select Update. Once the unit is done updating, select Save. Open Clarius to begin configuring the Clarius software.

Selecting and Configuring the *moscap-cv-dit-cviv* Project for C-V Measurements

The built-in library of the Clarius application includes several tests and projects that perform high and low frequency measurements on MOS capacitors. With the Clarius V1.9 release, a new project, ***moscap-cv-dit-cviv***, has been added to the Projects Library. This project switches between high and low frequency C-V sweeps and includes the calculation of the interface trap density (DIT). This project can be found in the library in the Select view search bar by entering DIT. By selecting and then creating the project, the ***moscap-cv-dit-cviv*** project will appear in the project tree as shown in **Figure 3**. The following sections will describe the tests in the project tree.

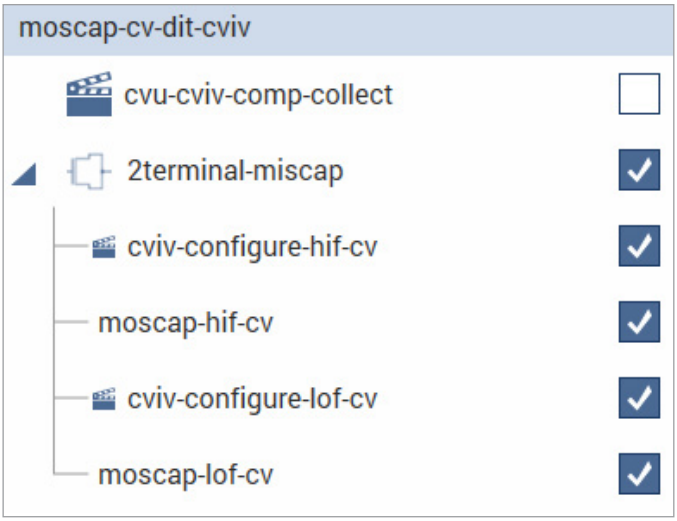


Figure 3. Project tree of *moscap-cv-dit-cviv* project.

Acquiring CVU Compensation Data

The first item listed in the project tree is the ***cvu-cviv-comp-collect*** Action for acquiring compensation data. CVU Connection Compensation is used to correct for offset and gain errors caused by the connections between the CVU and the device under test (DUT). In this case, the connections are from the CVU through CH1 and CH2 of the CVIV and to the cabling to the probe and chuck. This Action is Run with the probes up. A screen capture of the Configure view of the ***cvu-cviv-comp-collect*** Action is shown in **Figure 4**.

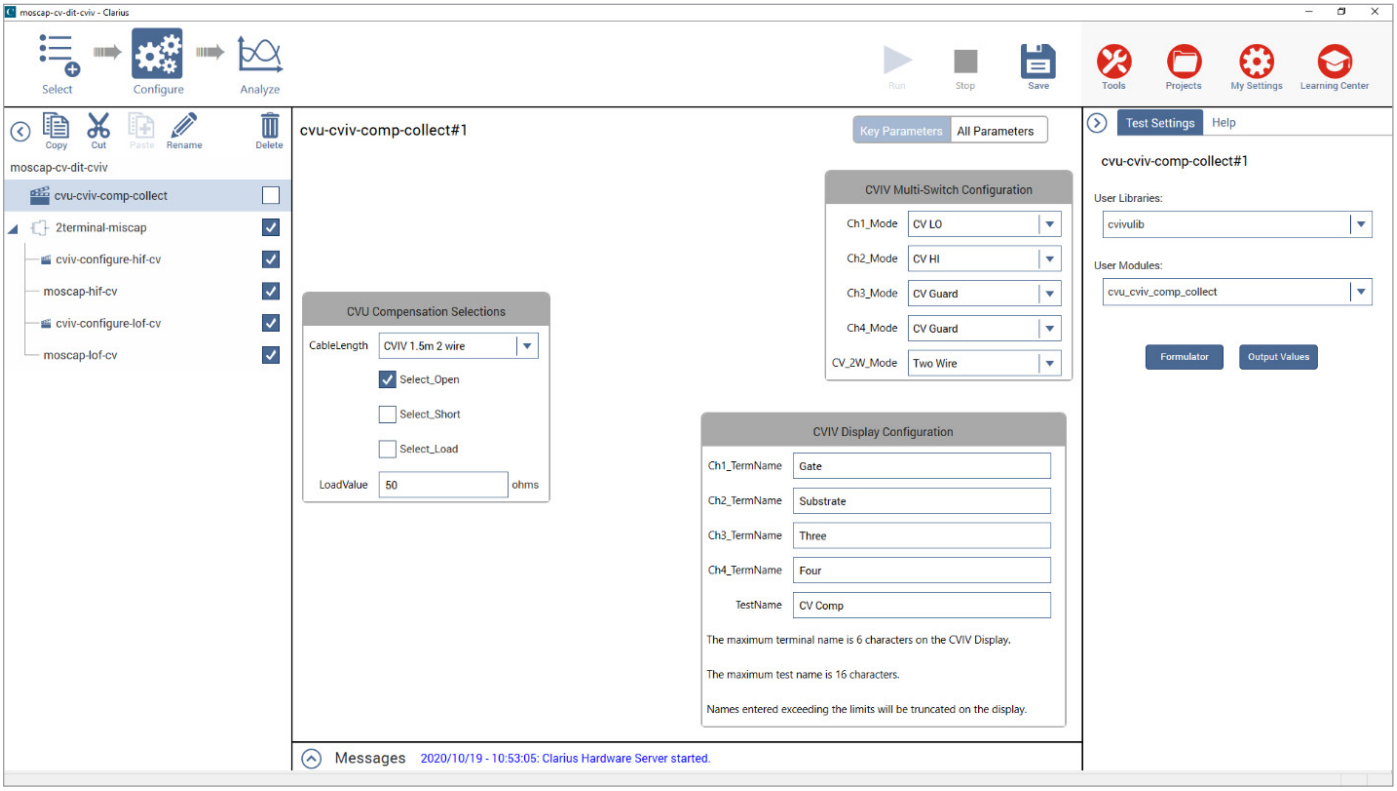


Figure 4. Configure view of the *cvu-cviv-comp-collect* Action for acquiring compensation data.

Switching Between the CVU and SMUs

The ***cviv-configure-hif-cv*** and ***cviv-configure lof-cv*** actions are used to automatically switch the outputs of CH1 and CH2 of the CVIV between the CVU and the two SMUs. This prevents unnecessary disturbances of the cabling and connections to the device during the test.

The CVU connections through the CVIV are shown in **Figure 5**. In this case, CVH terminal is connected through CH 1 to the substrate of the MOS cap and forces the DC bias voltage. The CVL terminal is connected through CH 2 to the gate of the MOS cap and measures the ac current. Even though CH 3 and CH4 are unused, these channels are configured for CV Guard to minimize noise from unwanted pathways. A screen capture of the ***cvu-configure-hif-cv*** Action is shown in **Figure 6**.

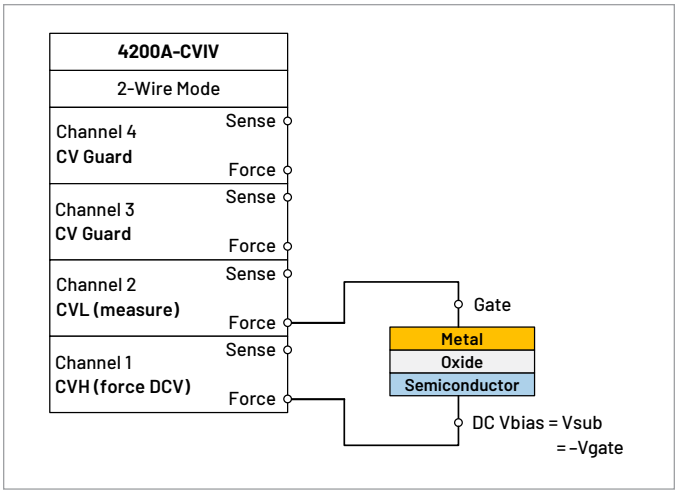


Figure 5. CVU connections through the 4200A-CVIV to the MOS capacitor.

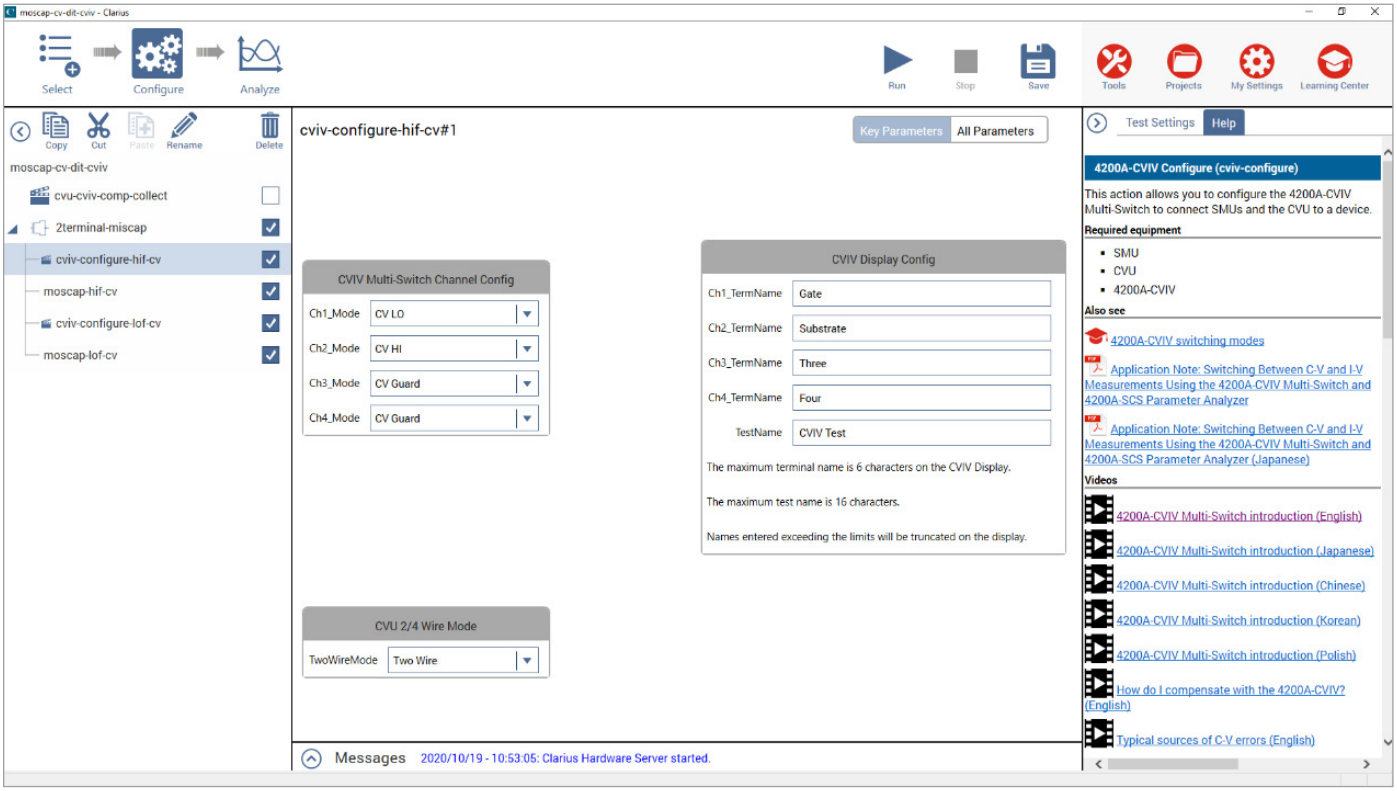


Figure 6. Configuration view of *cviv-configure-hif-cv action.*

Figure 7 shows the SMU connections through the CVIV for the low frequency C-V measurements. SMU1 is connected through CH1 to the substrate and SMU2 is connected through CH2 to the gate. Just like for the high frequency CVU measurements, the DC bias is applied to the substrate so that the gate voltage = (-1)*Vsubstrate.

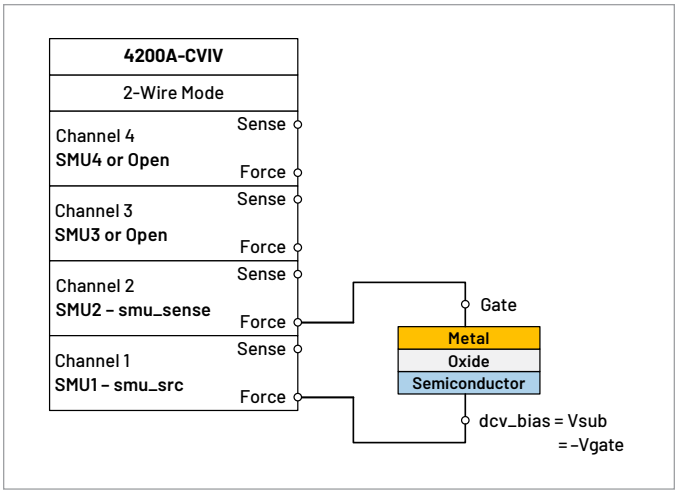


Figure 7. SMU connections through the 4200A-CVIV for MOS capacitor measurements.

High Frequency Measurements Using the CVU

The 4215-CVU or 4210-CVU Capacitance Voltage Unit can measure capacitance with a range of test frequencies from 1 kHz to 10 MHz. The ***moscap-hif-cv*** test in the project is configured for making a C-V sweep with the CVU. The test parameters, such as the test frequency, DC bias, and timing settings, can be adjusted in the Configure view of the test, which is shown in **Figure 8**. To enable the CVU offset compensation, check the appropriate Compensation boxes in the Terminal Settings window.

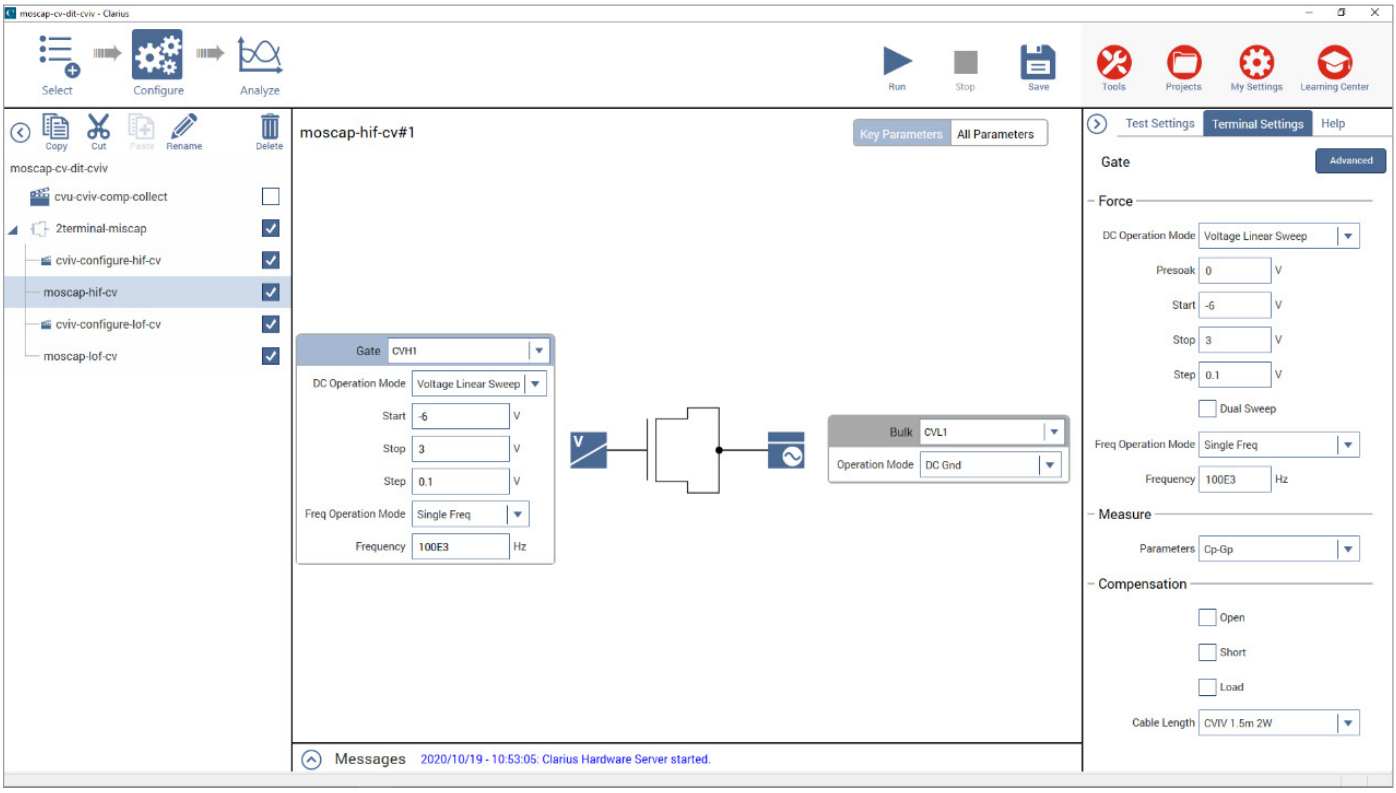


Figure 8. Configure view of the *moscap-hif-cv* test.

This test has calculations in the Formulator for deriving and adjusting for the series resistance. The formulas in this test are listed in Appendix A. Some of the constants in the Formulator including the gate area and temperature will need to be adjusted prior to executing the test.

Once the test is Run, the graph is automatically generated. **Figure 9** shows the results of measuring an n-type MOS capacitor using the test.

Keithley application notes for making optimal high frequency C-V measurements on MOS capacitors are listed in Appendix B.

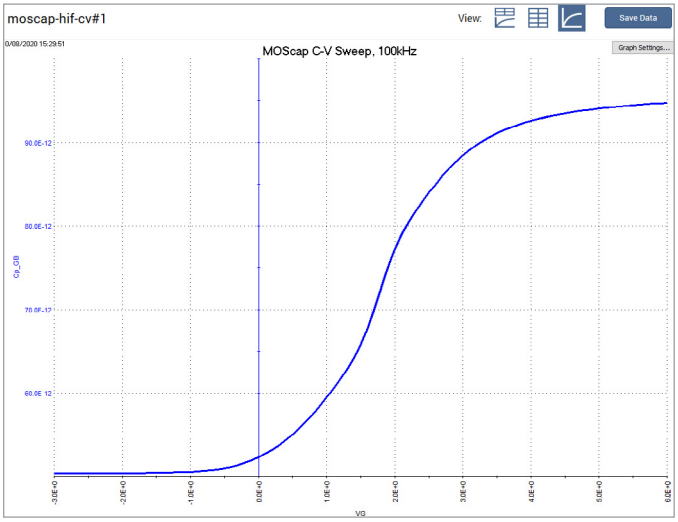


Figure 9. C-V sweep of MOS capacitor using the 4215-CVU.

Low Frequency Measurements Using Two SMUs

The 4200A-SCS makes low frequency C-V measurements using the very low frequency (VLF) C-V technique, which uses the low current measurement capability of the SMUs to perform C-V measurements at specified low frequencies in the range of 10 mHz to 10 Hz. The VLF C-V technique requires two SMUs with preamps.

Figure 10 is a simplified diagram of the SMU instrument configuration used to generate the low frequency impedance measurements. SMU1 outputs the DC bias with a superimposed AC signal and measures the voltage. SMU2 measures the resulting AC current while sourcing 0 V DC.

More detailed information on the VLF-CV technique can be found in the Keithley application note, ***"Performing Very Low Frequency Capacitance-Voltage Measurements on High Impedance Devices Using the 4200A-SCS Parameter Analyzer".***

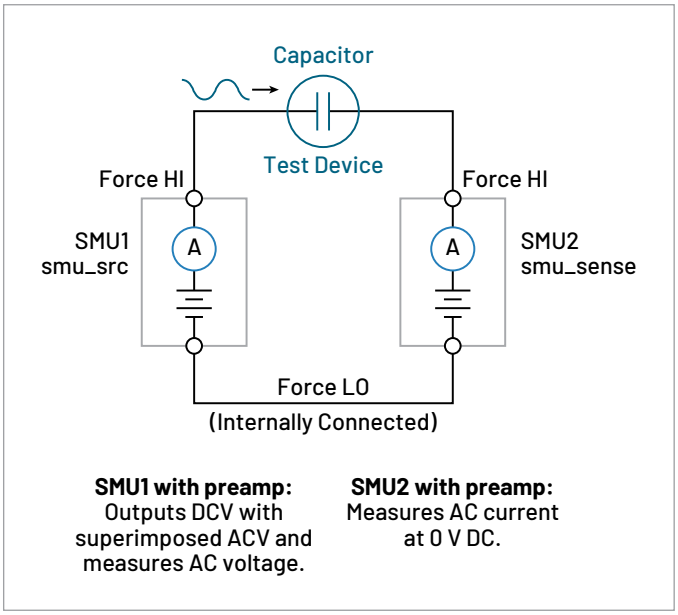


Figure 10. VLF C-V measurement setup for a MOS capacitor on wafer.

The ***moscap-lof-cv*** test in the project tree is used for making a very low frequency C-V sweep on the MOS capacitor. Test parameters can be adjusted in the Configure view, shown in **Figure 11**.

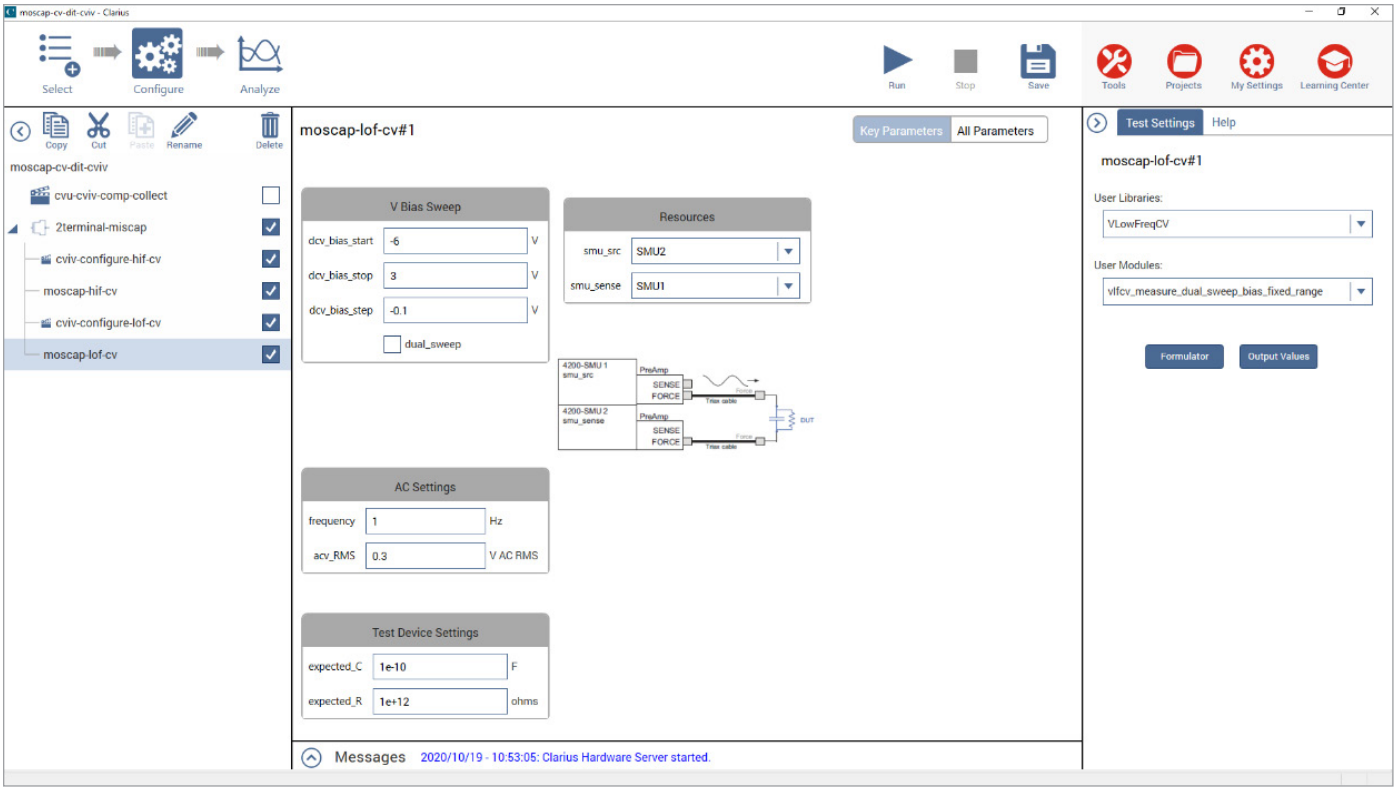


Figure 11. Configure view of the *moscap-lof-cv* test.

Once the test is Run, the graph is automatically generated as shown in **Figure 12**.

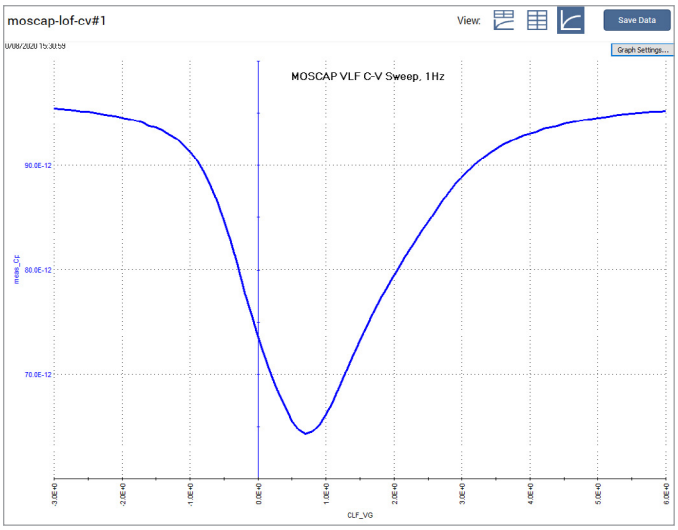


Figure 12. Very low frequency (VLF) C-V sweep of MOS capacitor.

Executing the *moscap-cv-dit-cviv* project and parameter extractions

When the ***moscap-cv-dit-cviv*** project is selected and is executed from the top of the project tree, the actions and tests will sequentially execute in their order in the project tree. The high and low frequency C-V measurements are sent to the project level Analyze Sheet and Graph and are plotted as shown in **Figure 13**.

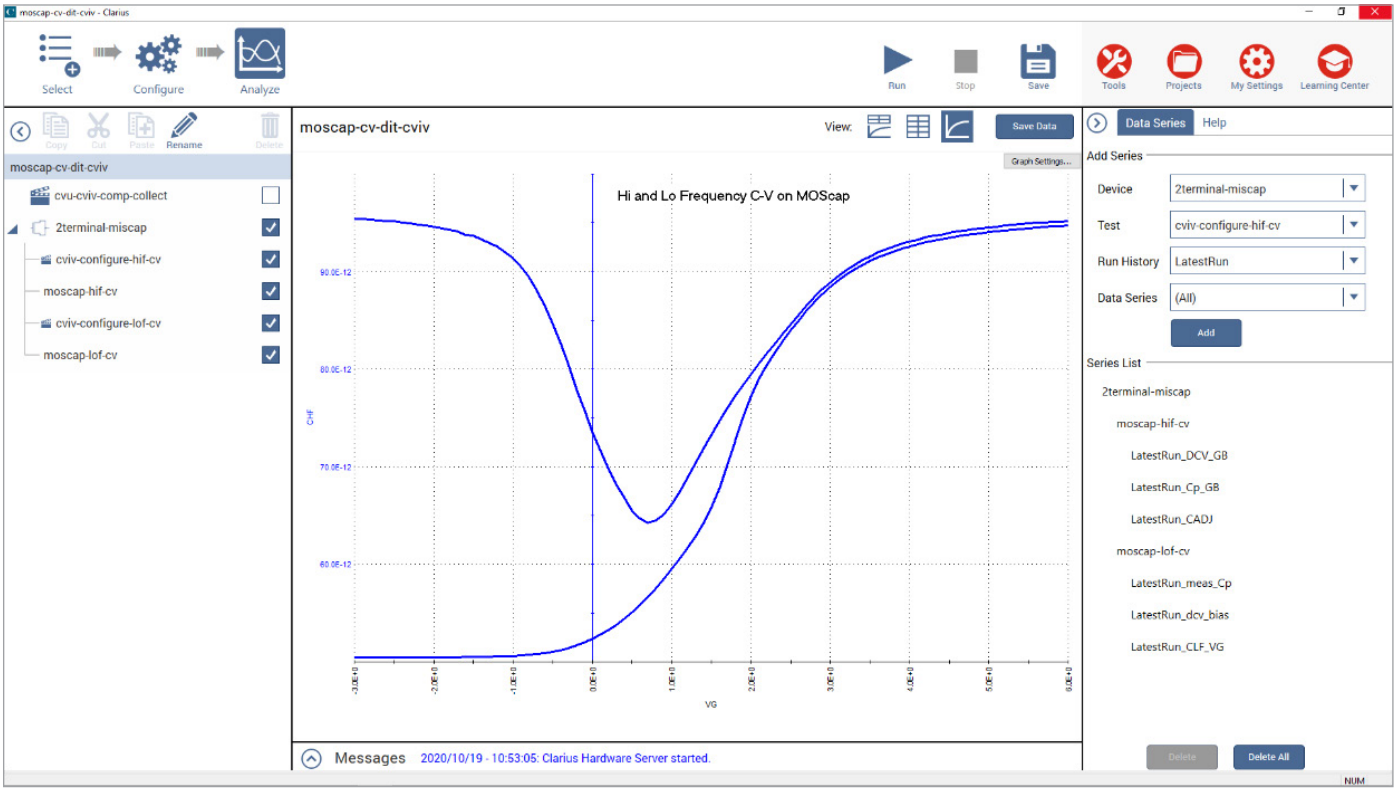


Figure 13. HI and LO Frequency C-V curves plotted in the project level Analyze view.

The C-V measurements are combined in equations in the formulator to calculate many MOS capacitor parameters including the flatband capacitance, flatband voltage, oxide capacitance, and the interface trap density as shown in **Figure 14**. Appendix A lists all the calculated parameters found at the project level Analyze view as well as in the ***moscap-hif-cv*** test in the project tree.

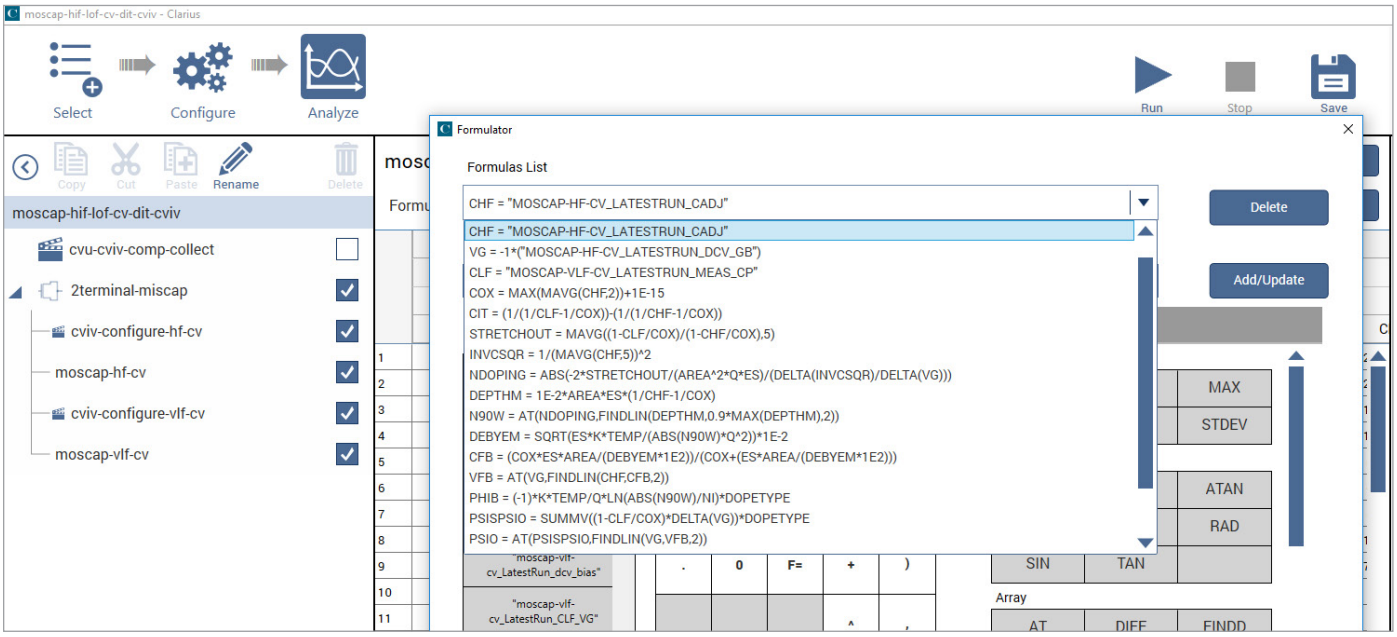


Figure 14. Project level Formulas List.

Interface Trap Density (DIT)

From the calculated parameters in the project level, the interface trap density (DIT) is derived and can be plotted. Interface traps are defects or impurities resulting from processing or device damage. These traps are located at the semiconductor interface and can be charged or discharged and affect the device capacitance. Because traps may respond slowly to changes in gate voltage, they affect the device capacitance at high frequencies but not low frequencies. DIT can be plotted against the interface trap energy (eV) with respect to mid band gap as shown in **Figure 15**.

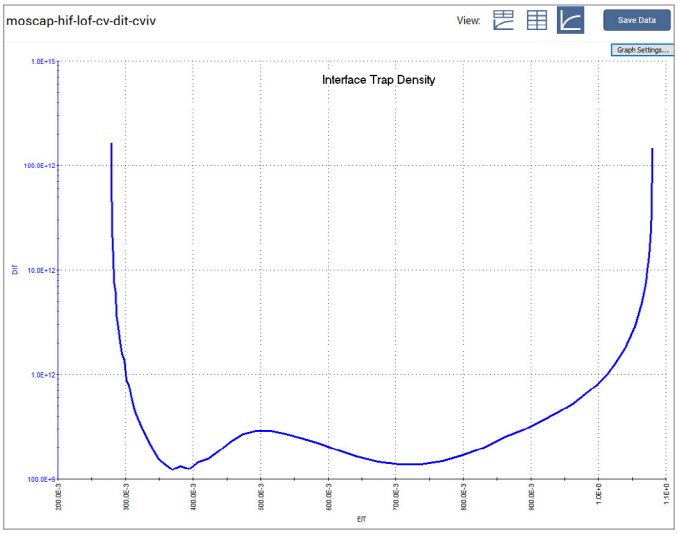


Figure 15. Interface trap density graphed in project level Analyze View Graph.

Conclusion

High and low frequency C-V measurements can be automated using two SMUs with preamps, a CVU, the 4200A-CVIV Multi-Switch, and the Clarius software. From the C-V data, many important device parameters are derived including the interface trap density. Techniques for making optimal high and low frequency C-V measurements are found in the applications notes listed in Appendix B.

Appendix A: Project Formulas and Constants

Project Level Calculations in the Formulator

Formula	Description
CHF	Adjusted high frequency capacitance from the latest Run of the moscap-hf-cv test: CHF= "MOSCAP-HF-CV_LATESTRUN_CADJ"
VG	Since the DC voltage is applied to the substrate, VG=-Vsubstrate, and is updated from the latest Run of the moscap-hf-cv test: VG= -1*("MOSCAP-HF-CV_LATESTRUN_DCV_GB"
CLF	Low frequency capacitance from the latest Run of the moscap-vlf-cv test: CLF="MOSCAP-VLF-CV_LATESTRUN_MEAS_CP"
COX	Oxide capacitance: COX = MAX(MAVG(CHAF,2))+1E-15
CIT	Interface trap capacitance: CIT=(1/(1/CLF-1/COX)-1/(1/CHF-1/COX))
STRETCHOUT	Stretch out factor due to interfacial states: STRETCHOUT = MAVG((1-CLF/COX)/(1-CHF/COX),5)INVCSQR = 1/(MAVG(CHF,5))^2
INVCSQR	Inversed square of high frequency capacitance: INVCSQR = 1/(MAVG(CHF,5))^2
NDOPING	Doping density: NDOPING = ABS(-2*STRETCHOUT/(AREA^2*Q*ES)/(DELTA(INVCSQR)/DELTA(VG)))
DEPTH	Depletion depth (in meters): DEPTHM = 1E-2*AREA*ES*(1/CHF-1/COX)
N90W	Doping density at 90% of maximum depletion depth: N90W = AT(NDOPING,FINDLIN(DEPTHM,0.9*MAX(DEPTHM),2))
DEBYEM	Debye length (in meters): DEBYEM = SQRT(ES*K*TEMP/(ABS(N90W)*Q^2))*1E-2
CFB	Flatband capacitance: CFB = (COX*ES*AREA/(DEBYEM*1E2))/(COX+(ES*AREA/(DEBYEM*1E2)))
VFB	Flatband voltage: VFB = AT(VGS,FINDLIN(CHF,CFB,2))
PHIB	Bulk Potential: PHIB = (-1)*K*TEMP/Q*LN(ABS(N90W)/NI)*DOPETYPE
PSISPSIO	PSIS-PSIO, which is surface potential: PSISPSIO = SUMMV((1-CLF/COX)*DELTA(VG))*DOPETYPE
PSIO	Offset in surface potential due to calculation method and flatband voltage: PSIO = AT(PSISPSIO,FINDLIN(VG,VFB,2))
PSIS	Silicon surface potential, ϕ_s. More precisely, this value represents band bending and is repeated to surface potential via the bulk potential. PSIS = PSISPSIO-PSIO
EIT	Interface trap energy (eV) with respect to mid band gap: EIT = PSIS+PHIB
DIT	Interfacial states density (cm^-2eV^-1): DIT = CIT/(AREA*Q)

Constants in Project level Sheet Formulator

Name	Default Value	Unit	Description
ES	1.04E-12	F/cm	Semiconductor permittivity
DOPETYPE	-1		1 = p-type -1 = n-type
TEMP	300	K	Test temperature
AREA	0.0025	cm^2	Gate area
NI	1.45E+10	cm^-3	Ni – intrinsic carrier concentration

Formulas for *moscap-hf-cv* test:

Formula	Description
VG	Gate voltage: VG = -DCV_GB
RS	Series Resistance calculated from capacitance in strong accumulation and conductance: RS = (AT(MAVG(GP_GB, 5)/((2*PI*F_GB)*MAVG(CP_GB, 5)), MAXPOS(MAVG(CP_GB, 5))))^2/((1+(AT(MAVG(GP_GB, 5)/((2*PI*F_GB)*MAVG(CP_GB, 5)), MAXPOS(MAVG(CP_GB, 5))))^2)*(AT(MAVG(GP_GB, 5),MAXPOS(MAVG(CP_GB, 5)))))
AR	Intermediate parameter for calculation of corrected capacitance: AR = GP_GB-(GP_GB^2 + (2*PI*F_GB*CP_GB)^2)*RS AR = G – (G2 + (2πfC)2)RS
CADJ	Corrected capacitance by compensating series resistance: CADJ = ((GP_GB^2) + (2*PI*F_GB*CP_GB)^2)*(CP_GB)/(AR^2 + (2*PI*F_GB*CP_GB)^2)
COX	Oxide capacitance (usually set to max capacitance in accumulation): COX = MAX(MAVG(CADJ, 2))+1E-15

Appendix B: References

1. Nicollian, E.H. and Brews, J.R. MOS Physics and Technology, Wiley, New York (1982)

2. Schroder, D.K. Semiconductor Material and Device Characterization, 2nd edition (New York, Wiley, 1998)

3. Keithley application notes:

   "C-V Characterization of MOS Capacitors Using the 4200A-SCS Parameter Analyzer".

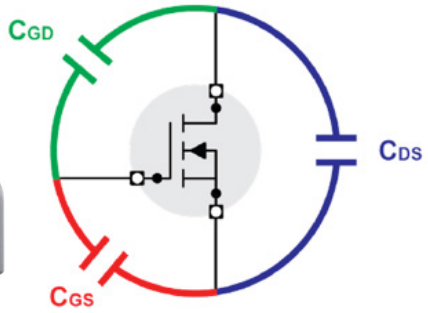
   "Making Optimal Capacitance and AC Impedance Measurements with the 4200A-SCS Parameter Analyzer".

   "Performing Very Low Frequency Capacitance-Voltage Measurements on High Impedance Devices Using the 4200A-SCS Parameter Analyzer".

   "Switching Between C-V and I-V Measurements Using the 4200A-CVIV Multi-Switch and 4200A-SCS Parameter Analyzer".

Tektronix®

Making Three-Terminal Capacitance-Voltage Measurements Up to 400 V Using the 4200A-CVIV Multi-Switch Bias Tee Capability



Introduction

The switching speeds of semiconductor devices such as MOSFETs, IGBTs and BJTs are affected by the capacitance of the components themselves. In order to design their circuits for efficiency, designers need to know these parameters. For example, designing an efficient switch-mode power supply would require the designer to know the device capacitance because this would affect the switching speed and, therefore, the efficiency. This information is usually provided in a MOSFET's datasheet.

The capacitance of three-terminal power semiconductor devices can be looked at in two different ways: at the component level and at the circuit level. Looking at the capacitances at the component level involves characterizing capacitance between every device terminal. Looking at the capacitance at the circuit level involves characterizing the combination of component-level capacitances. For example, **Figure 1** illustrates the component-level capacitances of a power MOSFET.

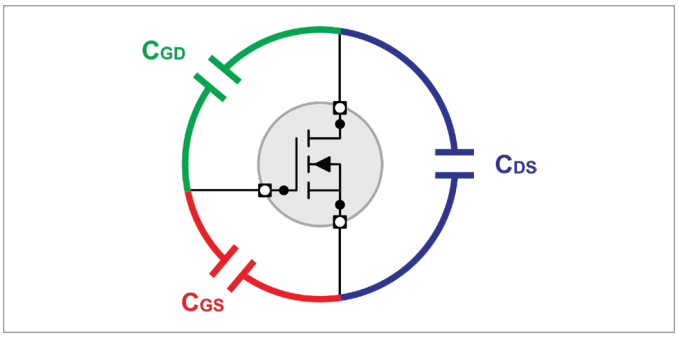


Figure 1. Component-level capacitances for a power MOSFET

Figures 2 through 4 illustrate the relationship between the component-level and circuit-level capacitance for a power MOSFET. Similar capacitance measurements can also be made for BJT and IGBT devices.

The relationships are derived as follows:

- $C_{ISS} = C_{GS} + C_{GD}$ = input capacitance
- $C_{OSS} = C_{DS} + C_{GS}$ = output capacitance
- $C_{RSS} = C_{GD}$ = reverse transfer capacitance

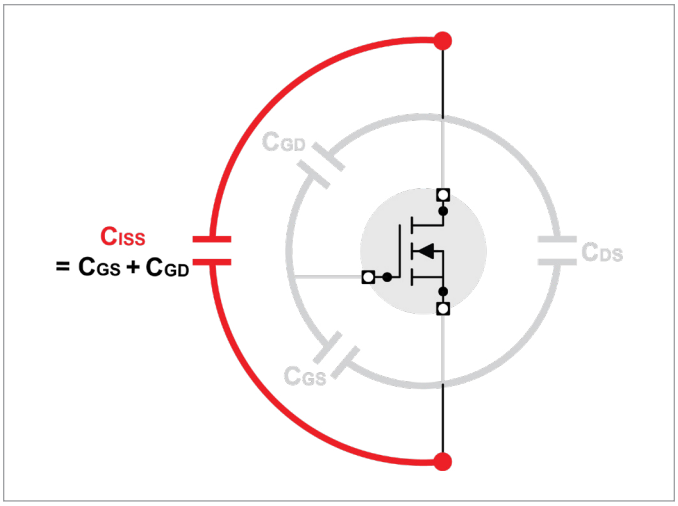


Figure 2. Input capacitance for a power MOSFET

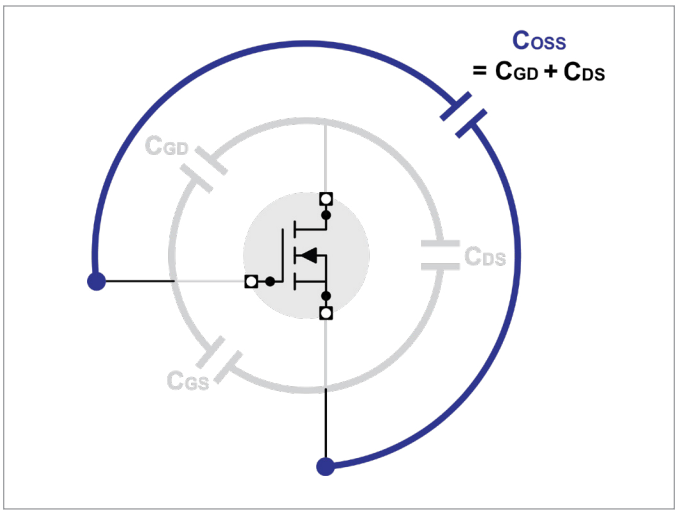


Figure 3. Output capacitance for a power MOSFET

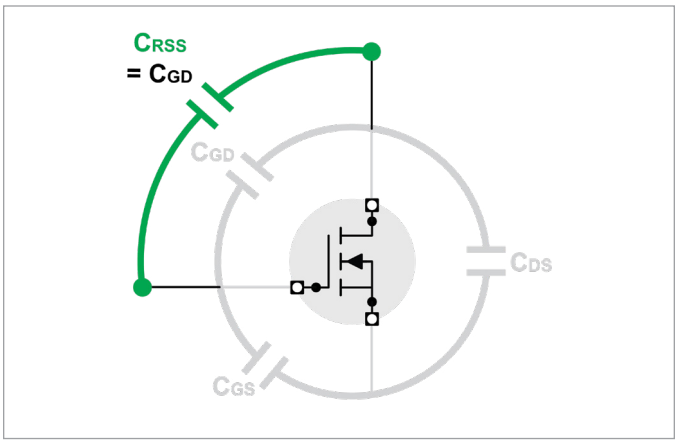


Figure 4. Reverse transfer capacitance for a power MOSFET

Device capacitance typically varies with the applied voltage. Therefore, complete characterization requires knowledge of the capacitance at the maximum rated voltage. This application note explains how the C_{ISS}, C_{OSS} and C_{RSS} measurements are made using the bias tee capabilities provided by the 4200A-CVIV Multi-Switch and that were added in Clarius V1.4. The CVIV can easily switch between I-V and C-V measurements without recabling. It can also move the C-V measurements to any device terminal without recabling or lifting prober needles.

This application note also shows how the instrument DC output voltage was doubled from 200 V to 400 V for higher voltage measurements on the drain, which is beneficial for testing higher power semiconductors, such as GaN devices. This capability was added in Clarius V1.6 and updated in Clarius V1.9. This application note assumes the reader is familiar with making C-V measurements with the Keithley 4200A-SCS using the 4200A-CVIV.

For more information on bias tee capabilities, refer to these Keithley application notes:

- Using the 4200A-CVIV Multi-Switch to Make High Voltage and High Current C-V Measurements
- Switching Between C-V and I-V Measurements Using the 4200A-CVIV Multi-Switch and 4200A-SCS Parameter Analyzer

Device Connections

All the SMU and CVU connections described in this application note are made through the 4200A-CVIV. The CVIV could have one 4210-CVU or 4215-CVU and up to four SMUs connected to a device. Refer to the 4200A-CVIV Multi-Switch User's Manual for more information.

Using the 4200A-CVIV offers these advantages:

- User-ready, built-in projects to measure C_{ISS}, C_{RSS} and C_{OSS} at up to 200 V and 400 V.
- Automated measurements enabled by the 4200A-CVIV Multi-Switch. There is no need to reconnect the device or cables.
- Open and short C-V compensation.

Figure 5 shows the connection of a MOSFET to the CVIV. For this specific application, at least three SMUs and one CVU are required to complete the test.

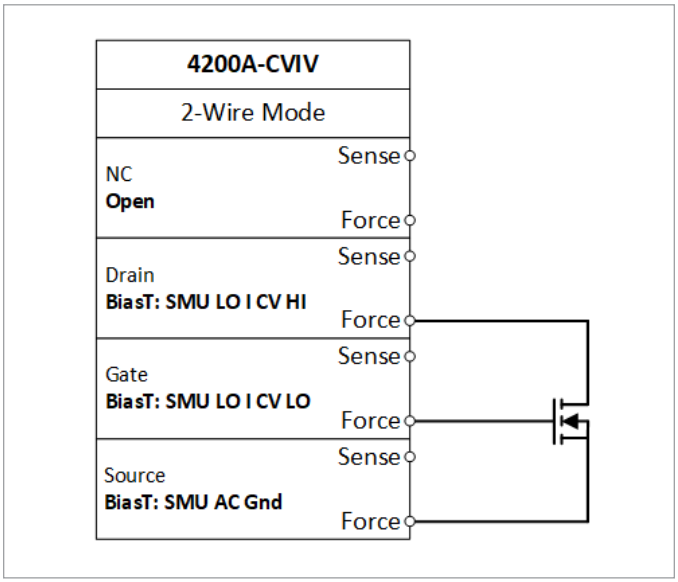


Figure 5. MOSFET connections to the output terminals of the 4200A-CVIV

Figure 6 shows the actual CVIV connections to a packaged MOSFET. Note that all the channels are open on the CVIV. The four channels of the 4200A-CVIV will be configured based on the configuration of each test, so no cable reconnections are required for each test.

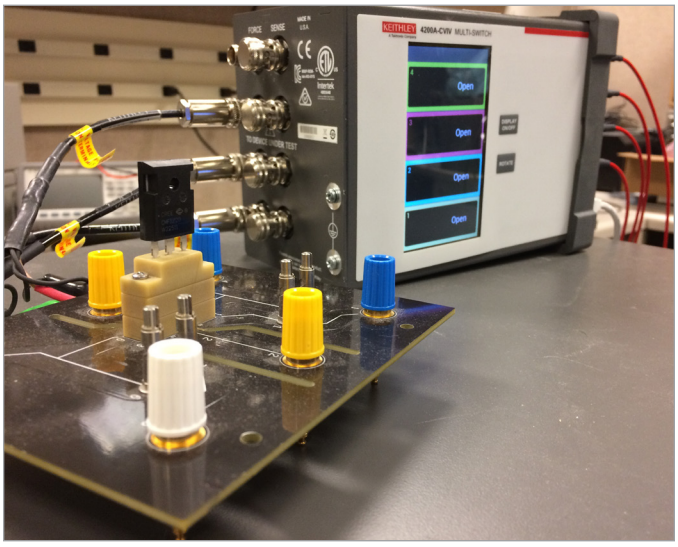


Figure 6. Packaged MOSFET connected to the 4200A-CVIV

Configuring the Measurement in Clarius

The library in Clarius has two projects that perform three-terminal capacitance measurements on MOSFETs. Both projects are similarly configured in Clarius; the difference is with the capability. One project, "MOSFET 3-terminal C-V Test Using 4200A-CVIV Bias Tees," uses a single SMU on the drain, sweeping from 0 to 200 V. The other project, "MOSFET 3-terminal C-V tests up to 400 V using 4200A-CVIV Bias Tees," uses a novel approach to double the voltage to go from 0 to 400 V. This approach uses three SMUs sweeping simultaneously, one on each terminal, to provide a 400 V DC differential across the drain.

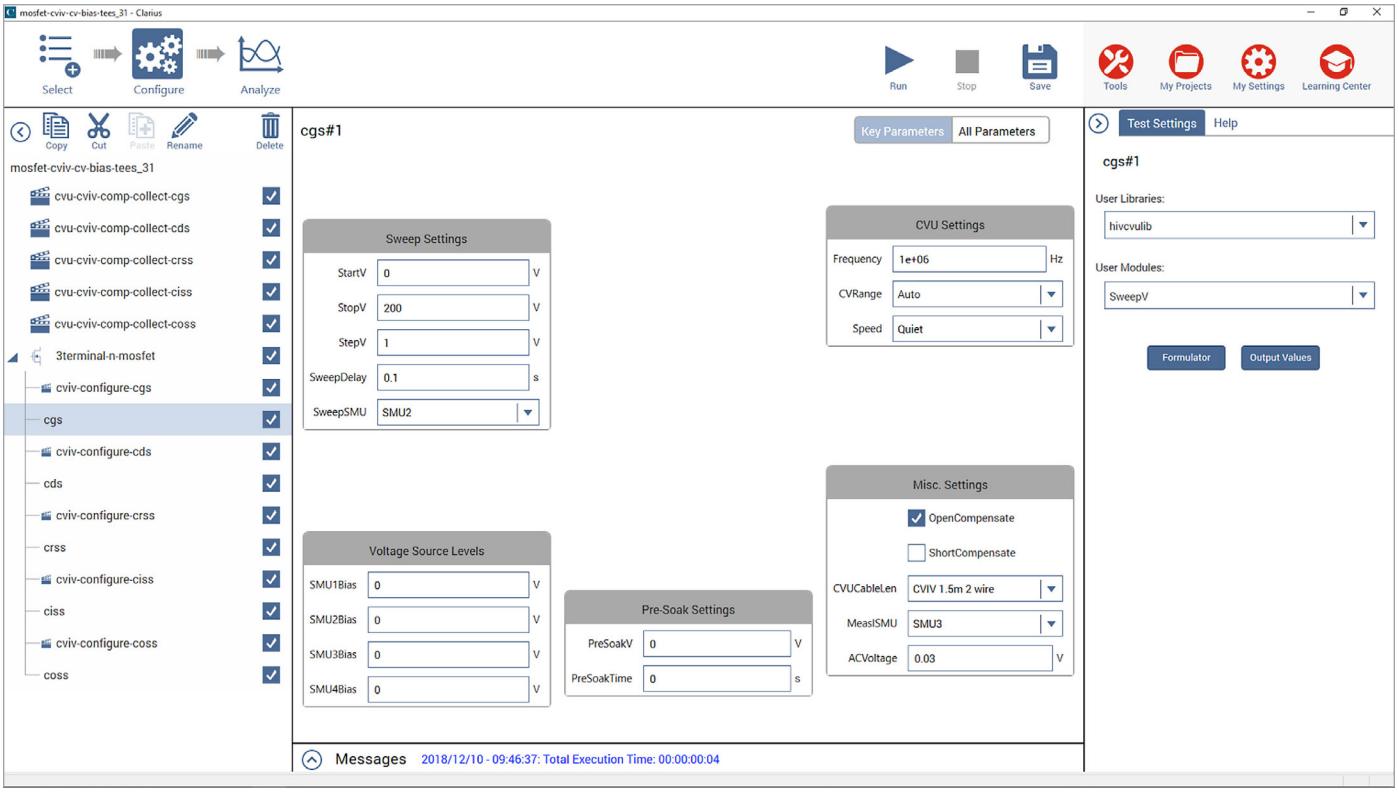


Figure 7. MOSFET-CVIV-CV-Bias-Tees project using the SweepV user module

Figure 7 shows the "MOSFET 3-terminal C-V Test Using 4200A-CVIV Bias Tees" project that uses the SweepV user module in the *hivcvulib*.

This user module enables one sweeping SMU at the drain and capacitance measurements taken at each terminal.

First, open and short compensations are performed to ensure accurate measurements. Specific configuration steps are necessary to perform these compensations. They are called compensation collect actions and are provided in the project tree. Compensation is performed for each test configuration before any test is executed. The 4200A can store the compensation for each configuration so multiple tests can be performed.

This project has five different configurations: C_{GS}, C_{DS}, C_{RSS}, C_{ISS} and C_{OSS}.

CVIV Configuration

The CVIV must be configured accordingly for each test.

The CVIV has many output modes, which are described in the user manual. **Table 1** lists the various output modes.

Table 1. 4200A-CVIV output modes

4200A-CVIV Output Mode	Application and Description
Open	Default setting. Also disconnects a channel from the device.
SMU	Used for I-V measurements. Connects Force HI and Sense HI to the device.
CV HI	Used for C-V measurements. Connects the CVU (HPOT and HCUR) to the device.
CV LO	Used for C-V measurements. Connects the CVU (LPOT and LCUR) to the device.
CV Guard	Used to guard unwanted impedance when making C-V measurements on multi-terminal devices. Apply CV Guard to the terminal to be excluded from the C-V measurement.
Ground Unit	Used for I-V measurements. Connects Force LO and Sense LO to the device.
AC coupled AC ground	Used for C-V measurements. Allows an AC path to ground without providing a DC path.
BiasT SMU CV HI and BiasT SMU CV LO	Used for C-V measurements up to 200 V DC bias. Allows a DC current of up to 1 A, ideal for on-state device measurements.
BiasT SMU LO I CV HI and BiasT SMU LO I CV LO	Recommended for C-V measurements up to 200 V DC bias. Allows a DC current of up to 100 µA, ideal for off-state device measurements.
BiasT SMU AC Gnd	Used to guard unwanted impedance when making C-V measurements on multi-terminal devices. Allows DC bias up to 200 V. Apply BiasT SMU AC Gnd to the terminal to be excluded from the C-V measurement.

Figures 8 through 12 indicate states for each channel of the CVIV for each of the component- and circuit-level capacitance measurements.

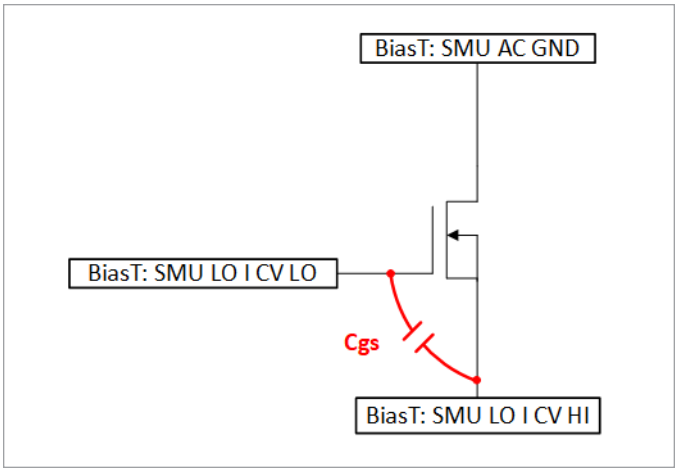


Figure 8. C_{GS} configuration

Figure 8 shows the C_{GS} configuration. This test measures capacitance between the gate and source of the MOSFET while an SMU sweeps DC voltage at the drain.

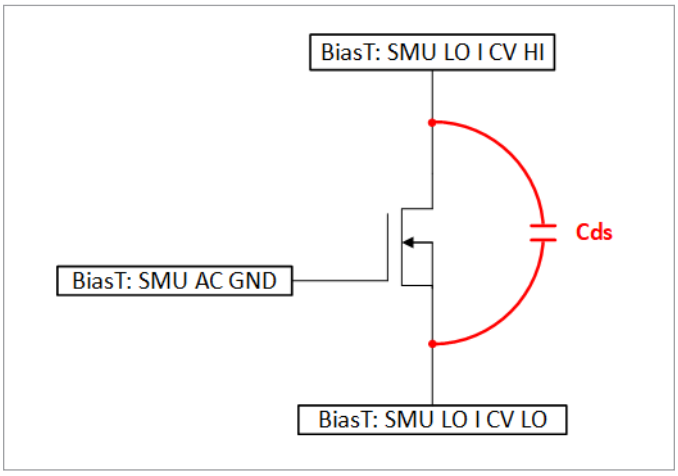


Figure 9. C_{DS} configuration

Figure 9 shows the C_{DS} configuration. This test measures capacitance between the drain and source of the MOSFET while an SMU sweeps DC voltage at the drain.

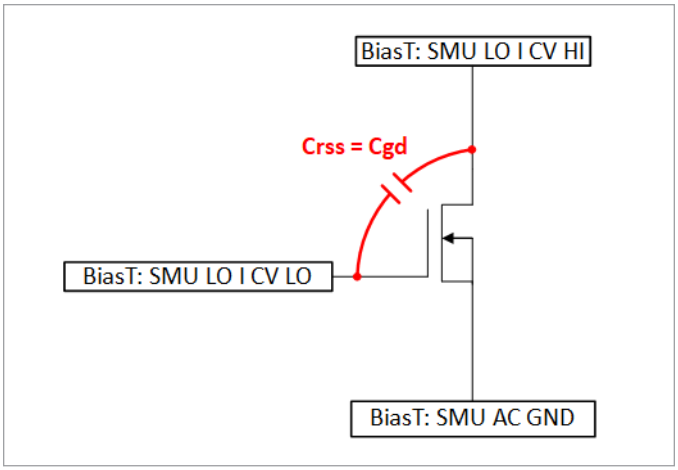


Figure 10. C_{RSS} and C_{GD} configuration

Figure 10 shows the C_{RSS} configuration. This test measures reverse transfer capacitance of the MOSFET while an SMU sweeps DC voltage at the drain.

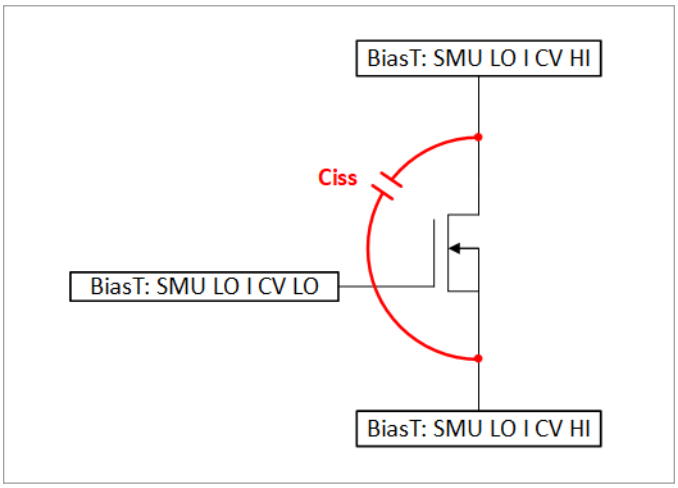


Figure 11. C_{ISS} configuration

Figure 11 shows the C_{ISS} configuration. This test measures the input capacitance of the MOSFET while an SMU sweeps DC voltage at the drain.

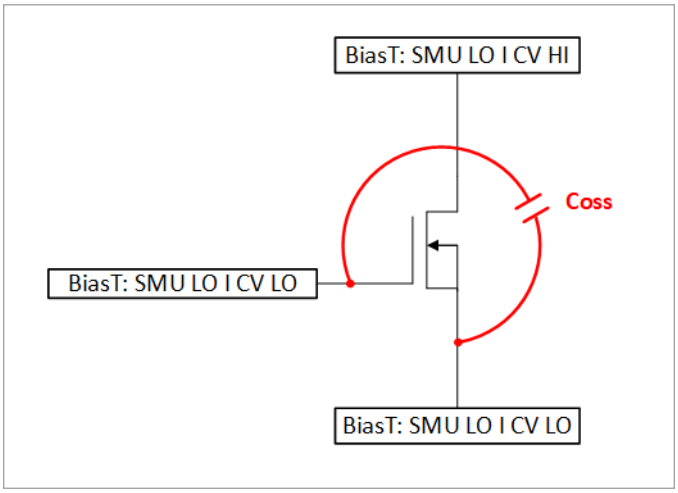


Figure 12. C_{OSS} configuration

Figure 12 shows the C_{OSS} configuration. This test measures the output capacitance of the MOSFET while an SMU sweeps DC voltage at the drain.

Once the tests are executed, the data is plotted. **Figure 13** shows the capacitance characteristics data of a MOSFET as generated with the 4200A.

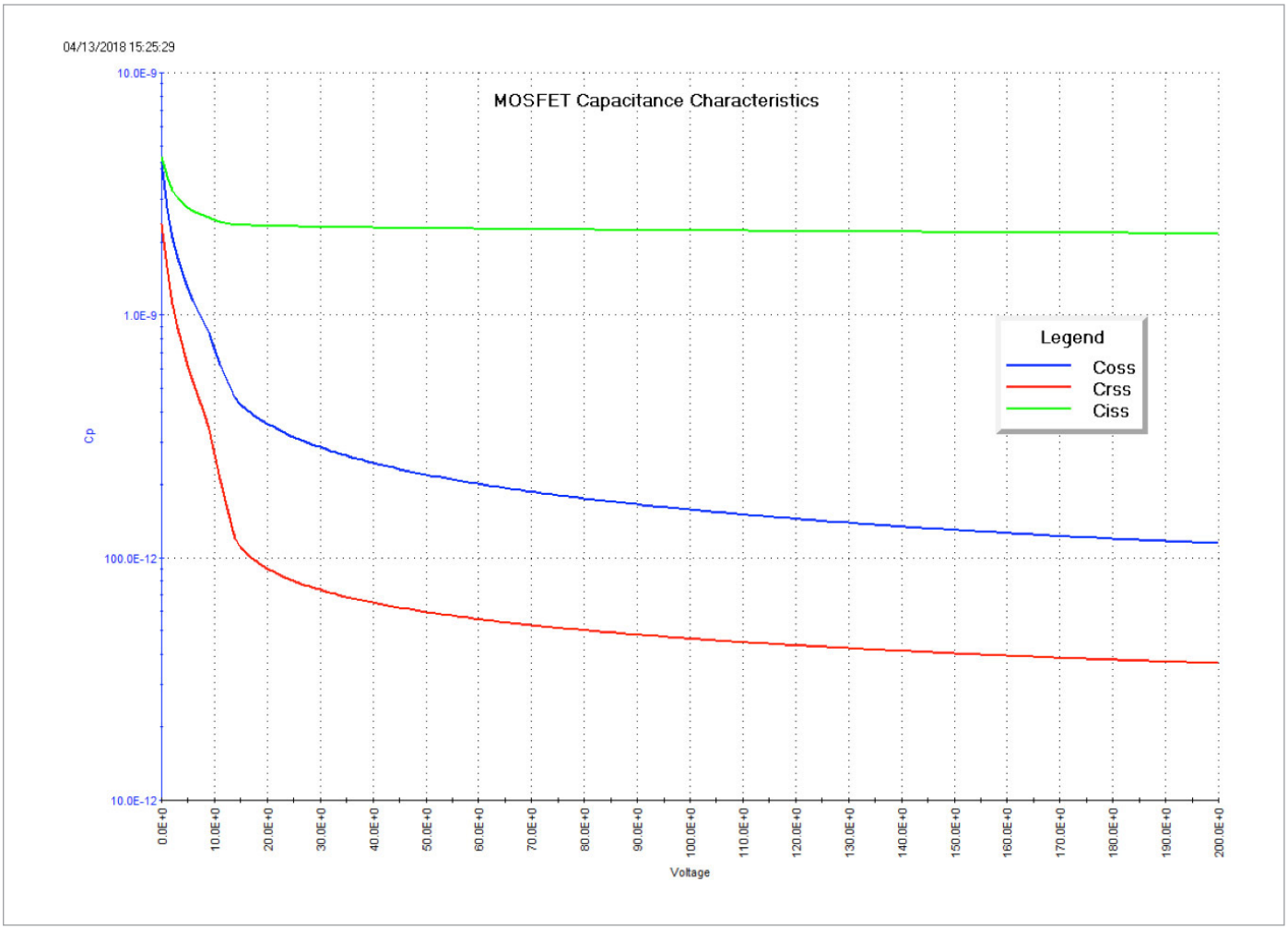


Figure 13. Capacitance characteristics of a MOSFET sweep to 200 V

400 V DC Voltage Sweep

A novel method has been developed to take advantage of the 4200A-CVIV Multi-Switch and sweeping multiple SMUs simultaneously to double the output voltage to 400 V at the MOSFET terminal. These tests are usually done in the OFF state (V_{GS} = 0 V). There's usually one sweeping SMU at the drain and, using the bias tee capabilities built into the 4200A-CVIV, the capacitance is then measured at each terminal.

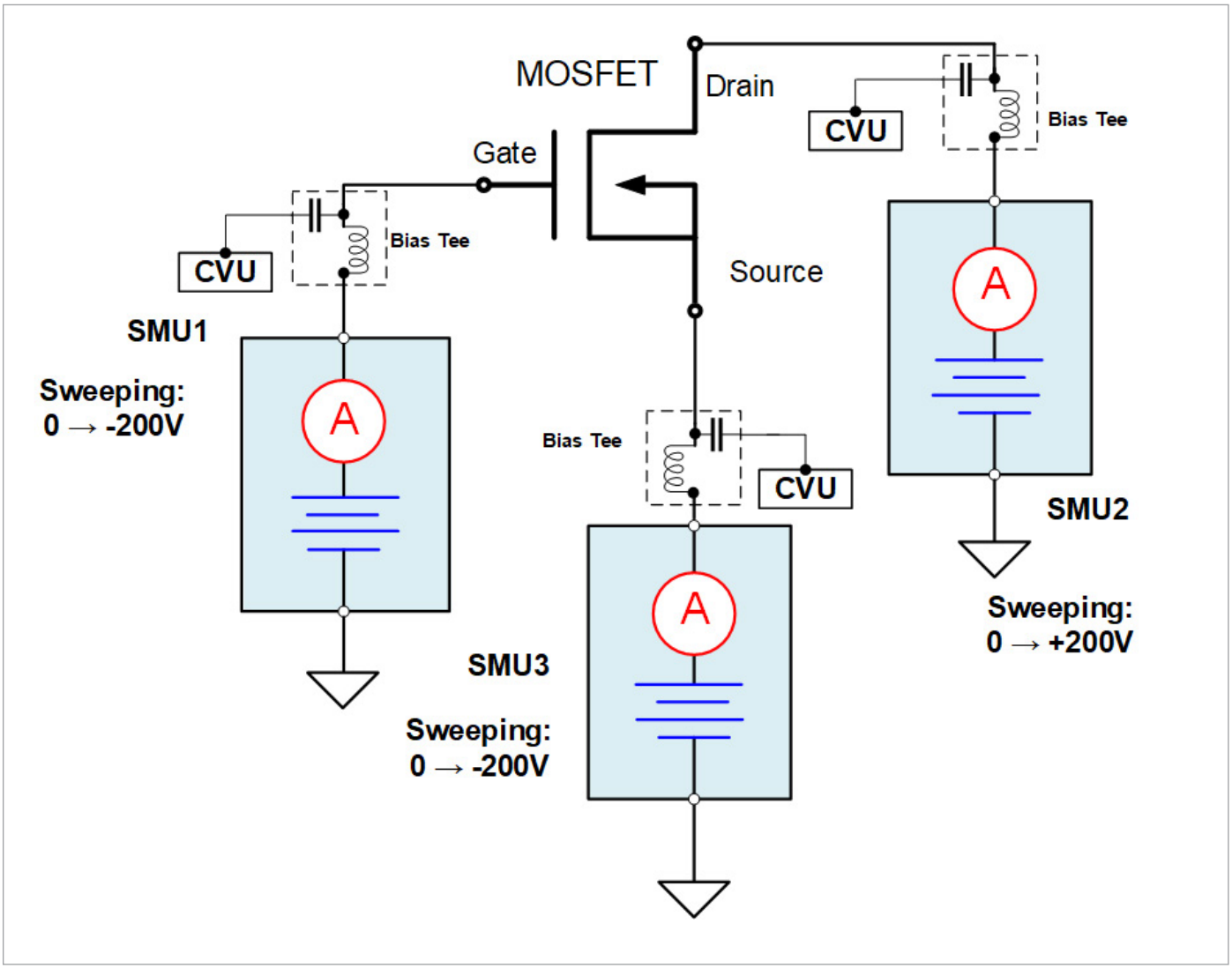


Figure 14. Three SMUs sweeping simultaneously

Figure 14 shows three sweeping SMUs connected to the three terminals of the MOSFET. SMU1 and SMU2 will enable a voltage sweep up to 400 V differential. SMU2 and SMU3 must sweep simultaneously at the same voltage, which enables a 0 V drop at the gate. Using this method, we can produce a 400 V sweep at the drain.

Note: This method is to be used on packaged devices only, and not for wafer-level devices.

These measurements are performed using the *multipleSMU_SweepV* user module, available in the *hivcvulib* user library.

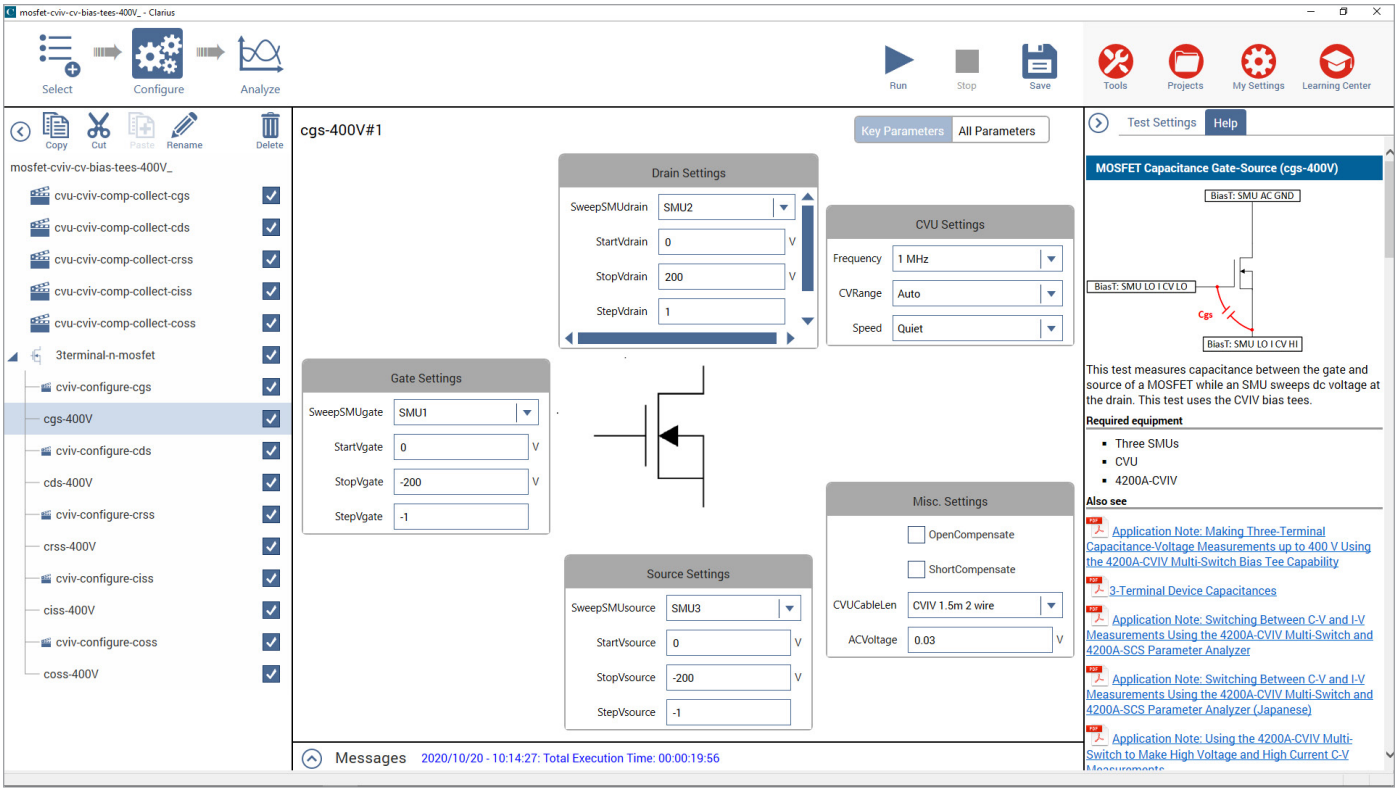


Figure 15. Project for outputting up to 400 V DC differential

Figure 15 shows the *MOSFET 3-terminal C-V tests up to 400V using 4200A-CVIV Bias Tees* project that uses the user module *multipleSMU_SweepV*.

The project tree is set up the same way as the previous project. All of the CVIV configuration actions, including the compensation, are done in exactly the same way. The only difference is that there are two more SMUs that must be configured. The device connections are still the same.

By default, the test should sweep from 0 to 400 V on the drain. Both the gate and source SMUs should sweep simultaneously and at the same voltage. The user is restricted when changes are made to start and stop voltages on the terminals.

The user also has the ability to change the CVU settings such as the frequency, range and speed based on the impedance of the device being tested.

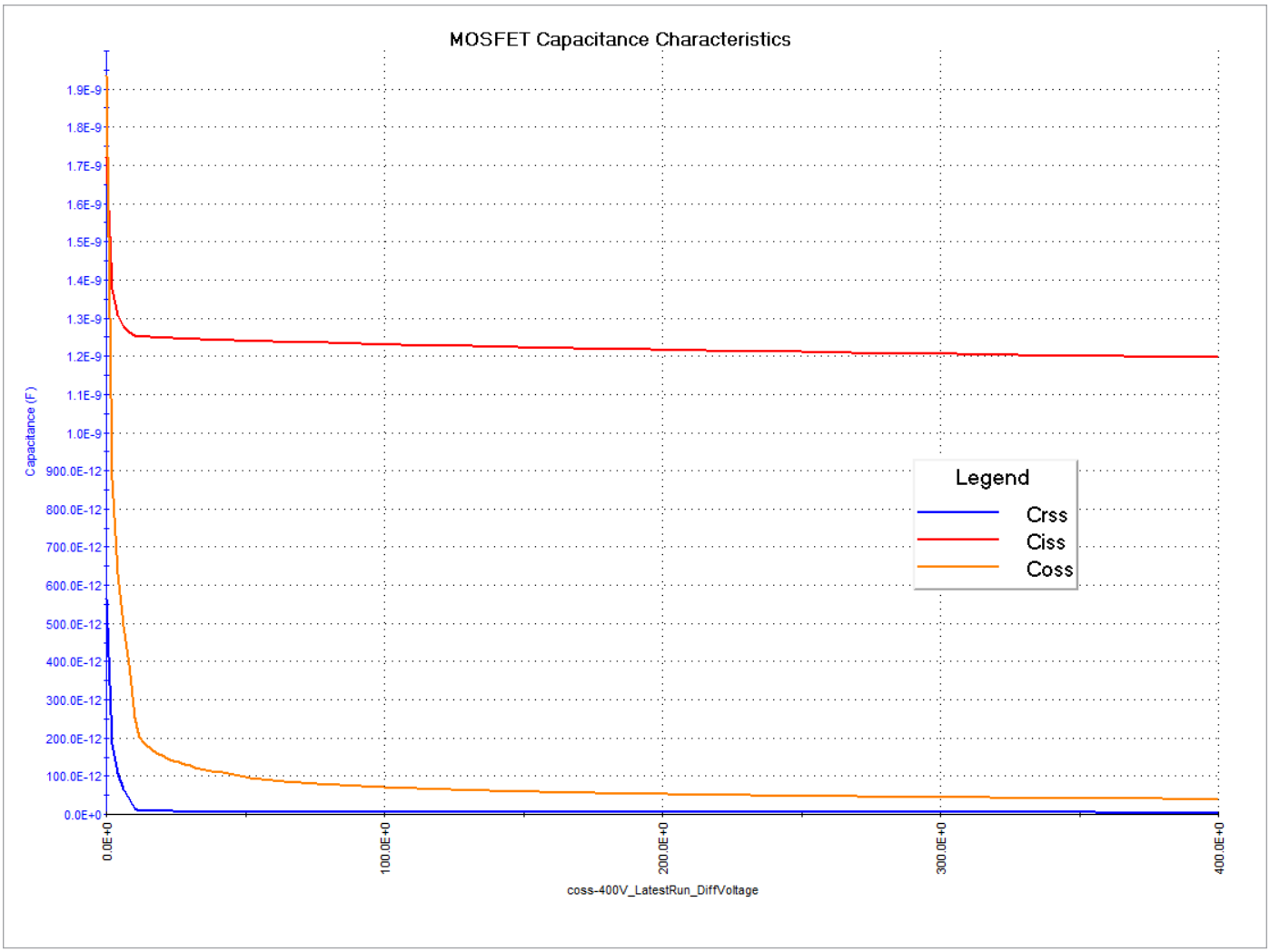


Figure 16. Capacitance characteristics of a MOSFET sweep to 400 V

Figure 16 shows the C-V sweep up to 400 V on a MOSFET generated by the 4200A-SCS. The differential voltage is a calculated value. It's the difference between the drain and the source voltages.

Run1 Formulas List

	multipleSMU_S	Cp	Gp	Time	DrainVoltage	GateVoltage	SourceVoltage	DiffVoltage	FrequencyVal
1	0	1.7217E-9	1.0779E-3	000.0000E-3	000.0000E-3	000.0000E-3	000.0000E-3	000.0000E-3	1.0000E+6
2		1.3747E-9	682.4445E-6	1.1321E+0	1.0000E+0	-1.0000E+0	-1.0000E+0	2.0000E+0	1.0000E+6
3		1.3068E-9	618.0853E-6	2.2607E+0	2.0000E+0	-2.0000E+0	-2.0000E+0	4.0000E+0	1.0000E+6
4		1.2769E-9	591.6332E-6	3.3917E+0	3.0000E+0	-3.0000E+0	-3.0000E+0	6.0000E+0	1.0000E+6
5		1.2618E-9	579.0844E-6	4.5208E+0	4.0000E+0	-4.0000E+0	-4.0000E+0	8.0000E+0	1.0000E+6
6		1.2533E-9	572.9777E-6	5.6486E+0	5.0000E+0	-5.0000E+0	-5.0000E+0	10.0000E+0	1.0000E+6
7		1.2517E-9	571.9208E-6	6.7769E+0	6.0000E+0	-6.0000E+0	-6.0000E+0	12.0000E+0	1.0000E+6
8		1.2508E-9	571.0873E-6	7.9057E+0	7.0000E+0	-7.0000E+0	-7.0000E+0	14.0000E+0	1.0000E+6
9		1.2499E-9	570.1984E-6	9.0337E+0	8.0000E+0	-8.0000E+0	-8.0000E+0	16.0000E+0	1.0000E+6
10		1.2492E-9	569.5463E-6	10.1610E+0	9.0000E+0	-9.0000E+0	-9.0000E+0	18.0000E+0	1.0000E+6
11		1.2484E-9	568.8524E-6	11.2894E+0	10.0000E+0	-10.0000E+0	-10.0000E+0	20.0000E+0	1.0000E+6

Figure 17. Output data for the 400 V sweep

Figure 17 shows the output data, which lists the sweep voltages on the three terminals. The diffVoltage is the calculated differential voltage value.

Conclusion

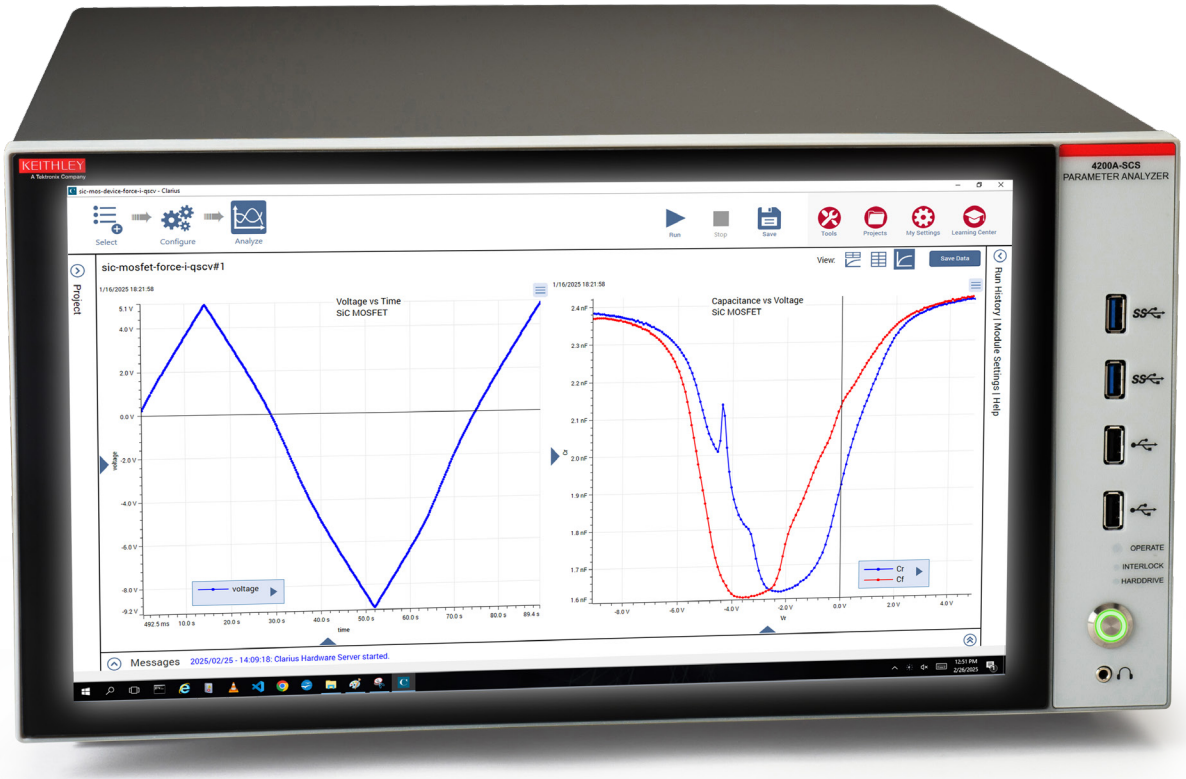
Switching speeds of semiconductor devices like MOSFETs, IGBTs and BJTs are affected by the capacitance of the component itself. This application note demonstrates how using the 4200A-CVIV enables making these measurements at 200 V DC bias without the need to reconnect any cables, which reduces user error and permits automated testing. It also allows measuring circuit-level capacitances directly without going through component-level capacitances, which allows the circuit-level designer to get to the desired data faster.

Moreover, when measuring capacitance on three-terminal devices, one of the terminals is usually not included in the measurement and its capacitance could impact the overall measurement. Using a bias tee at every terminal eliminates the need for external capacitors or shorts.

We have also shown a new method to double the DC bias of the 4200A on three-terminal devices by using three SMUs sweeping simultaneously. The gate and the source SMUs sweep at the same polarity simultaneously to avoid an on-state of the device. The drain SMU will sweep the opposite polarity of the source and gate, so that the differential voltage is doubled. This supports a voltage sweep up to 400 V at the drain, which is beneficial to test higher power semiconductors such as GaN.

Tektronix®

Forced Current Quasistatic C-V Method for SiC Devices



Introduction

Capacitance voltage (C-V) measurements are used for analyzing semiconductor materials and in semiconductor device fabrication. C-V is particularly useful for characterizing Metal-Oxide-Semiconductors (MOS). Some of the many MOS device properties extracted from C-V data include mobile charges in the oxide, oxide capacitance, interface traps, doping profile, flat band voltage, doping concentration, minority carrier lifetime and input/output capacitances.

For most semiconductor C-V measurements, high frequency (typically 100 kHz to 1 MHz) is used. However, for some C-V measurements, a low frequency, or quasistatic, technique is required. This is the case for interface trap density (DIT) measurements on a MOScap, where quasistatic C-V is able to detect interface traps. For Si MOSFETs, a charge pumping technique can be used for determining DIT. At high frequency, interface traps cannot change state rapidly enough to contribute to the device capacitance. As a result, both the high and low frequency measurements are required to determine the number of trapped charges.

Available quasistatic C-V solutions usually involve forcing a voltage and measuring current using a source measure unit (SMU). These techniques can be effective on traditional silicon MOS devices. However, with SiC MOS devices, the higher capacitance makes these ammeter techniques difficult to use because the higher capacitance can cause unstable results.

To avoid problems caused by measuring current and stepping voltages in quasistatic methods, the Keithley 4200A-SCS Parameter Analyzer uses the Forced Current Quasistatic C-V (Force-I QSCV) technique. This method forces current, measures voltage and time, and derives the capacitance. Some of the advantages to using the Force-I QSCV technique on a SiC power MOS device include:

- Requires only one SMU with a preamp (other methods use two).
- Forcing current is faster than force voltage methods.
- Forcing constant DC current to the DUT allows for a steady state condition unlike stepping voltages.
- Measures voltage: avoids instability problems when using an instrument in low output impedance mode to derive the capacitance.
- Calculates capacitance from the following equation:

$$I = C * \frac{dV}{dt}$$

- Performs open correction.
- Corrects for leakages.
- Provides similar results to C-V measurements taken with the Keithley 595 Quasistatic C-V Meter.
- Investigating if DIT can be extracted using forward and reverse curves.
- This technique works on larger capacitances > 20 pF.

Beginning with the Clarius V1.14 Software release, tests that perform the Force-I QSCV technique are included with the Clarius Software that comes with the Keithley 4200A-SCS. These tests are some of many included in the extensive test library provided in the 4200A-SCS Clarius+ Software Suite. A single SMU with a preamp is required to run the Force-I QSCV tests in Clarius.

This application note describes the Force-I QSCV technique, explains how to use the tests in the Clarius Software, compares this technique to other methods and derives calculations for internal charges on a SiC MOSFET from the forward and reverse C-V sweeps.

Force-I QSCV Technique Using Three Steps

The Force-I QSCV technique uses a single SMU with a preamp to derive the quasistatic C-V characteristics of a SiC MOSFET or MOScap. An SMU is an instrument that sources and measures current and voltage. As shown in **Figure 1**, the force HI terminal of the SMU is connected to the gate of the power MOSFET, and the force LO terminal of the SMU is connected to the drain and source terminals shorted together.

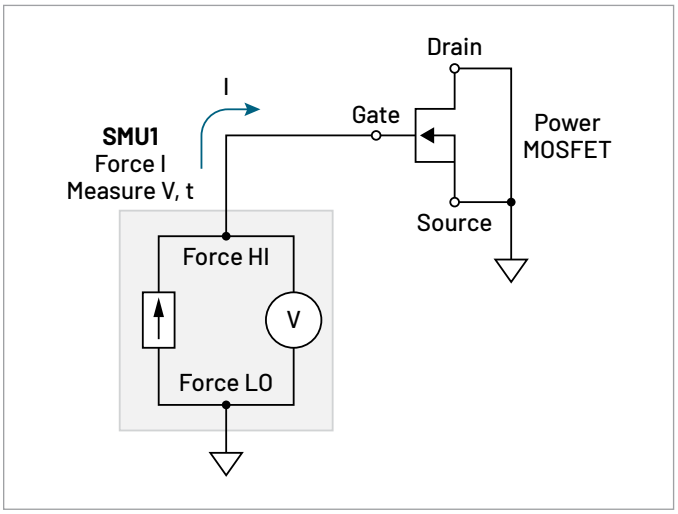


Figure 1. A power MOSFET is connected between the force HI and force LO terminals of the SMU.

The forced current quasistatic C-V method derives forward and reverse C-V curves using a three-step method by forcing positive and negative current while measuring voltage as a function of time. The constant current provides accurate control of the total charge (Q=∑I*dt) supplied to the device. Using constant current allows for a steady state condition for the instrument unlike voltage stepping that can cause dynamic changes in the measurement equipment. The voltage and current timing diagrams of the three steps are illustrated in **Figure 2** and are further explained in the paragraphs that follow.

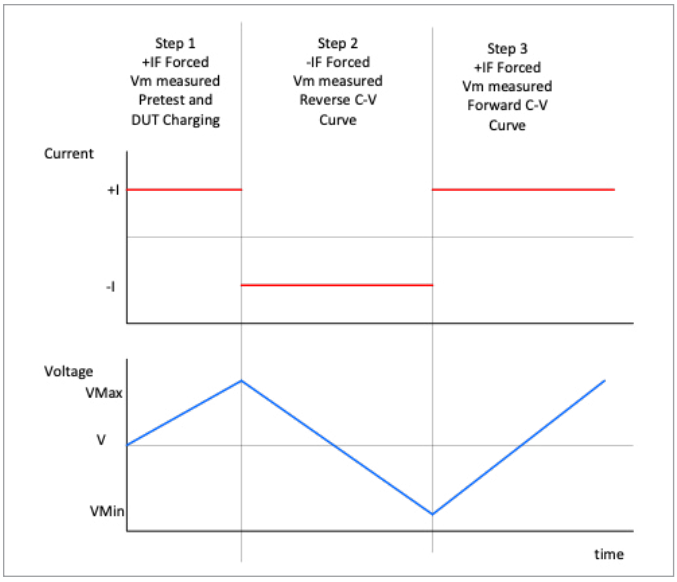


Figure 2. Current and voltage timing diagrams for Force-I QSCV test.

Step 1. The SMU forces a constant current (+I) and measures the voltage (V) and time until the voltage reaches a user defined maximum level, VMax. This step charges the device. The readings taken during this step are not used for the capacitance measurements.

Step 2. After VMax is reached, the polarity of the current source changes to -I and the voltage is measured until the predefined VMin is reached. During this step, the reverse C-V (Cr) sweep is derived.

Step 3. After VMin is reached, the polarity of the current source changes again to +I and the voltage is measured until VMax is reached. During this step, the forward C-V (Cf) sweep is derived.

Both the forward and reverse C-V curves can be extracted because both the positive and negative current was forced. The derived DUT capacitance (C) is calculated as follows:

$$I = C * \left(\frac{dV}{dt}\right), \text{ therefore } C = I \div \left(\frac{dV}{dt}\right)$$

where: I = forced current (A), V = measured voltage (V), t = time (s), C = derived capacitance (F).

Using the Clarius Software for Force-I QSCV

Tests using the Force-I QSCV method are located in both the Test and Project Libraries that can be found in the Select view by searching for the phrase "force-I QSCV" or just "qscv". Once the tests are found in the Test Library, they can be selected and then added to the project tree. The Test Library includes tests for both a SiC MOSFET (*sic-mosfet-force-i-qscv*) and a SiC MOScap (*sic-moscap-force-i-qscv*). These particular tests can be used with other devices, or a new test can be created by adding a custom test (UTM) to the project tree and using the *force_current_CV* user module found in the *QSCVulib* user library.

The following paragraphs describe the input parameters, output parameters, and analyzing the results of the Force-I QSCV test.

Input Parameters

The input parameters for the Force-I QSCV tests appear in the Configure View of Clarius as shown in **Figure 3**. The user sets both the maximum and minimum test voltages, output current and timing parameters. Open compensation and leakage correction are optional and can also be applied within the Configure View.

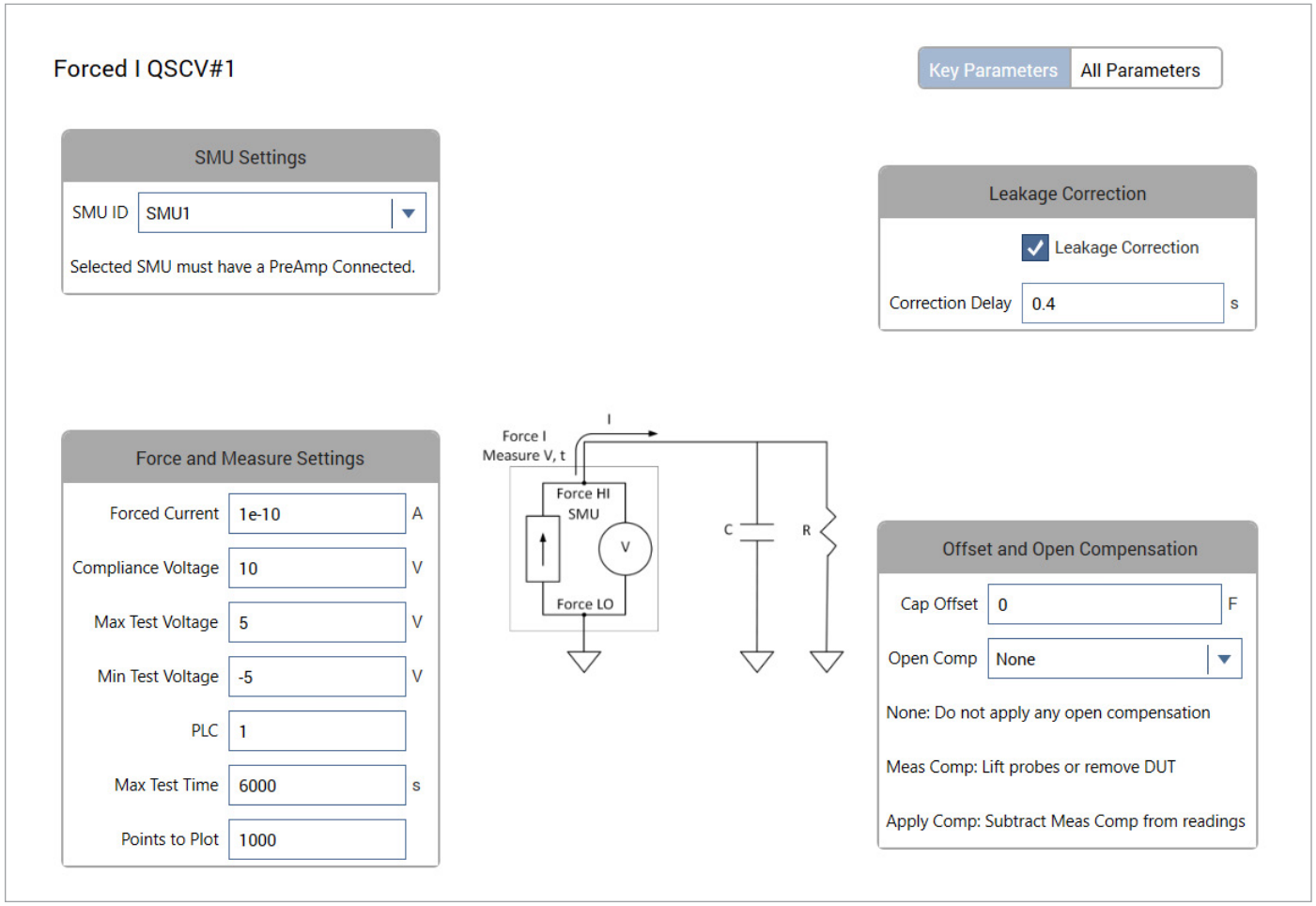


Figure 3. Configure view of the Force-I QSCV test in Clarius.

Table 1 lists all the input parameters with their descriptions and comments.

Table 1. Input parameters of Force-I QSCV test.

Input Parameter	Description	Comments
SMU ID	SMU# to be used in the test.	
Forced Current (A)	DC Current to be applied to DUT.	The lower the capacitance, the lower the test current.
Compliance Voltage (V)	Compliance voltage.	The compliance voltage is reached during the test.
Max Test Voltage (V)	Maximum test voltage to be applied to DUT.	
Min Test Voltage (V)	Minimum test voltage to be applied to DUT.	
Max Test Time (s)	The maximum allowable test time before the test times out.	
PLC	Integration time for both voltage and leakage current measurements.	Set from 0.01 to 10
Leakage Correction (A)	Checkbox for leakage correction.	Current leakage is measured and corrected at each point.
Correction Delay (s)	Settling time allowed after each voltage step. Setting only appears if Leakage Correction enabled.	Leakage is accomplished by forcing voltage, applying step delay, and measuring current.
Cap Offset	The offset to be applied to each capacitance measurement.	
Open Compensation	Choose to not enable Open Compensation (None), to measure the offset (Meas Comp), or apply the acquired offset (Apply Comp).	Open Compensation is a two-part process that is further explained in the paragraphs below.

The following paragraphs contain further information on some of the input parameters.

Forced Current. To choose an appropriate forced current may take some trial and error. The forced current typically is in the hundreds of picoamps to nanoamp range for a SiC MOSFET. The magnitude of the test current should be about a third of the magnitude of the maximum capacitance to be measured. For example, if the maximum capacitance is 2.4E-9 F than the test current should be about 800E-12 A. Using either too low or too high of test current may cause incorrect results.

Too low of test current may take longer for the device to charge up and the measurement time will be longer. Too high of a current will cause the test to reach the compliance voltage only after a few measurement points and return an error to the Sheet in the Analyze view.

The force current for the open compensation should be in the picoamp or less range. Too high of a current will cause the SMU to go into voltage compliance with no sufficient number of measurements collected. Too low of a current will cause very slow measurements.

PLC. The PLC timing setting adjusts the integration time of the measurement and can be set in the range of 0.01 to 10. However, it's best to use PLC values between 1 and 6.

This setting affects the measurement time as well as the voltage step size, which is the voltage difference between the readings. Ideally the step size should be between 50 mV and 100 mV. The voltage step size can be calculated using the DELTA function in the formulator. Increasing the PLC will improve noisy readings at the expense of longer measurement time.

Leakage Correction and Correction Delay. By default, leakage correction is disabled. If it is enabled, current leakage is measured and corrected at each voltage point. Leakage correction is done in three steps:

1. The C-V forward and reverse sweeps are derived using constant current.
2. Then the forward and reverse leakage current is measured at each voltage point returned in the first step.
3. Finally, the measured leakage current is used to correct the returned capacitance values (CrCorr and CfCorr). The leakage current is measured on a fixed current range and can be plotted in real time. Leakage correction uses the following equation for corrected capacitance:

$$C_{corrected} = C_{measured} * (1 - I_{measured}/I_{forced})$$

The corrected reverse capacitance, CrCorr, is plotted against Vr, and the corrected forward capacitance, CfCorr, is plotted against Vf. If the corrected capacitance appears to be noisy, increase the forced current and repeat the test.

The forced current (displacement current) must be higher than the leakage current otherwise the leakage current cannot be corrected. The displacement current is defined as I = C*(dV/dt).

An example of QSCV curves with and without leakage correction are shown in **Figures 4 and 5**. The test was run one time but both the uncorrected and corrected data were generated. **Figure 4** shows the forward (Cf) and reverse (Cr) C-V curves of a leaky SiC power MOSFET.

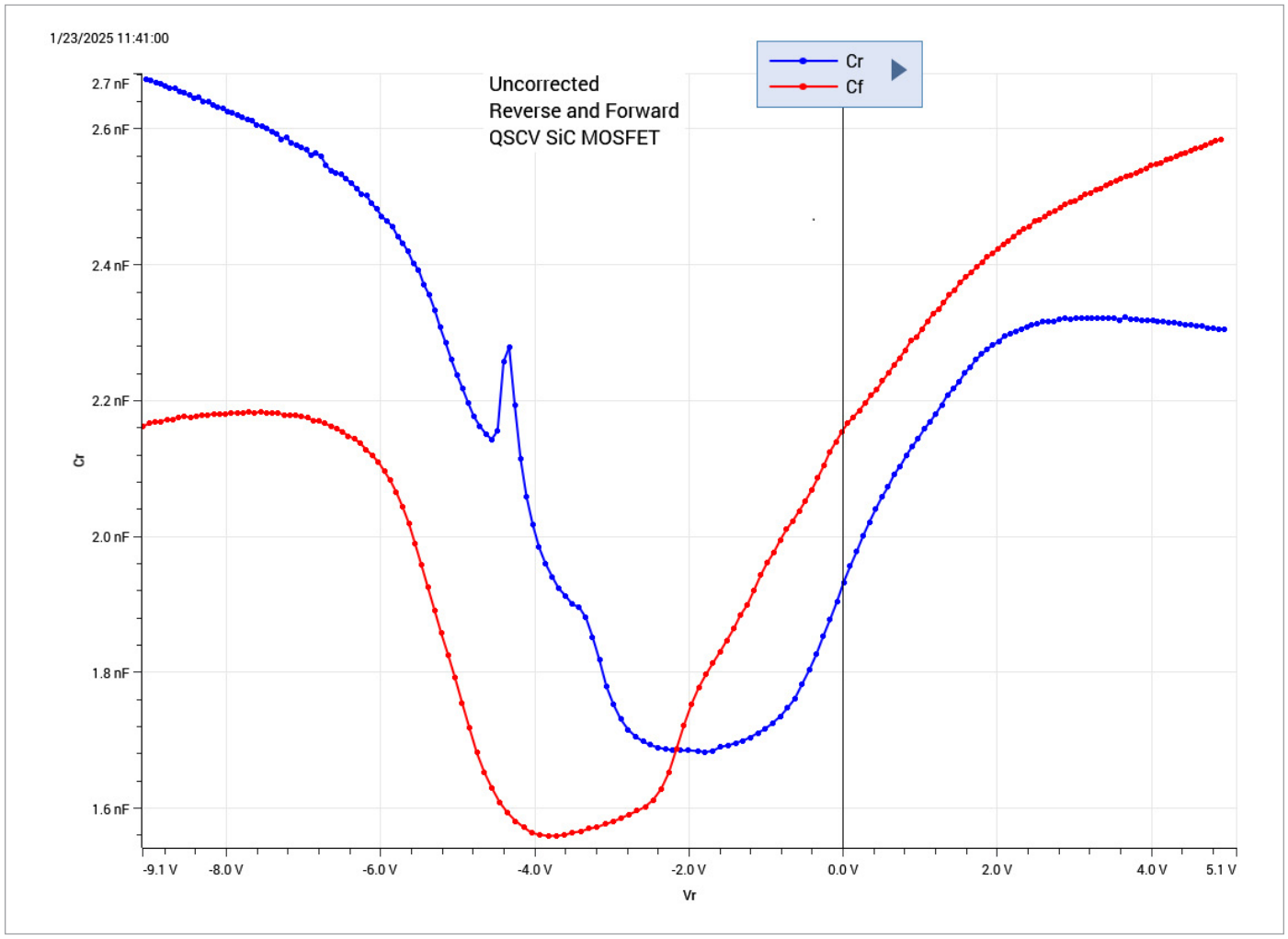


Figure 4. Forward and reverse quasistatic C-V curves of a leaky SiC MOSFET.

Figure 5 shows the results of the corrected forward (CfCorr) and reverse (CrCorr) C-V curves on the leaky device.

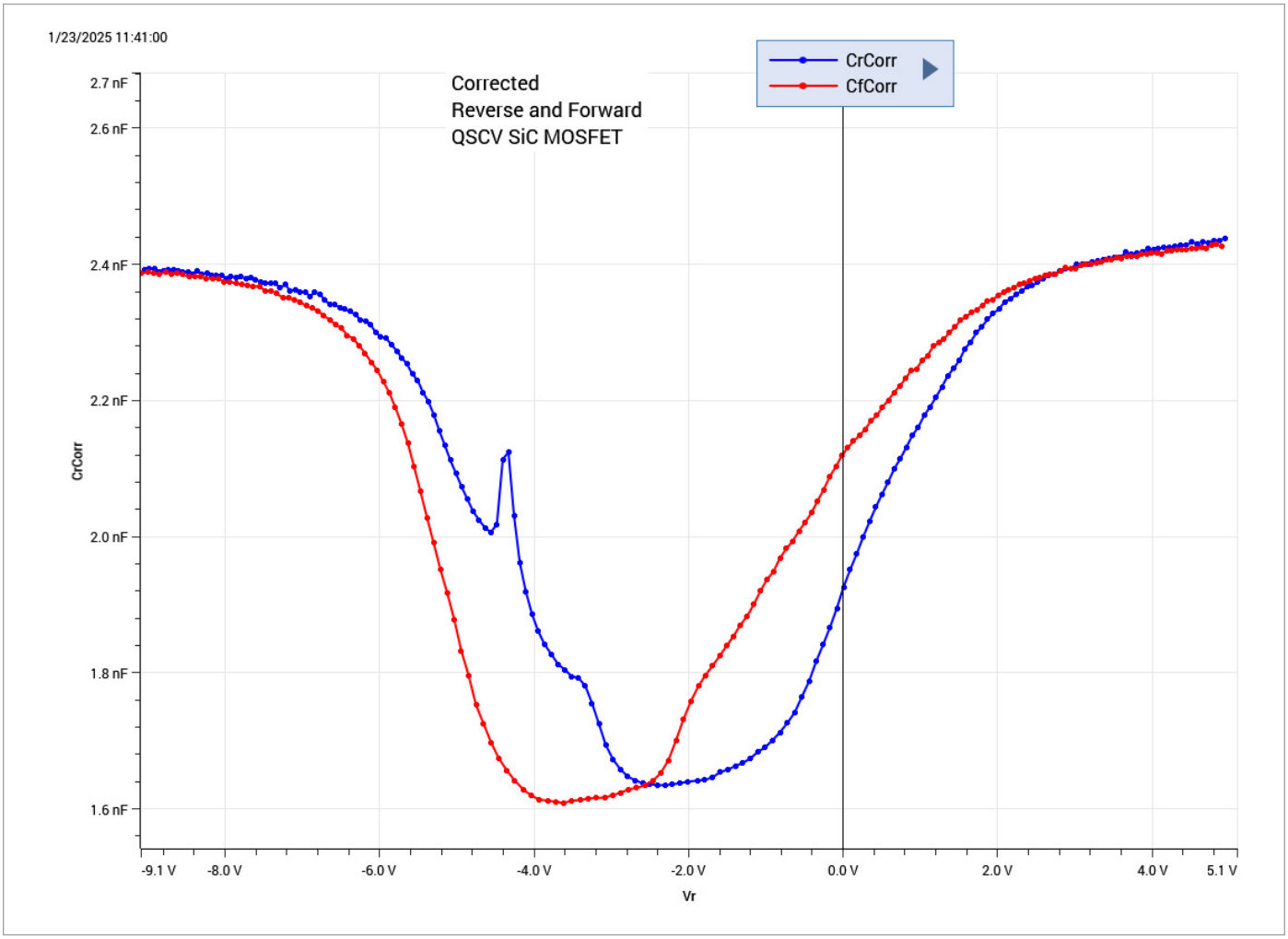


Figure 5. Corrected forward and reverse C-V curves on leaky SiC MOSFET.

Cap Offset and Open Compensation. Both cap offset and open compensation are used to correct for offsets due to capacitances in the test circuit such as cabling, test fixturing or probes. These two options are displayed in the Configure view of the tests as shown in **Figure 6**.

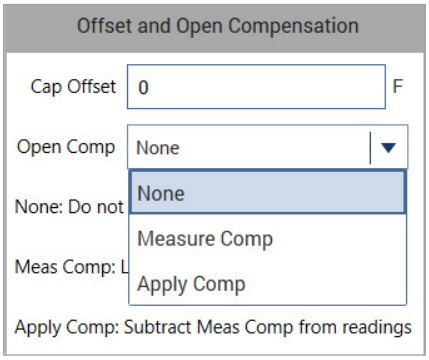


Figure 6. Offset and open compensation window.

By default, cap offset is set to 0 F, but the user can input a capacitance value that will be subtracted from both the forward and reverse capacitance readings.

Open compensation can be set to **None**, **Measure Comp** or **Apply Comp**.

If None is selected, then no open compensation measurements will be written to a file or applied.

If Measure Comp is enabled, the test is run with an open circuit with either the device removed from the test fixture or the probes up. There must be minimum of about 3–5 pF minimum capacitance to correct, otherwise an error (-35) will occur meaning that the SMU is in compliance. Typically, the forced current for an open circuit will be in the 1 E-13 A or less range to avoid the test from going into voltage compliance. Because the test current is so small,

the test will take several minutes to execute and acquire the offset capacitance. The average of the acquired open circuit data is stored in a file and will be subtracted from readings acquired using Apply Comp. The capacitance value that is subtracted is shown in the Sheet as Copen.

Once the test is Run with Measure Comp, then the DUT is connected in the test circuit and the test is Run again with Apply Comp enabled. Make sure to adjust the forced current to an appropriate level for the device. When the test is executed a second time, the average capacitance acquired (Copen) from Meas Comp will be subtracted from subsequent readings.

Analyzing the Results

Once the test is configured with the proper input settings, the test can be executed by selecting Run. When the test is run, a constant current is forced to the DUT as described in Steps 1, 2 and 3 to charge up the device and generate reverse and forward C-V curves.

The Analyze view graph will show the measurements results. The voltage vs. time measurements will appear in real time in the left-side graph and the forward and reverse C-V sweeps will appear in the right-side graph after the voltage measurements are finished.

The data is split into the reverse and forward C-V sweeps to accurately represent the measurements. For the reverse sweep, the reverse voltage (Vr), reverse sweep time (timeR) and reverse capacitance (Cr) are output. In the forward sweep, the reverse voltage (Vf), forward sweep time (timeF) and capacitance (Cf) are output.

Figure 7 shows the results in the Clarius graph view of testing a commercially available SiC power MOSFET using the *sic-mosfet-force-i-qscv* library test. For this test, a test current of 8 e-10 A and 4 PLC were used as test settings. The voltage step size is close to 80 mV using 4 PLC. Notice in the forward and reverse sweeps there is a shift in the voltage and peaks in the curves. Peaks were observed on the forward sweeps on the right side of the curve and on the reverse sweep on the left side of the curve. These shifts are usually attributed to internal device charge movement.

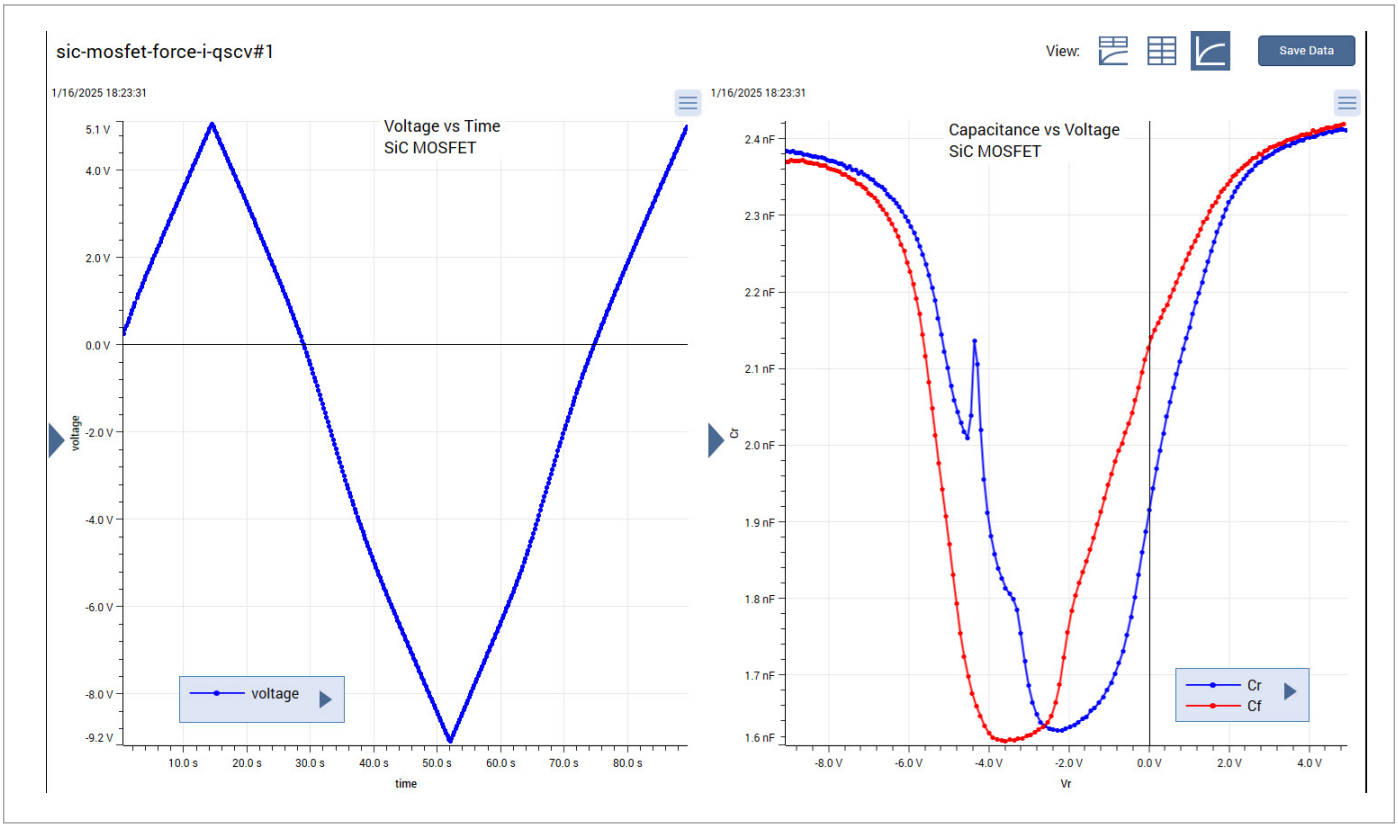


Figure 7. Voltage vs. time (left) and reverse and forward C-V graphs (right) of a SiC MOSFET.

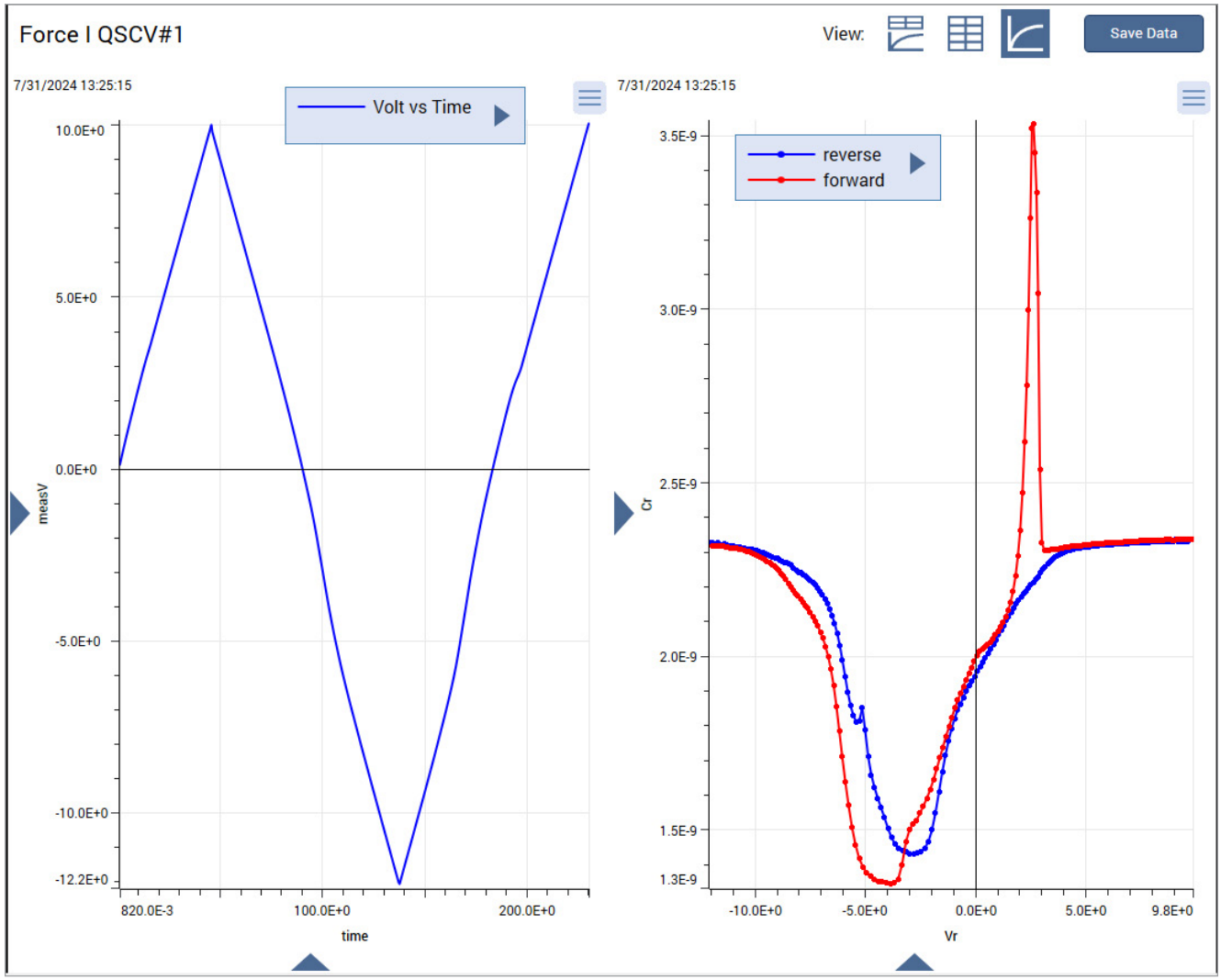


Figure 8. Forward and reverse quasistatic C-V sweeps on SiC MOSFET.

Example quasistatic C-V curves from a different commercially available SiC MOSFET are shown in **Figure 8**. In this case, the forward (red) curve has a "mobile ion" like peak that is not exhibited in the reverse sweep. For this test, the input parameters were set as follows: test current 5 e-10 A, 8 PLC, max voltage 10 V, min voltage -12 V, compliance 20 V.

In addition to looking at the data in the Graph tool, several parameters are returned to the Sheet in the Analyze View. These output parameters are listed in the following tables and are separated in the order shown in the Sheet as well as grouped into these categories: primary output parameters, reverse output parameters, forward output parameters, parameters used for DIT extraction, and miscellaneous parameters.

Table 2. Primary output parameters.

Output Parameter	Description	Comments
Voltage (V)	Voltage measured as a function of time across the device. Voltage = Vg.	Check to make sure the step size is between about 50 mV to 100 mV.
Vs (V)	Surface Potential defined as Vs=Vg-(Q/Cox) where Vg=Voltage	
charge (C)	Charge is defined as Q=∑I*dt supplied to the device (coulombs)	
time (s)	Time at each point	

Table 3. Reverse output parameters

Output Parameter	Description	Comments
Vr (V)	Reverse voltage from Step 2.	
Vrs (V)	Calculated surface potential for reverse voltage defined in Step 2.	Vsr=Vg-(Q/Cox), where Vg=Voltage
timeR (s)	Time array for the reverse sweep	
Cr (F)	Capacitance from reverse voltage sweep	
Ir (A)	Measured leakage current.	Leakage current is measured by forcing voltage at each voltage step in the Cr sweep and then measuring the current.
CrCorr (F)	Capacitance corrected to compensate for leakage current.	CrCorr = Cox(1-Ir/Iforce) where Iforce = Forced Current

Table 4. Forward output parameters.

Output Parameter	Description	Comments
Vf (V)	Forward voltage from Step 2.	
Vfs (V)	Calculated surface potential for forward voltage defined in Step 2.	Vfs=Vg-(Q/Cox), where Vg=Voltage
timeF (s)	Time array for the forward sweep.	
Cf(F)	Capacitance from forward voltage sweep.	
If (A)	Measured leakage current.	Leakage current is measured by forcing voltage at each voltage step in the Cf sweep and then measuring the current after the input Step Delay.
CfCorr (F)	Capacitance corrected to compensate for leakage current	CfCorr = Cox(1-If/Iforce) where Iforce = Forced Current

Table 5. Parameters used for DIT extraction.

Output Parameter	Description	Comments
CrDut (F)	Interpolated reverse capacitance.	
CfDut (F)	Interpolated forward capacitance.	
CrOnly (F)	Interpolated reverse capacitance with Cox removed.	
CfOnly (F)	Interpolated forward capacitance with Cox removed.	
Cdut_diff (F)	An array of values that represent the difference between the forward (CfOnly) and reverse (CrOnly) DUT capacitance values.	Plot with Vdut_diff.
Vdut_diff (V)	An array of differential voltage values that correspond to the surface potential	Plot with Cdut_diff.

Table 6. Miscellaneous output parameters.

Output Parameter	Description	Comments
Cox (F)	Maximum capacitance of both the Cr and Cf data.	
Copen (F)	Value used for open compensation	Copen is always returned even though this value doesn't get written to the file unless Meas Comp is selected.

Optimizing the Force-I QSCV Method

Minimum Capacitance. The minimum capacitance that can be measured is between 10–20 pF. This method is recommended for SiC devices that typically have capacitances in the nF range.

Electrostatically Shield the Device. Because this method involves detecting very small charges, it is important to electrostatically shield the device under test to avoid noisy measurements.

Voltage Step Size. The voltage step size should be between 50–100 mV for optimal results. The voltage step size can be adjusted by changing the PLC. The voltage step size can be measured using the DELTA function in the Formulator of the measured "voltage" in the Sheet.

Forced Current. Choosing the appropriate test current may take some trial and error. Too low of current will cause long test times. Too high of current will cause the test to reach compliance.

Open Compensation. In most cases of measuring QSCV on SiC devices, open compensation will not be necessary because cable and test fixturing capacitance (10 s of pF) is usually much smaller than the DUT capacitance (nF).

Force-I QSCV vs. Keithley 595 Quasistatic C-V Meter

The Keithley 595 Quasistatic C-V Meter, now obsolete, was used to make quasistatic C-V measurements on semiconductor devices. The 595 used a feedback charge method to measure capacitance. This method measured coulombs to derive the capacitance unlike most methods available today that measure current.

Comparisons were made between forward and reverse C-V curves taken with the 595 and the Force-I QSCV method on both SiC MOScaps on a wafer and commercially available SiC MOSFETs. Results of the forward and reverse quasistatic C-V curves taken on a SiC MOScap are shown in **Figure 9**. Notice the curves from the two methods overlap.

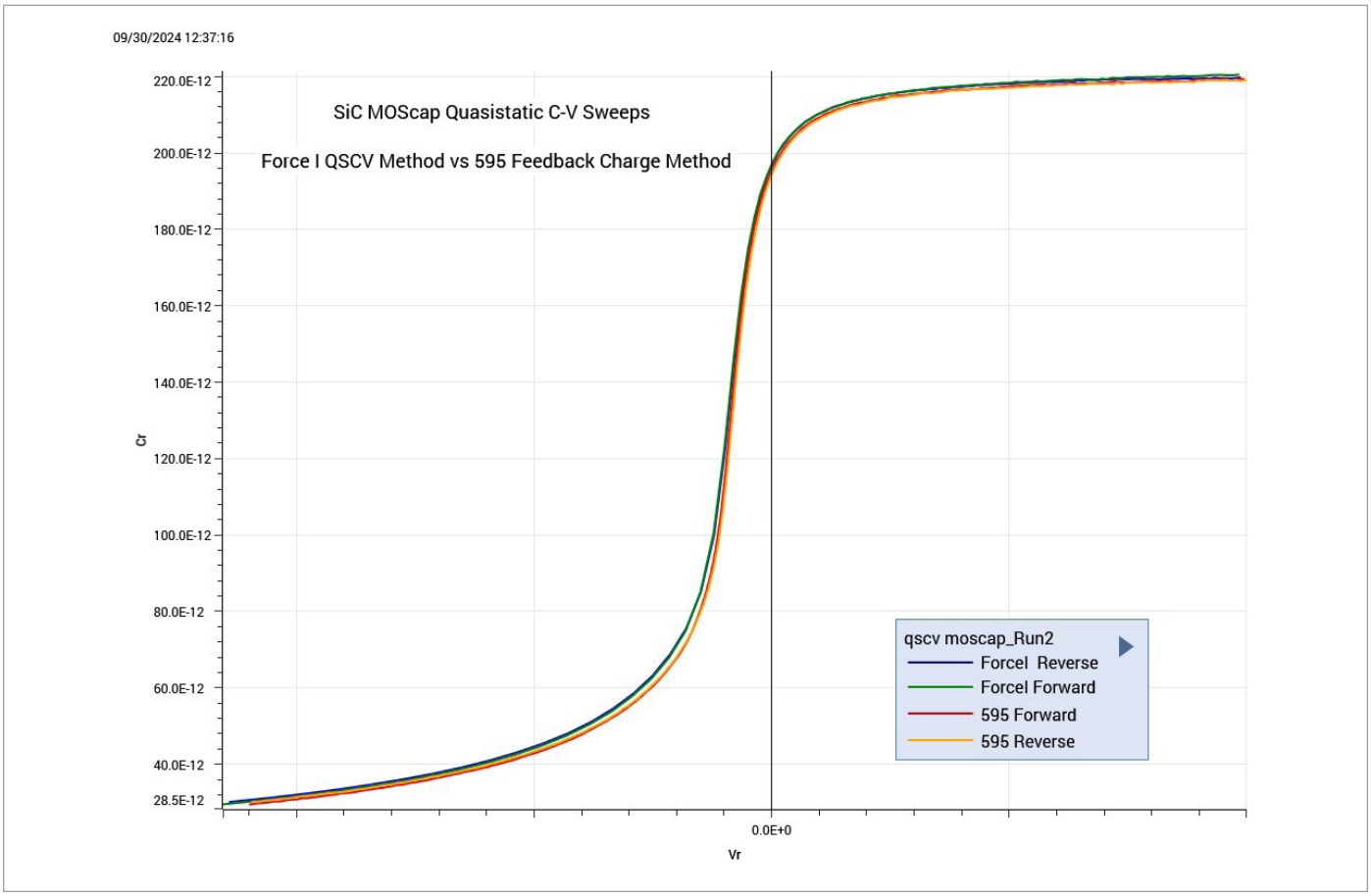


Figure 9. 595 and Force-I QSCV SiC MOScap forward and reverse quasistatic C-V curves.

Figure 10 shows graphs using both methods taken on a packaged SiC MOSFET. Notice the Force-I QSCV curves are less noisy than the 595 data, but in general, the curves correlate nicely.

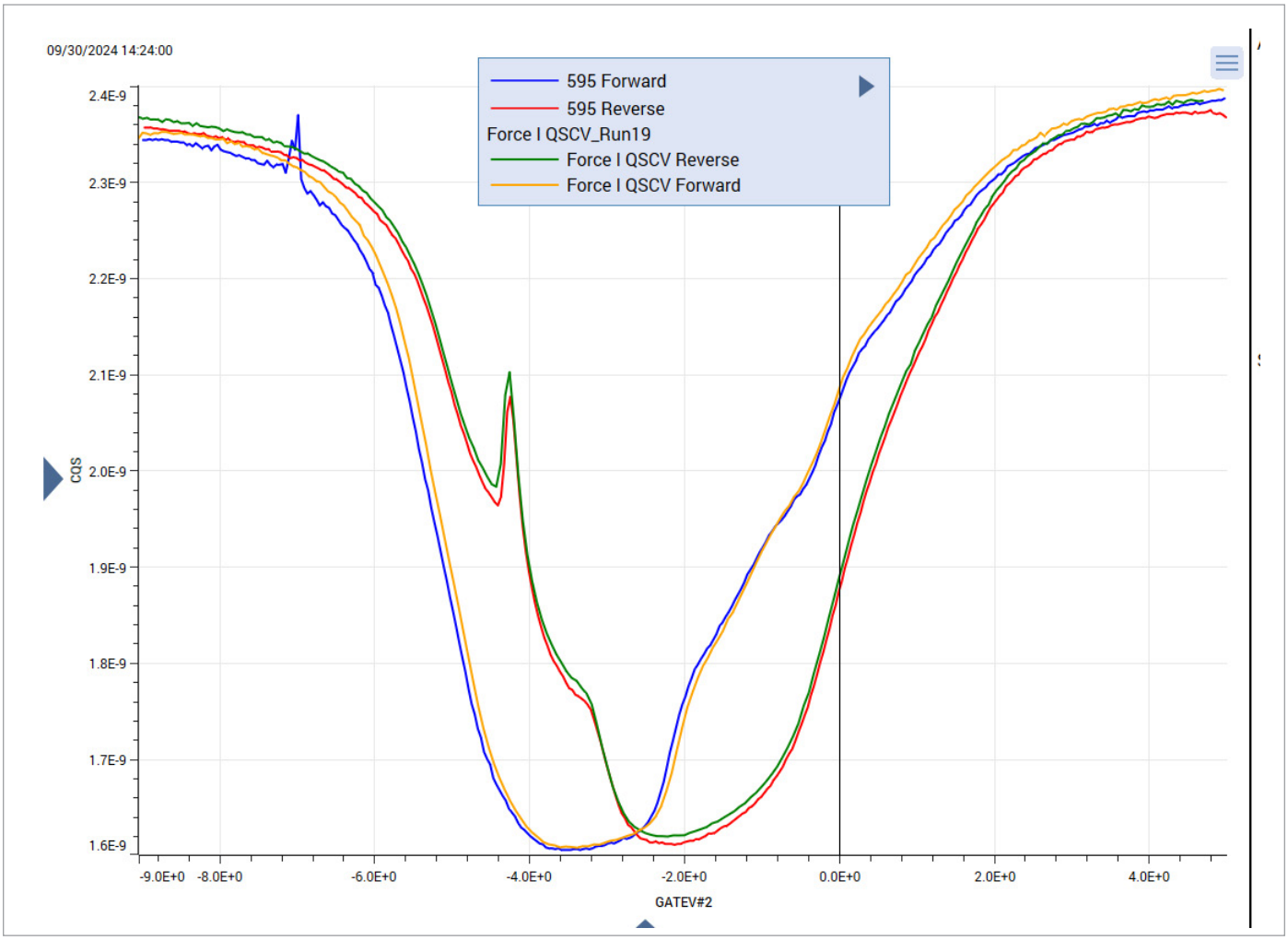


Figure 10. Both 595 and Force-I QSCV forward and reverse curves on SiC MOSFET.

Force-I QSCV vs. High Frequency C-V

Comparisons of C-V curves taken with the Force-I QSCV method and high frequency AC measurements (using the 4215-CVU Capacitance Voltage Unit) were also observed. The results are shown in **Figure 11**. The CVU data (green curve) encompassed both the forward and reverse quasistatic curves from both the 595 and the Force-I QSCV methods. The high frequency CVU data did not show any "peaks" in the curve.

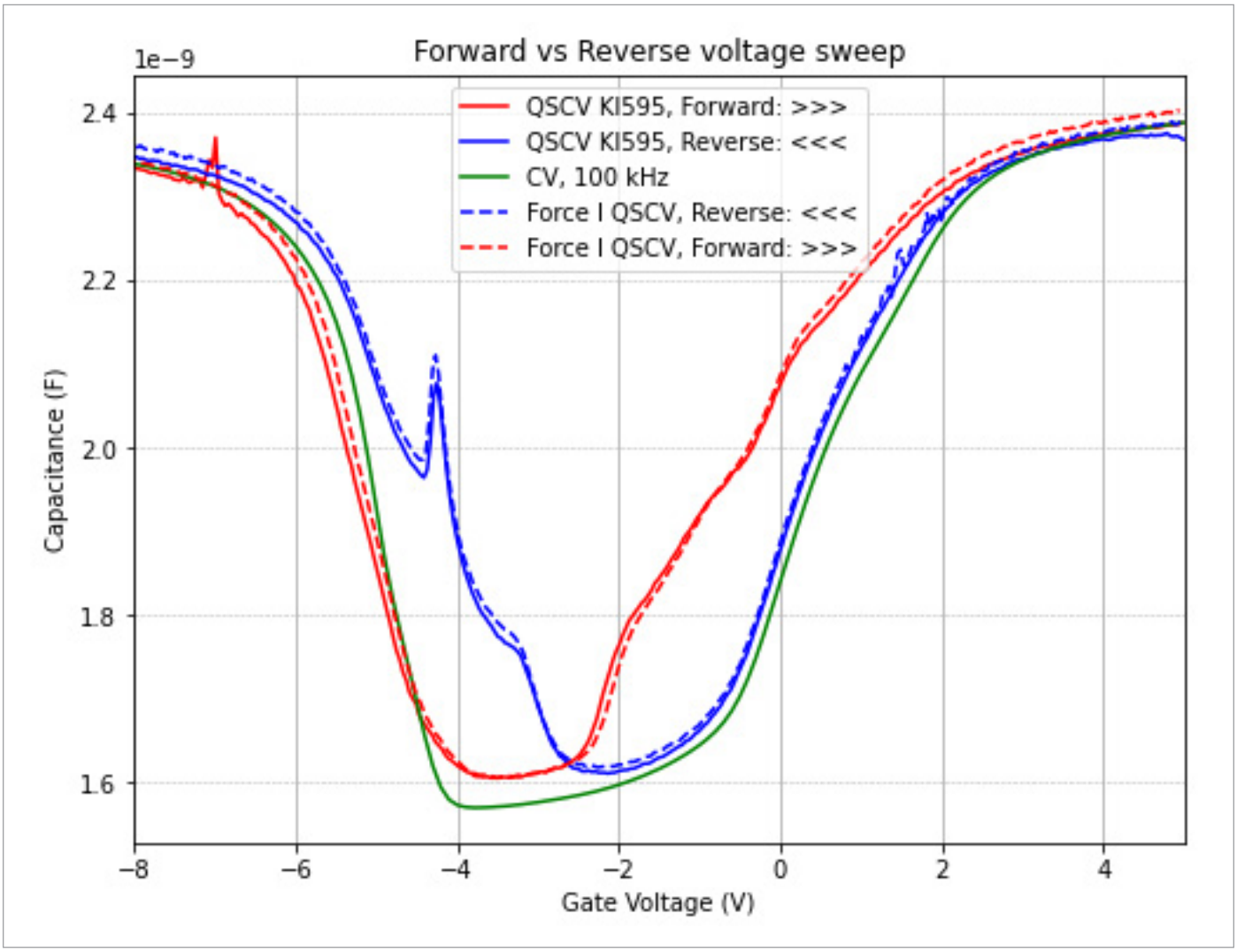


Figure 11. High frequency and quasistatic C-V sweeps on packaged SiC MOSFET.

C-V Measurements and Interface Trap Density on SiC MOS Devices

At the time of this writing (March 2025), we are in the process of verifying that the suggested interface trap density (DIT) calculations on both SiC MOSFETs and MOScaps using the Force-I QSCV method correlate with other known techniques, such as the comparison of combined low and high frequency capacitance measurements. The following paragraphs discuss these derivations.

SiC MOSFETs

Traditionally, the interface trapped charge of a silicon MOS cap was extracted from the capacitance difference of a low frequency (quasistatic) C-Vg curve and a high frequency (AC) C-Vg curve. We've learned that to observe internal charges of a SiC MOSFET, the forward and reverse quasistatic C-Vg sweeps can be used to extract this charge.

Because SiC MOSFETs have significantly more internal charges than traditional Si devices, the measured capacitance needs to be plotted against the surface potential (Vs) as opposed to the gate voltage (Vg) for calculations of trapped charges. Because charge is measured, the interface potential can be calculated. This enables the capacitance to be characterized as a function of the interface potential. In standard techniques, it's difficult to extract the interface potential because it's difficult or impossible to measure the oxide charge at a high frequency. Therefore, comparisons are usually made as a function of the gate voltage and not the interface potential.

The technique for deriving this interface trap capacitance can be summarized into five steps:

1. Generate forward (Cf) and reverse (Cr) quasistatic capacitance vs. gate voltage (Vg) curves on a SiC MOSFET using the Force-I QSCV method.
2. Derive surface potential (Vs) arrays for both forward and reverse sweeps.
3. Interpolate the forward capacitance (CfDut) and reverse capacitance (CrDut) at each surface potential point.
4. Subtract the oxide capacitance (Cox) from the forward (CfDut) and reverse (CrDut) measurements.
5. Calculate the capacitance (CIT) and interface trap density (DIT) due to trapped charge from the difference of the forward and reverse curves as a function of the surface potential.

These five steps are further explained in the following paragraphs:

Step 1. Generate Forward and Reverse Quasistatic C-V Curves.

Generate forward (Cf) and reverse (Cr) quasistatic capacitance vs. gate voltage (Vg) curves on a SiC MOSFET using the Force-I QSCV method.

From the forward and reverse C-V sweeps there is both a shift in the voltage between the two curves as well as "peaks" and smaller curve features (see Figures 4 and 5). We believe both the voltage shift and "peaks" are a result of internal devices charges such as trapped charges or mobile ion charge, or charges related to the device structure. Interestingly, when a high frequency C-V sweep is generated, the voltage shift and peaks are not observed.

Step 2. Derive Surface Potential (Vs) Arrays for both Forward and Reverse Sweeps

The capacitances of forward and reverse voltage sweeps of a MOS device are usually compared at the same gate voltage (Vg). Because SiC MOSFETs have significant internal charges, we compared the forward and reverse quasistatic curves as a function of the surface potential (Vs) instead. Using Vs corrects for the "shifts" seen in the gate voltage between the forward and reverse curves and allows for the curves to be compared. Accurately measured charge allowed us to correct for the voltage drop across the gate oxide to extract Vs.

Figure 12 shows the SMU applying a constant current to a SiC MOS DUT as well as the voltages, Vg and Vs. The voltage at the gate terminal of the device is Vg. The voltage at the SiC/SiO2 interface is the surface potential (Vs) and is represented by the equation:

$$Vs = Vg - Vox, \text{ where } Vox = Q/Cox$$

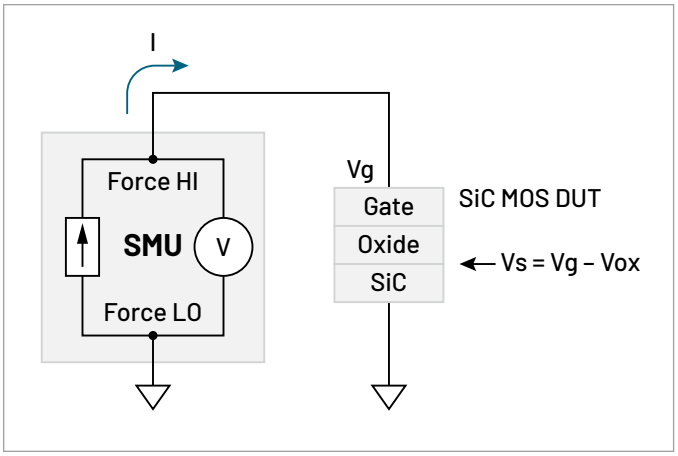


Figure 12. A SMU connected to SIC MOS Dut with circuit potentials.

First, the reverse and forward capacitance arrays (Cr and Cf) are analyzed to find the maximum value from either array. The maximum capacitance is defined as Cox, or oxide capacitance.

Then, from each gate voltage (Vg), the surface potential Vs is calculated using the oxide capacitance (Cox) and calculated charge (Q):

$$Vs = Vg - \frac{Q}{Cox}$$

Finally, the surface potential is split into two separate arrays for both sweeps. The output parameter, VsR, represents the reverse sweep surface potential, and VsF represents the forward sweep surface potential.

Step 3. Interpolate the forward capacitance (CfDut) and reverse capacitance (CrDut) at each surface potential point.

The forward and reverse data sets were collected at different gate voltages, but they need to be compared at the same surface potential. To do this, a linear interpolation algorithm is used.

The following process is used for linear interpolation:

a. Determine the number of voltage step points but using the following equation:

$$\Delta V = \frac{Vmax - Vmin}{(points\ to\ plot) - 1}$$

b. Run the linear interpolation twice, once for the reverse sweep and another for the forward sweep to extract the interpolated capacitance points. The forward and reverse interpolated capacitance arrays are CrDut and CfDut.

Figure 13 shows both the forward and reverse capacitance curves, CfDut and CrDut, plotted as a function of interface voltage instead of gate voltage.

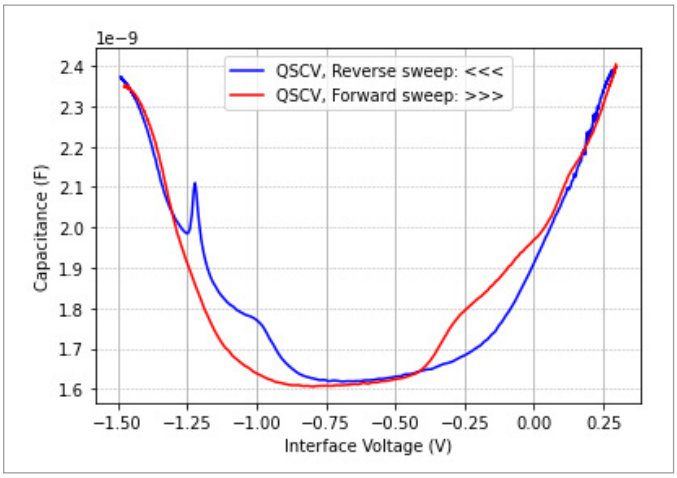


Figure 13. Forward and reverse capacitance curves as a function of Vs.

Step 4. Subtract the Oxide Capacitance from the Forward (CfDut) and Reverse (CrDut) Measurements.

Subtract and maximum capacitance (Cox) from all CrDut and CfDut values. To do this, the linear interpolation algorithm is run using the reverse and forward voltage surface potential values, VsR and VsF. The forward and reverse interpolated capacitance arrays are calculated, and in each function, the Cox value is removed at each point, using the following two equations:

$$Cf\ Only = \frac{1}{\frac{1}{Cf\ Dut} - \frac{1}{Cox}}$$

$$Cr\ Only = \frac{1}{\frac{1}{Cr\ Dut} - \frac{1}{Cox}}$$

In **Figure 14**, with Cox removed, CrOnly and CfOnly are plotted as a function of interface voltage, now in a logarithmic scale.

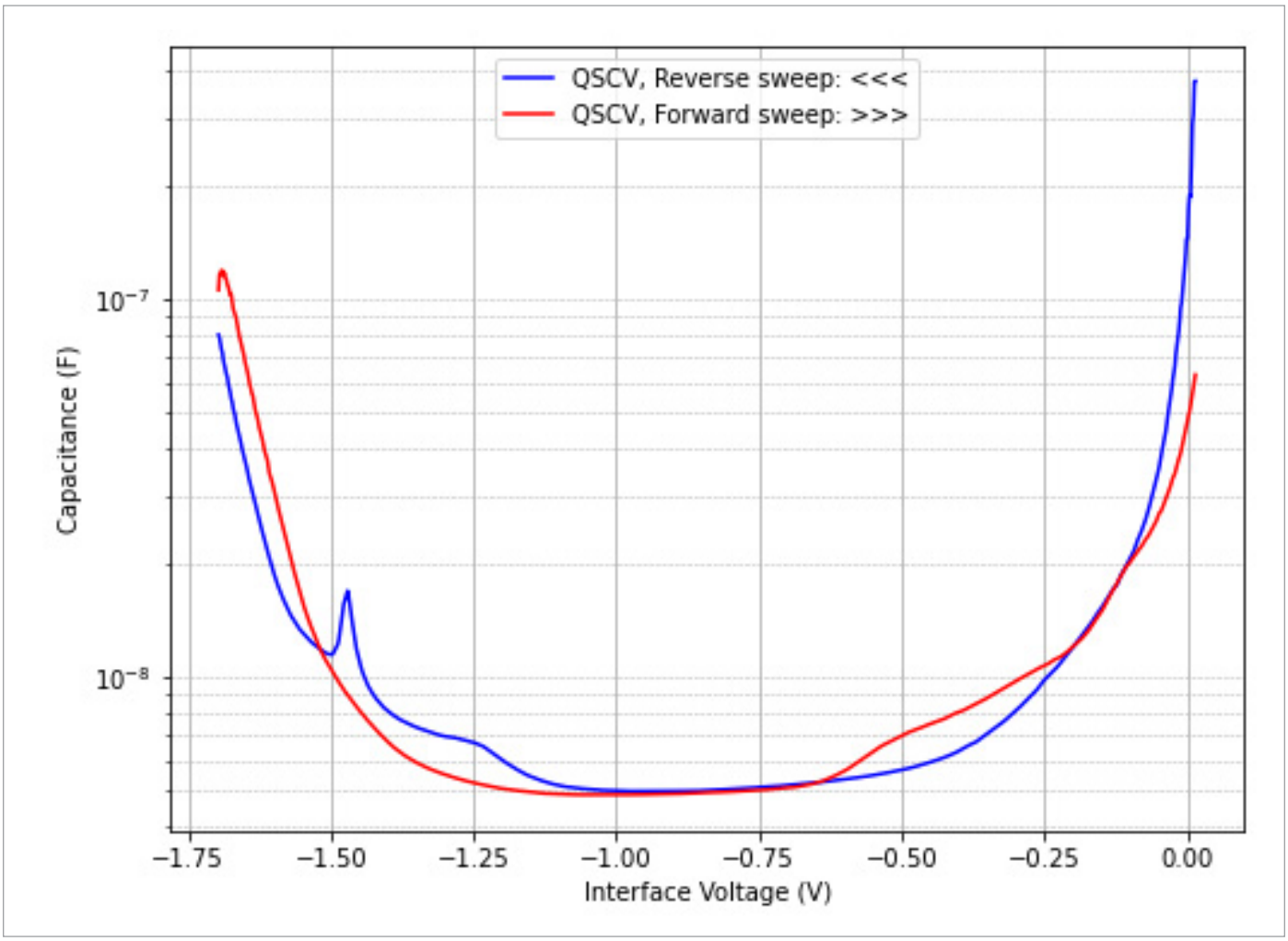


Figure 14. Cf and Cr curves with Cox removed as a function of Vs.

Step 5. Calculate the interface trapped capacitance (CIT) and density (DIT)

Calculate the capacitance (CIT) due to trapped charge from the difference of the corrected forward and reverse curves as a function of the surface potential.

$$CIT = [C_{Fonly}(V_s) - C_{Ronly}(V_s)] / \text{ gate area}$$

The interface trap density (DIT) is also derived using the following equation:

$$DIT = [C_{Fonly}(V_s) - C_{Ronly}(V_s)] / (\text{gate area} * q)$$

Figure 15 shows a plot of the interface trap density (DIT) as a function of surface potential (Vs).

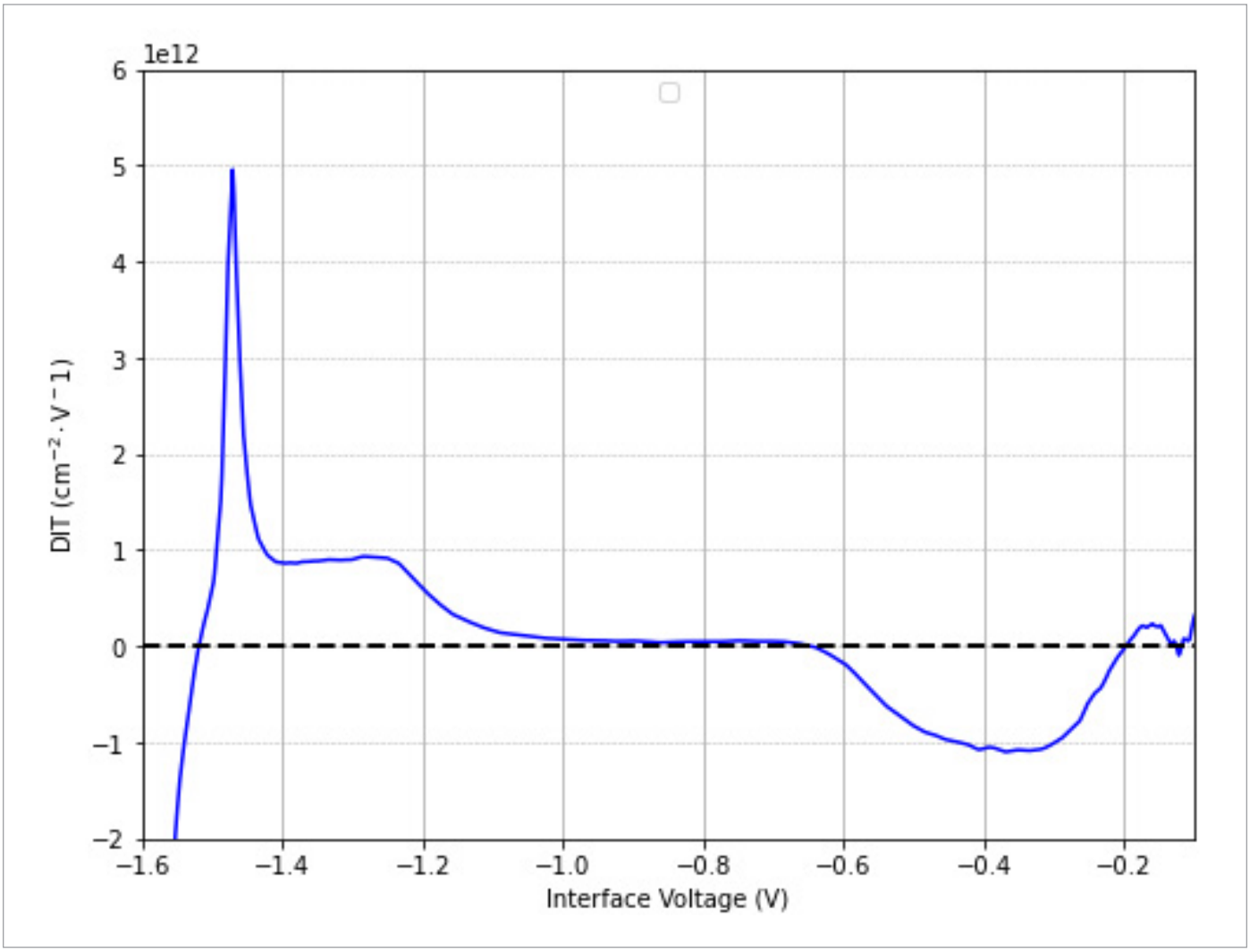


Figure 15. Plotted difference between the interpolated forward and reverse capacitances vs. interface voltage (Vs).

SiC MOScap

For interface trap density (DIT) measurements on a MOScap, a combination of both high and low frequency measurements is used. When generating both high frequency and quasistatic C-V curves, make sure the voltage step size is much smaller than the voltage difference between the two curves. The voltage step size can be reduced by decreasing the PLC value.

We are still investigating the DIT extraction of both SiC MOScaps and MOSFETs using the Force-I QSCV technique.

Conclusion

The Force-I QSCV technique enables quasistatic C-V measurements on SiC MOS devices. This method acquires two sets of data from forward and reverse sweeps as well as voltage vs. time data obtained by forcing positive and negative currents. With the total charge known, this method allows for the extraction of capacitance and charge at the semiconductor interface. Differential analysis of forward and reverse sweeps enables direct extraction of the density of interface traps (DIT).

Appendix 1. Error Codes

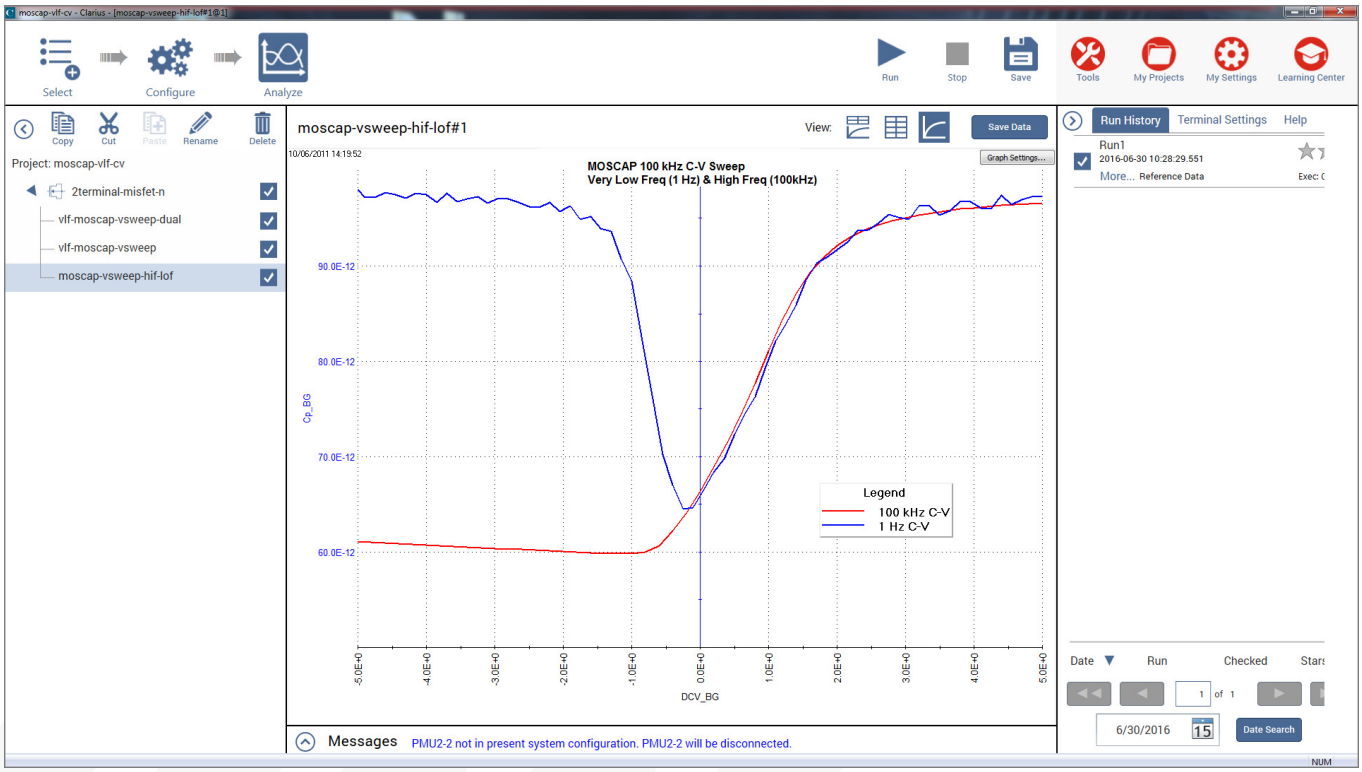
These error codes in **Table 7** appear in the first column, first row of the Sheet in the Analyze view after the test is executed. Below is a description of the error and provide help on what to do.

Table 7. Error codes for the *force_current_cv* user module.

Error Codes	Description
0	OK.
-20	The forced current is less than the minimum current of 5e-14 Amps. Increase the forced current.
-21	Min Test Voltage (vLow) or Max Test Voltage (vHigh) exceeds the absolute voltage limit (vLimit). Decrease the Min or Max Test Voltage or increase the compliance voltage.
-22	Max Test Voltage (vHigh) is smaller than Min Test Voltage (vLow). Increase the Max Test Voltage or decrease the Min Test Voltage.
-23	Polarity of the Forced Current (Iforce) is not consistent with polarity of Min Test Voltage (vLow) and Max Test Voltage (vHigh). Change the polarity of the forced current.
-30	Selected SMU is not present in the system.
-35	In the initial sweep the absolute measured voltage is greater than the absolute voltage limit. Increase the compliance voltage. The measured capacitance is too small to measure. The minimum measurable capacitance is about 10-20pF.
-37	Internal memory values could not be allocated. Please check system memory usage.
-40	The initial sweep count is greater than the maximum number of steps. Increase the forced current, PLC, or maximum number of steps.
-50	Test time during the initial sweep exceeded the maximum time. Increase the max test time or forced current.
-55	Not enough initial points to continue the test. Decrease the forced current. Minimum capacitance is too small.
-60	The reverse sweep count exceeded the maximum number of steps. Increase the forced current, PLC, or maximum number of steps.
-70	Test time during the reverse sweep exceeded the maximum time. Increase the max test time or forced current.
-76	In the reverse sweep the absolute measured voltage is greater than the absolute voltage limit. Increase the compliance voltage.
-90	The forward sweep count exceeded the maximum number of steps. Increase the forced current, PLC, or maximum number of steps.
-100	Test time during the forward sweep exceeded the maximum time. Increase the max test time or forced current.
-104	In the forward sweep the absolute measured voltage is greater than the absolute voltage limit. Increase the compliance voltage.
-110	Error during writing the offset to the filesystem. Check write access to C:\\S4200\\kiuser\\coffset.csv

Tektronix®

Performing Very Low Frequency Capacitance-Voltage Measurements on High Impedance Devices Using the 4200A-SCS Parameter Analyzer



Introduction

Capacitance measurements on semiconductor devices are usually made using an AC technique with a bridge-type instrument. These AC instruments typically make capacitance and impedance measurements at frequencies ranging from megahertz down to possibly tens of hertz. However, even lower frequency capacitance measurements are often necessary to derive specific test parameters of devices such as MOScaps, thin film transistors (TFTs), and MEMS structures. Low frequency C-V measurements are also used to characterize the slow trapping and de-trapping phenomenon in some materials. Instruments capable of making quasistatic (or almost DC) C-V measurements are often used for these low frequency impedance applications. However, the 4200A-SCS Parameter Analyzer uses a new narrow-band technique that takes advantage of the low current measurement capability of its integrated source measure unit (SMU) instruments to perform C-V measurements at specified low frequencies in the range of 10 mHz to 10 Hz. This new method is called the Very Low Frequency C-V (VLF C-V) Technique.

The VLF C-V Technique makes it possible to measure very small capacitances at a precise low test frequency. This patent-pending, narrow-band sinusoidal technique allows for low frequency C-V measurements of very high impedance devices, up to >1E15 ohms. Other AC impedance instruments are usually limited to impedances up to about 1E6 to 1E9 ohms. The VLF C-V approach also reduces the noise that may occur when making traditional quasistatic C-V measurements.

The 4200A-SCS Parameter Analyzer comes with preconfigured tests and a user library to perform impedance measurements automatically using this very low frequency technique. Because this approach uses the 4200A-SCS's SMU instruments, no additional hardware or software is necessary if low current I-V characterization is already required. This application note describes the VLF C-V technique, explains how to make connections to the DUT, shows how to use the provided software, and describes optimizing VLF C-V measurements using the 4200A-SCS.

Very Low Frequency C-V Technique

Figure 1 is a simplified diagram of the SMU instrument configuration used to generate the low frequency impedance measurements. This configuration requires a 4200A-SCS system with two SMU instruments installed, with 4200-PA preamps connected to either side of the device under test. SMU1 outputs the DC bias with a superimposed AC signal and also measures the voltage. SMU2 measures the resulting AC current while sourcing 0 V DC.

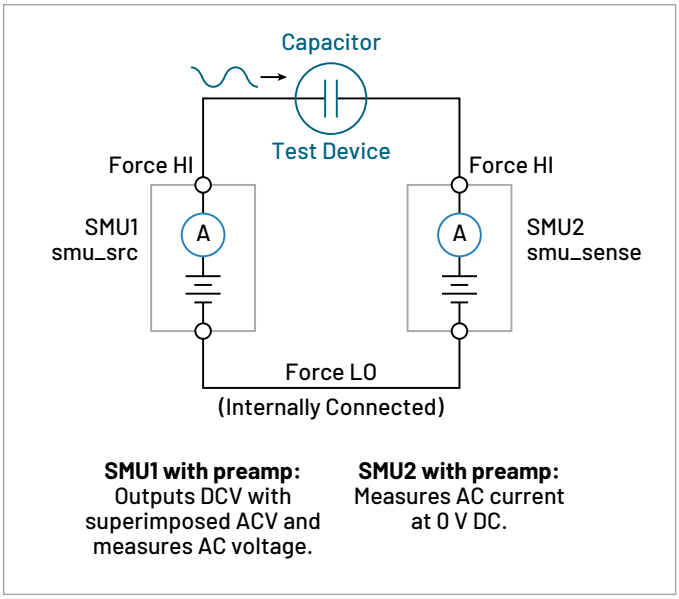


Figure 1. Connections for very low frequency C-V measurements.

Basically, while the voltage is forced, voltage and current measurements are obtained simultaneously over several cycles. The magnitude and phase of the DUT impedance is extracted from the discrete Fourier transform (DFT) of a ratio of the resultant voltage and current sinusoids. This narrow-band information can be collected at varying frequencies (10mHz to 10Hz) to create a complex, multi-element of the DUT. The resulting output parameters include the impedance (Z), phase angle (θ), capacitance (C), conductance (G), resistance (R), reactance (X), and the dissipation factor (D).

Because the very low frequency method works over a limited frequency range, the capacitance of the device under test (DUT) should be in the range of 1pF to 10nF. **Table 1** summarizes the VLF C-V specifications (see Appendix A for complete specifications).

Table 1. Very Low Frequency C-V specifications.

Measurement Parameters	Cp, Gp, F, Z, θ, R, X, Cs, Rs, D, time
Frequency Range	10 mHz to 10 Hz
Measurement Range	1 pF to 10 nF
Typical Resolution	3.5 digits, minimum typical 10 fF
AC Signal	10 mV to 3 V RMS
DC Bias	±20 V on the High terminal, minus the AC signal, 1 µA maximum

Required Hardware for VLF C-V Measurements

To make very low frequency impedance measurements, the following hardware is required:

- 4200A-SCS with Clarius software
- Two SMU instruments (4200-SMU, 4201-SMU, 4210-SMU, or 4211-SMU)
- Two 4200-PA Preamps
- Optional: 4210-CVU or 4215-CVU Capacitance Voltage Unit (CVU) for making high frequency C-V measurements

Making Connections to the Device

To make VLF C-V measurements on a device, connect the DUT between the two Force HI terminals of two SMU instruments (4200-SMU, 4201-SMU, 4210-SMU or 4211-SMU) with 4200-PA Preamps (**Figures 1, 2**). The preamp option is necessary because measuring very high impedances requires measuring very small currents. With the 4200-PAs, currents of <1E-12A can be measured. Because the VLF C-V method requires measuring small currents, it is best to use the triax cables that come with the SMU instruments to make these connections. The method does not support any switching instrumentation between the SMU instrument preamp and the device under test (DUT). One SMU outputs both the DC and AC voltage (SMU1 in **Figures 1 and 2**) and measures the AC voltage. The other SMU instrument measures the AC current (SMU2 in **Figures 1 and 2**). The SMU instrument used to measure the AC current should be connected to the high impedance terminal of the device (**Figure 2**).

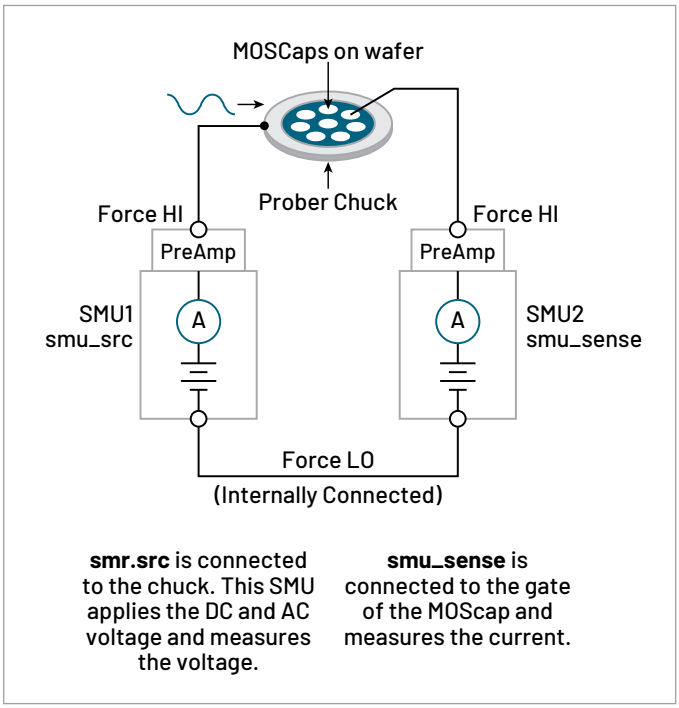


Figure 2. VLF C-V measurement setup for a MOScap on wafer.

An example of a MOSCap circuit connected for VLF C-V measurements is shown in **Figure 2**. Most MOSCaps have only a single pad on the top of the wafer, with the backside of the wafer used as the common contact for all MOSCaps. SMU1 outputs the AC+DC voltage and is connected to the chuck. The SMU that outputs the voltage is known as "smu_src" in the software that is included with the system. The high impedance terminal of the MOSCap is the gate and is connected to SMU2, which is called "smu_sense" in the software.

Using the Clarius Software to Perform VLF C-V Measurements

The system includes a user library called *VLowFreqCV* that contains several user modules that you can use to make low frequency C-V measurements. Clarius includes example tests and projects that are based on these user modules that you can use as templates to develop tests. The example tests and projects are available in the Library.

You can also build custom tests using these user modules. The *VLowFreqCV* User Library contains several modules, listed in **Table 2**, that can be used in a test in a project. To build a custom test, in the Library, select Custom Test and select the option "Choose a test from the pre-programmed library (UTM)". Select Configure. In the right pane, for the User Library, select *VLowFreqCV* User Library and then select the appropriate User Module.

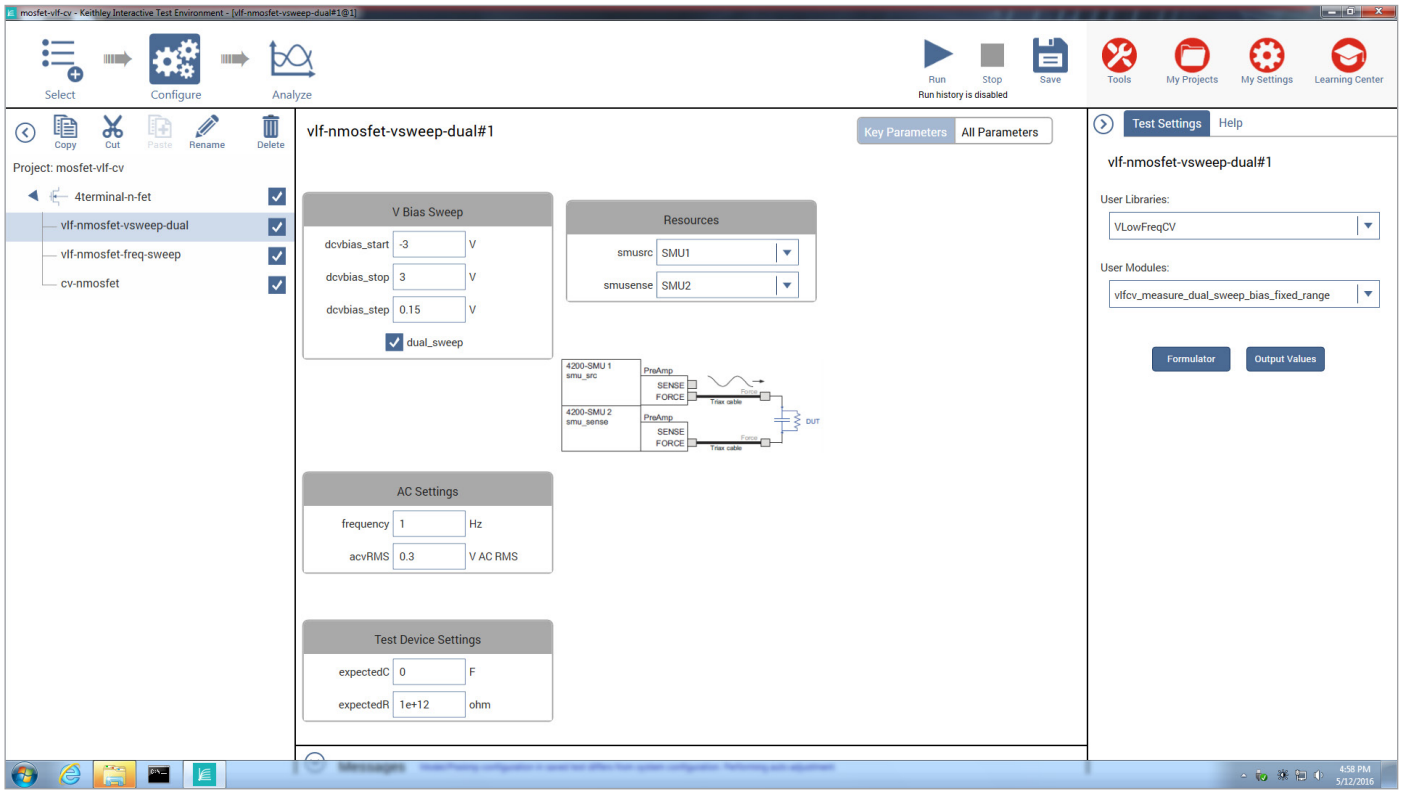


Figure 3. Screen capture of *vlfcv_measure_dual_sweep_bias_fixed_range* user module

Table 2. User Modules in the *VLowFreqCV* User Library.

User Module	Description
vlfcv_measure	Measures C, G, Z, theta, R+jX at a fixed DC bias.
vlfcv_measure_dual_sweep_bias	Measures C, G, Z, theta, R+jX, time while sweeping the DC voltage. Optional dual sweep allows sweeping from dcv_bias_start to dcv_bias_stop, with 1 measure point at dcv_bias_stop, then back down to dcv_bias_start.
vlfcv_measure_dual_sweep_bias_fixed_range	Measures C, G, Z, theta, R+jX, time while sweeping the DC voltage. Measurements are made on a fixed current range which is determined by the expected_C, expected_R and maximum DC voltage. Optional dual sweep allows sweeping from dcv_bias_start to dcv_bias_stop, with 1 measure point at dcv_bias_stop, then back down to dcv_bias_start.
vlfcv_measure_sweep_freq	Measures C, G, Z, theta, R+jX, time at multiple user-specified test frequencies.
vlfcv_measure_sweep_time	Measures C, G, Z, theta, R+jX, time as a function of time.

Once you've added a new module to a project, you need to input a few parameters. Many of the parameters are common to all the modules; however, each module has some unique parameters. **Figure 3** illustrates the Key Parameters view of the *vlfcv_measure_dual_sweep_bias_fixed_range* User Module showing all the user-defined parameters. The adjustable parameters for all the modules are listed in **Tables 3 through 6.**

The values of the expected capacitance (expected_C) and the expected parallel resistance (expected_R) determine which current range will be used to make the measurement. However, choosing specific values is generally not required, as setting expected_C = 0 will allow the test routines to estimate the C and R to use.

The simplest module is *vlfcv_measure*. It is used in the *Capacitor VLF C-V Measurement* (*vlf-cap-one-point*) test in the *Capacitor VLF-CV Project*. This test performs a single measurement. The module does not perform any sweeping,

but it allows for all test parameters to be controlled (**Table 3**). Note that the maximum voltage possible is a combination of both the AC and DC voltages. The maximum negative DC bias voltage = –20 + (acv_RMS * $\sqrt{2}$). The maximum positive DC bias voltage = +20 – (acv_RMS * $\sqrt{2}$). Use expected_C = 0 to have the routine auto-detect the estimated C and R values.

Table 3. Adjustable parameters in *vlfcv_measure* User Module.

Parameter	Range	Description
smu_src	SMUn	SMU instrument to source DC + AC voltage waveform and measure AC volts: SMU1, SMU2, SMU3...
smu_sense	SMUn	SMU t instrument o measure AC current: SMU1, SMU2, SMU3...
frequency	0.01 to 10	Test frequency in hertz, from 0.01 to 10.
expected_C	1e-12 to 1e-8	Estimate of DUT capacitance in Farads, use 0 for auto-detect of DUT C and R.
expected_R	1e6 to 1e14	Estimate of resistance parallel to DUT, in ohms
acv_RMS	30e-3 to 3	AC drive voltage in volts RMS
dcv_bias	±20 less (acv_RMS * $\sqrt{2}$)	The DC voltage applied to the device

Table 4. Adjustable parameters in the *vlfcv_measure_dual_sweep_bias_fixed_range* User Modules.

Parameter	Range	Description
smu_src	SMUn	SMU instrument to source DC + AC voltage waveform and measure AC volts: SMU1, SMU2, SMU3...
smu_sense	SMUn	SMU instrument to measure AC current: SMU1, SMU2, SMU3...
frequency	0.01 to 10	Test frequency in hertz, from 0.01 to 10.
expected_C	1e-12 to 1e-8	Estimate of DUT capacitance in Farads, use 0 for auto-detect of DUT C and R.
expected_R	1e6 to 1e14	Estimate of resistance parallel to DUT, in ohms
acv_RMS	30e-3 to 3	AC drive voltage in volts RMS
dcv_start	±20 less (acv_RMS * $\sqrt{2}$)	Starting DC voltage of the sweep
dcv_stop	±20 less (acv_RMS * $\sqrt{2}$)	Stop DC voltage of the sweep
dcv_step	±20 less (acv_RMS * $\sqrt{2}$)	Step size of the DC voltage. Number of steps limited to 512.
dual_sweep	0 or 1	Enter 0 for single sweep; enter 1 for dual sweep

Table 5. Adjustable parameters in the *vlfcv_measure_dual_sweep_freq* user module.

Parameter	Range	Description
smu_src	SMUn	SMU instrument to source DC + AC voltage waveform and measure AC volts: SMU1, SMU2, SMU3...
smu_sense	SMUn	SMU instrument to measure AC current: SMU1, SMU2, SMU3...
frequency	0.01 to 10	Array of Test frequencies in Hertz. Maximum number of entries limited to 512, from 0.01 to 10.
expected_C	1e-12 to 1e-8	Estimate of DUT capacitance in Farads, use 0 for auto-detect of DUT C and R.
expected_R	1e6 to 1e14	Estimate of resistance parallel to DUT, in ohms
acv_RMS	30e-3 to 3	AC drive voltage in volts RMS
dcv_bias	±20 less (acv_RMS * $\sqrt{2}$)	The DC Voltage applied to the device

Table 6. Adjustable parameters in the *vlfcv_measure_sweep_time* user module.

Parameter	Range	Description
smu_src	SMUn	SMU instrument to source DC + AC voltage waveform and measure AC volts: SMU1, SMU2, SMU3...
smu_sense	SMUn	SMU instrument to measure AC current: : SMU1, SMU2, SMU3...
frequency	0.01 to 10	Test frequency in Hertz, from 0.01 to 10.
expected_C	1e-12 to 1e-8	Estimate of DUT capacitance in Farads, use 0 for auto-detect of DUT C and R.
expected_R	1e6 to 1e14	Estimate of resistance parallel to DUT, in ohms
acv_RMS	30e-3 to 3	AC drive voltage in volts RMS
dcv_bias	±20 less (acv_RMS * $\sqrt{2}$)	The DC Voltage applied to the device
num_points	1 to 512	Number of points to take as a function of time

Once any test is executed, several test parameters will be returned to the Sheet in the Analyze view and can be saved as an .xls file. These test parameters can also be plotted on the Graph. **Table 7** lists the returned test parameters and their descriptions. From these returned test parameters, more device extractions can be performed using the mathematical functions in the Formulator. Note that the tests return all typical C-V measurement parameters. For example, both Cp-Gp and Cs-Rs are always returned, even if the test device response only matches the parallel (Cp-Gp).

Table 7. Measurements returned for the modules in the *VLowFreqCV* Library.

Returned Test Parameters	Description
Status	Error code from test module execution. Definitions of the returned errors are listed at the bottom of the Definition tab in the UTM Description.
times	Calculated time difference between readings.
dcv_bias	Programmed DC voltage applied to the device.
meas_Cp	Measured capacitance in parallel (Cp-Gp).
meas_Gp	Measured conductance in parallel (Cp-Gp)
meas_freq	Measured test frequency.
meas_Z	Measured impedance (Z-theta).
meas_Theta	Measured phase angle in degrees (Z-theta).
meas_R	Real component of the impedance (R + jX).
meas_X	Imaginary component of the impedance (R + jX).
meas_Cs	Measured AC capacitance in series (Cs-Rs).
meas_Rs	Measured resistance in series (Cs-Rs).
meas_D	Calculated dissipation factor, D.
meas_irange	The SMU instrument current range that the measurement was taken.

Using the Example Tests and Projects in the Library

The Clarius software comes with example tests of very low frequency C-V measurements on various devices. Choose Select to search for the examples in either the Test or Project Libraries. Enter VLF in the search box from either the Test or Project tab. The Tests or Projects will automatically be displayed in the Library. Select the desired Test or Project and add it to the Project tree on the left. Even though the test and projects were created using specific devices, these examples can be used on other devices. Descriptions of the very low frequency C-V projects that can be found in the Project Library are described in the following paragraphs.

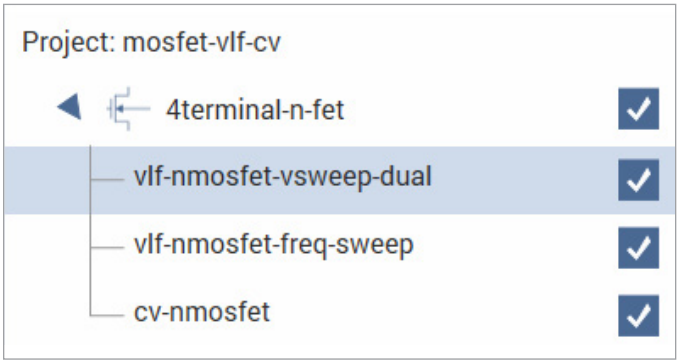


Figure 4. Project tree of *MOSFET VLF-CV* project

MOSFET VLF-CV Project

In the *MOSFET VLF-CV Project*, there are three tests for the n-fet devices, as shown in **Figure 4**. **Figure 6** shows the results of generating a very low frequency dual C-V sweep on an n-MOSFET measured between the Gate terminal and the Drain/Source/Bulk terminals tied together (**Figure 5**). This C-V sweep was generated using the *MOSFET VLF-CV Sweep* (*vlf-nmosfet-vsweep-dual*) test. Tests for measuring capacitance as a function of frequency (*vlf-nmostfet-freq-sweep*), as well as a high frequency C-V test (*cvu-nmostfet*, taken with the CVU) are also included in the project.

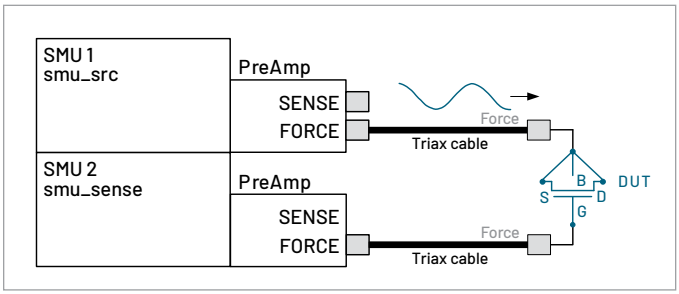


Figure 5. Connection for MOSFET with the gate connected to SMU2 and, with the drain-source-bulk tied together and connected to SMU1 (*smu_sense*).

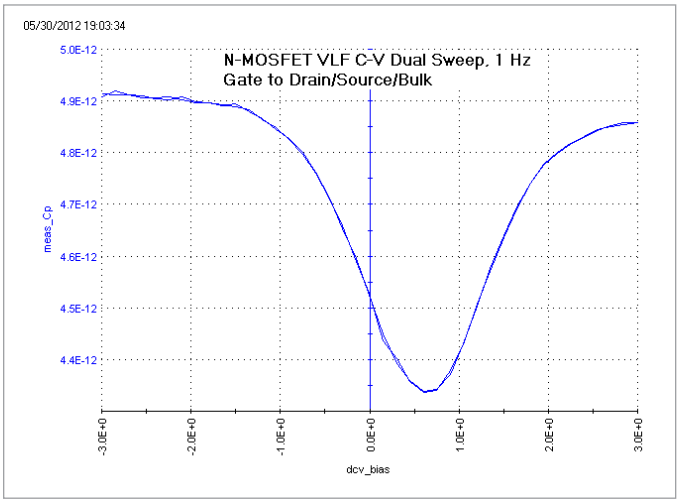


Figure 6. VLF C-V Sweep of an n-MOSFET measured between the gate to drain/source/bulk. This graph is from the *vlf_nmosfet_vsweep_dual* test (user module *vlfcv_measure_dual_sweep_bias_fixed_range*).

Capacitor VLF-CV Project

Using the VLF C-V method, capacitors can be measured in the range of 1 pF to 10 nF, and connections are made as shown in **Figure 7**. The project has four tests for measuring capacitors (**Figure 8**). The *Capacitor VLF-CV C-t Sweep* (*vlf-cap-time*) Test measures the capacitance of a 1pF capacitor as a function of time (**Figure 9**). The results of performing a C-V sweep on a 1 pF capacitor are shown in **Figure 10**. This small capacitance was measured at a test frequency of 1 Hz with capacitance measurement noise levels at less than ±5E-15F. The Formulator can be used to determine the noise and average capacitance readings easily.

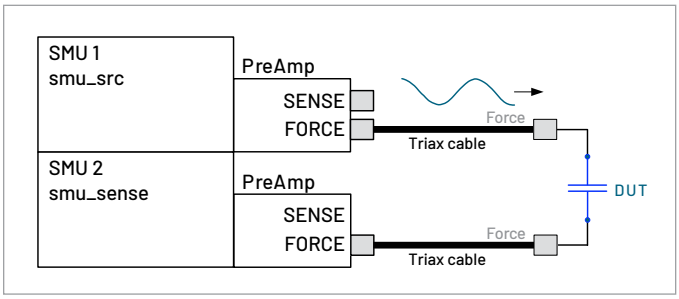


Figure 7. VLF C-V connections for the capacitor. If the test device is on wafer, see the MOSCap diagram (Figure 2) for connections.

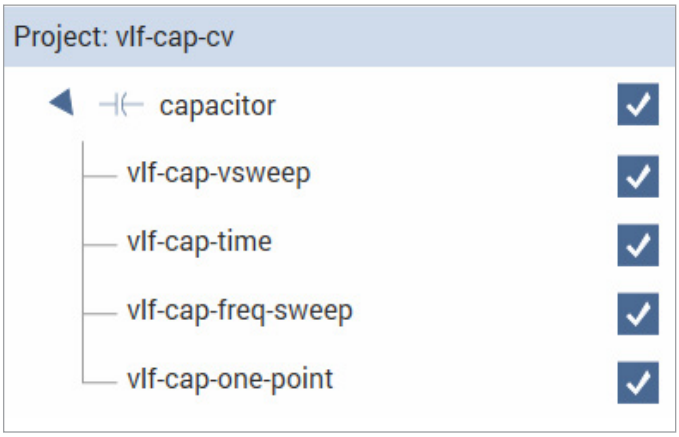


Figure 8. Capacitor tests in the *Capacitor VLF-CV Project*.

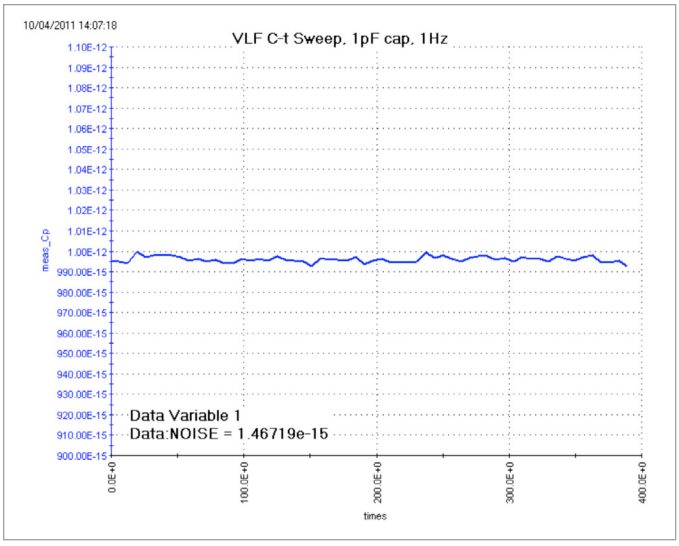


Figure 9. Results of C-t measurements of nominal 1 pF reference capacitor, using VLF capacitance technique at a test frequency of 1 Hz. This graph is from the *vlf-cap-time* test (user module *vlfcv_measure_sweep_time*).

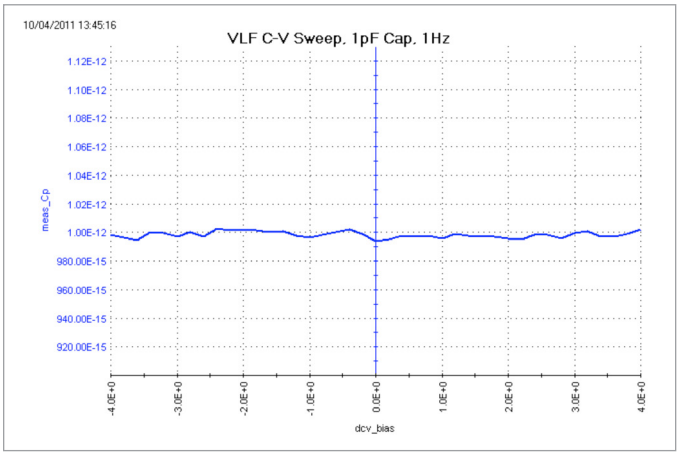


Figure 10. VLF C-V results, at 1 Hz, of a voltage sweep on a 1 pF reference capacitor. This graph is from the *vlf-cap-vsweep* test (*vlfcv_measure_dual_sweep_bias_fixed_range* user module).

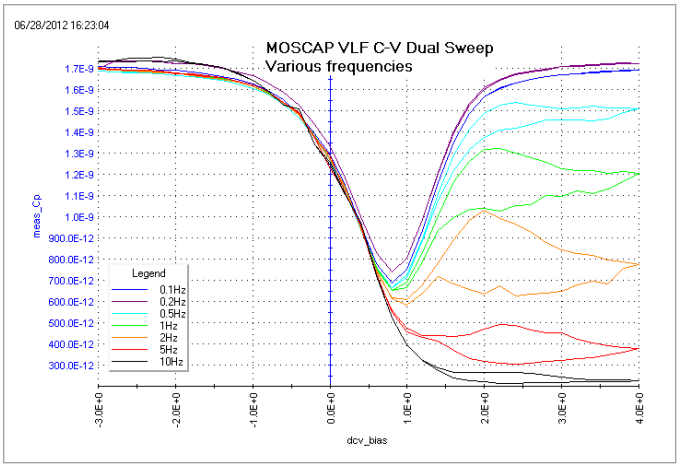


Figure 11. A VLF C-V sweep of a MOScap at various frequences from 100mHz to 10Hz created using the *MOS Capacitor VLF-CV Project*. This graph is from the *vlf-moscap-vsweep-dual* test (*vlfcv_measure_sweep_bias_fixed_range* user module).

MOS Capacitor VLF-CV Project

The MOScap Project has three tests; all are DC bias sweeps with two using SMUs for the VLF C-V test DC bias voltage sweep (*vlf-moscap-vsweep-dual* and *vlf-moscap-vsweep*) and the other using the 4210-CVU or 4215-CVU for higher frequency testing (*cvu-moscap-vsweep*). An example of a MOScap VLF-CV dual sweep generated with various test frequencies ranging from 0.1 Hz to 10 Hz is shown in **Figure 11**. This test was performed on a chuck at room temperature. This sweep is the result of executing the *vlf-moscap-vsweep-dual* test in the project. From the low frequency C-V data, characteristics about the MOScap can be determined. The built-in math functions are helpful in performing the analysis of these devices from the C-V data. The connection diagram for the MOSCap is shown in **Figure 2.** The dual sweep functionality aids in determining any hysteresis behavior in the inversion region of the MOScap device, where frequency dependence is also observed. Note that the SMU instrument measuring the low current is not connected to the chuck. Connecting the sensitive (i.e., low-current measurement) instrument to the chuck will result in noisier measurements.

In addition to the test that generates VLF C-V measurements on the MOScap, the project includes a test to measure high frequency C-V on the MOScap. The high frequency C-V measurements were generated using the CVU, which has a test frequency range of 1 kHz to 10 MHz, with the example data taken at 100 kHz.

To compare the results of both low and high C-V measurements on one graph, the data can be copied from one test module into another. Just select and copy the C-V measurements from the Sheet of one test module and then paste the data into the columns of the CALC Sheet of the other test module. The data in the CALC Sheet can be selected on the graph to plot. To do this, make sure to check the "Enable Multiple Xs" box in the Graph Definition window. An example showing both the low and high frequency C-V measurements on one graph is shown in **Figure 12.**

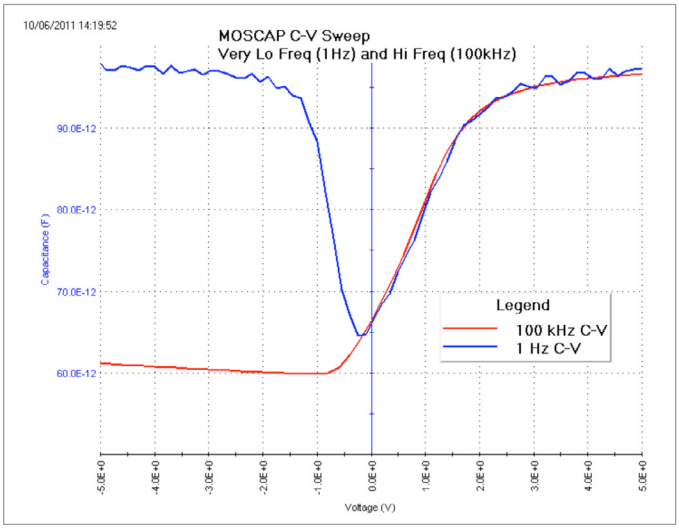


Figure 12. This graph is from the *moscap-vsweep-hif-lof* test, showing the high frequency data from the CVU card along with the VLF C-V data from the *vlf-moscap-vsweep* test.

R-C Circuit VLF-CV Project

Some devices can be modeled as a parallel RC combination (connection diagram in **Figure 13**). The parallel resistance is usually the leakage resistance of the device. In the *R-C Circuit VLF-CV Project*, there are two tests for the RC device: one is the test for a VLF C-V DC bias sweep (*vlf-1nf-1gohm*) and the other tests sweeps votage and measures current using an SMU (*smu-vsweep*). **Figure 14** shows the results of performing a low frequency sweep on a 1.5 nF and 1 GΩ parallel combination. From the bias voltage and the resistance (1/Gp) of the device, the current can be calculated in the Formulator and displayed on the graph. Excessive leakage current can cause erroneous results if the current exceeds the maximum current range for the particular RC combination. To determine the DC leakage current of an unknown DUT, use the *smu-vsweep* test, as described in the section titled "Testing a Device with VLF C-V." More information about making optimal measurements is described in the next section of this note.

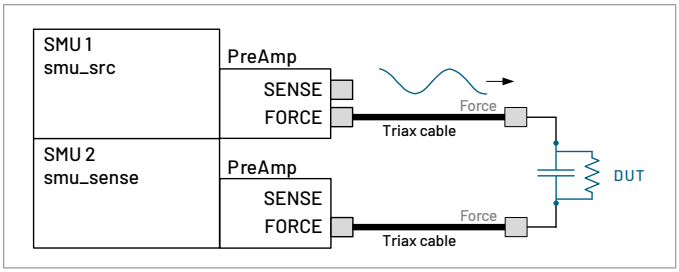


Figure 13. Connection diagram for parallel RC test device.

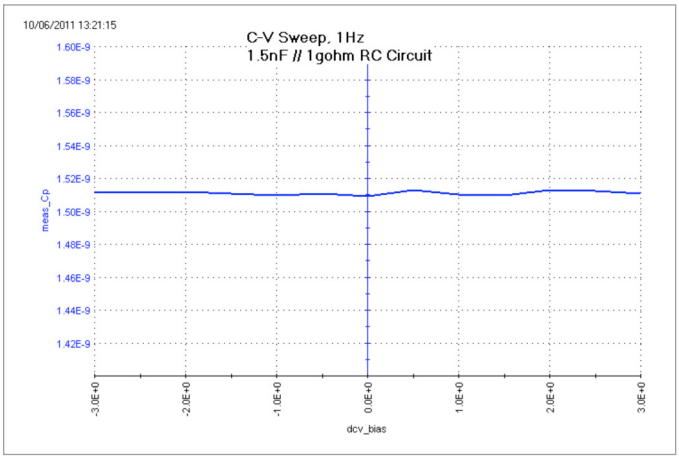


Figure 14. Results of measuring parallel RC combination of 1.5nF capacitor and 1GΩ resistor. This graph is from the *vlf-1nF-1gohm* test (*vlfcv_measure_dual_sweep_bias_fixed_range* user module).

Testing a Device with VLF C-V

Dissipation Factor

The parallel resistance of the device under test is a key aspect that determines the quality of the capacitance measurement because it causes additional DC current to flow, which reduces measurement accuracy. This parallel resistance at a given frequency is otherwise expressed as D, the dissipation factor. Here is the equation for the simple parallel model.

$D = \text{Reactance/Resistance} = 1/\omega RC = 1/2\pi fRC$

where:

f is the test frequency, in Hz

R is the parallel resistance of the test device, in Ω

C is the capacitance of the test device, in farads

Guidance for measurement performance across a range of D values is shown in **Table 8**. As the table shows, higher D values reduce the accuracy of the reported C measurement.

Table 8. VLF C-V typical accuracy vs. D and current measure range for the sense SMU instrument.

	0.01 D	0.1 D	1 D	10 D
1 µA	0.6 %	1.6 %	Not Recommended	Not Recommended
100 nA	1.4 %	10 %	Not Recommended	Not Recommended
10 nA	0.7 %	4 %	6 %	Not Recommended
1 nA	0.4 %	2 %	2.6 %	3 %
100 pA	0.8 %	0.6 %	0.6 %	2 %

"Not Recommended" means that the typical error is >10%. For details on specific capacitance and frequency values, see the VLF C-V Typical Specifications in Appendix A.

If the device is purely capacitive (very low to almost no leakage current, a D <0.1), then just connect the DUT as shown in **Figure 7** (or **Figure 2** if the DUT is on a wafer). After connection, run the desired test(s). However, if the device type is new, or its electrical characteristics are unknown, then use the following procedure. This procedure provides a guideline for determining reasonable parameter values for unknown test devices using the parallel (**Figure 13**). It also provides guidance for evaluating results.

Setup

1. Connect the DUT as shown in **Figure 2**. The connection must be direct with the supplied triax cables. No switching or 4225-RPMs may be in the cable path from the SMU instrument Preamp to the DUT. The VLF C-V method utilizes low current measurements, so ensure that appropriate shielding and guarding are used. Use triax cable and eliminate, if possible, or minimize any unshielded or unguarded cable runs. For on-wafer measurements, use triax probe manipulators and guarded probe arms.
2. Open one of the example very low frequencyy tests or project examples in the Library.

Initial Screening of DUT characteristics

3. Choose the SMU instrument IV sweep, *smu-vsweep* test, *R-C Circuit VLF-CV Project*. Choose voltage start and stop values for the sweep that match the desired

minimum and maximum DC bias voltages to be used for VLF C-V tests. This test will help determine if the DUT leakage is too high for repeatable, accurate results.

4. Run the *smu-vsweep* test. Review the results on the graph or in the Sheet. For best results, the maximum current should be <±1 µA. If the current >±1 µA, reduce the bias voltages until the current <±1 µA. Note these voltages for later testing. These voltages may need to be adjusted again as described later in this procedure.
5. Next, choose the *vlf-cap-freq-sweep* test, *Capacitor VLF-CV Project*. Enter the desired test frequencies, using just five to ten points to span the desired frequency range. If only one test frequency is desired, use the single point test *vlf-cap-one-point* instead. Use the default expected_C = 0 and expected_R = 1E+12. Use acv_RMS = 0.3V and dcv_bias = 0.0V. This test will help determine the dissipation factor D of the DUT.
6. Run the *vlf-cap-freq-sweep* test. Review the results in the Sheet. Review the value(s) in the meas_D column. If |meas_D| <1, then the results are reasonable for the test frequencies and DC bias values that had <±1 µA with the *smu_vsweep* test. If |meas_D| <10 then results should be reasonable for dcv_bias = 0V. If |meas_D| >10, then this present implementation of VLF C-V may provide unacceptable results or results with fairly large errors (**see Table 8**). Note that reasonable values with a low D value at dcv_bias = 0 may provide larger errors as the DC bias is increased.

VLF C-V Characterization of DUT

7. Configure the desired test, such as the bias sweep *vlf-cap-vsweep* (**Table 4**) or frequency sweep *vlf-cap-freq-sweep* (**Table 5**) in the *Capacitor VLF-CV Project*. Use the voltage values determined in the previous step. As stated earlier, using expected_C = 0 will perform an auto-detect of both the C and R values. For the other parameters, follow the description in the table corresponding to the test (**Tables 3** through **6**).
8. Run the test. Because of the Run History feature, repeating the test keeps the old data, allowing for comparison across multiple tests. The test parameters used for each run are in the Settings tab of each Run History. For unknown or new devices, review the measurements to ensure that the results are reasonable by evaluating the data in the Sheet as well as the plotted values.
   a. Review the plotted data, noting the overall shape and Y-axis values.
   a. Check the status returned from the test. Status = 0 means that the routine did not detect any errors, but the validity of the data must still be assessed; go to the next step. If there is a non-zero status value, refer to the **Table 9** Error Codes to see the explanation and troubleshooting suggestions.
   a. In the Sheet, check the current measurement range used. The column meas_irange, located on the right side of the Sheet, shows the current measure range used for each point. If this range is 1E-6 (1 µA) or lower, skip to the next step. If any of the measure range values is 10E-6 (10 µA) or larger, the results for these rows are suspect. Change the DC bias voltage to reduce the current measure range used for the test. For example, when running a voltage bias sweep, reduce the start and stop voltage used, for example from ±5 V to ±2 V, and re-run the test. Verify that the new test uses a meas_irange 1E-6 (1 µA) or lower, then compare the results to the previous run taken with the 10 µA range. Generally, the results with the 1 µA range are more accurate.
   a. If the Y-axis scale shows the maximum of 7E22 or 70E21, then an overflow has occurred on one or more measurements in the test. Review the data in the Sheet, in the meas_Cp column, for entries of 70E21 or 7E22. There are a few causes of the overflow:
      i. If the overflow values are only at the start and end of the test, consider reducing the range of sweep values to omit the sweep points that cause the overflow values. Another option is to specify appropriate values for expected_C and expected R. Before choosing values for expected_C and expected_R, let's briefly explain how these values affect the test. If the overflow values are most or all of the rows in the meas_Cp column, it is possible that an incorrect measure range was used for the test. This means that the current measure range used for the test was too small for the test parameters and DUT. The measure range used for the test is contained in the meas_irange in the Sheet. The current measure range for the sense SMU instrument is based on the expected_C and expected_R values.

i. To change the current measure range for a test, supply an expected_C value that is larger than the meas_Cp value. Review the values in the meas_Cp column and choose a representative, non-overflow value and use it to calculate the expected_C = 2 * chosen meas_Cp value. To choose a value for expected_R, review the meas_Gp column for a representative value. Set expected_R = 1/(2 * chosen meas_Gp).

e. If one or more of the meas_Cp values is negative:

i. Ensure that the DUT connections are good.

i. The D may be too high, or the DC current leakage is too high compared to the capacitance.

1. Review the Sheet for meas_D and meas_irange values. If D > ~10 and or meas_irange is ≥10 nA, the results may have a larger error.

1. Consult **Table 8**. Compare the current measure range (in the meas_irange) column to the corresponding row in **Table 8**. Note that the higher D values are more difficult to test.

1. Try one or more of the following adjustments: a) reduce the DC bias voltage; b) increase the acv_RMS = 0.3 V; c) increase the test frequency.

1. If the meas_Cp values seem noisy or inconsistent, append several tests with identical parameter values and review the data. If the results are different across each run, this indicates that the system is operating at or near the noise floor, which means that the capacitance value of the test device is small, or the test device has a higher D value (**Table 8**).

1. If none of these adjustments provides reasonable results, try a higher frequency C-V test using the CVU, if available.

9. Add tests, such as the capacitance vs. time (test *vlf-cap-time*) or more DC bias sweeps at additional test frequencies. Recall that data may be saved in .xls or .csv file formats by using the Save Data button in the Analyze pane.

Table 9. VLF C-V error codes and descriptions.

Error Code	Description	Explanation and Troubleshooting Recommendation
0	Test executed with no errors	No software or operational errors were detected.
-16001	smu_src is out of range	Specified SMU instrument is not available in the chassis. For example, if SMU5 is entered, but there are only four SMU instruments in the 4200 chassis, then this error will occur. Modify SMU instrument string to an available SMU instrument number: SMU1, SMU2, SMU3 ...
-16002	smu_sense is out of range	Specified SMU instrument is not available in the chassis. For example, if SMU5 is entered, but there are only four SMU instruments in the 4200 chassis, then this error will occur. Modify SMU instrument string to an available SMU number: SMU1, SMU2, SMU3 ...
-16003	Frequency is out of range.	Ensure that the test frequency is within the range of 10mHz to 10Hz, inclusive
-16004	acv_RMS is out of range	Make sure that the RMS voltage is within the range of 0.01V to 3.0V, inclusive
-16005	dcv_bias is out of range	Modify the DC or AC voltage bias to ensure that the ±20V maximum is not exceeded. Maximum negative voltage = –20 + (AC voltage *) Maximum positive bias voltage = 20 – (AC voltage * √_2)
-16006	hold_time is out of range	This error is unused for the *VLowFreqCV* routines.
-16007	delay_time is out of range	This error is unused for the *VLowFreqCV* routines.
-16008	Too few points per period	This error indicates that the test was aborted by the operator.
-16009	Output array sizes are not equal, or are larger than 4096.	Make sure all output array sizes are the same value and are not greater than 4096.
-16010	Over range indication detected.	Current measurement over-range occurred and returned values are set to 7E22 (70E21). Troubleshooting: Review the value in the meas_CP column of the Sheet, looking for the overflow values (7E22 or 70E21). Follow the process given in **Step 8d**.
-16011	Results array size is less than the number of points in the sweep.	Increase the size of all output arrays to be equal to the number of points in the sweep.
-16012	Could not collect enough data to perform measurement.	Cannot estimate expected_C or expected_R. This error occurs only when expected_C = 0. Input a estimated non-zero value for expected_C. Review the meas_Cp values in the Sheet for non-overflow values. Set estimated_C = 2 * non-overflow meas_Cp
-16013	Unable to allocate memory.	This error is unused for the *VLowFreqCV* routines.
-16014	Current range is out of range.	This error is unused for the *VLowFreqCV* routines.
-16015	Irange_sense and expected_C cannot be 0 at the same time	This error is unused for the *VLowFreqCV* routines.
-16016	expected_C is out of range	expected_C must be 0 (auto-detect C) or between 1E-15 and 1E-3, inclusive.
-16017	This test requires preamp is connected to smu_sense	Make sure preamp is connected to each SMU used in the test. If reconnecting preamps, run run KCON and choose "Update PreAmp and RPM Configuration" in the Tools menu.
-16018	Invalid start, stop, step DC bias sweep values.	Correct the values for the voltage bias sweep. dcv_bias_step cannot be 0, unless dcv_bias_start = dcv_bias_stop. If dcv_bias_start = dcv_bias_stop, then dcv_bias_step must = 0.
-16019	Output array sizes are less than number of points in sweep.	Increase the size of all output arrays to be equal to the number of points in the sweep.
-16020	Invalid combination of start, stop, step dc bias sweep values.	Correct the values for the voltage bias sweep. dcv_bias_step cannot be 0, unless dcv_bias_start = dcv_bias_stop. If dcv_bias_start = dcv_bias_stop, then dcv_bias_step must = 0.

Guidelines for Making Optimal Measurements and Troubleshooting Techniques

When making high impedance, very low frequency C-V measurements using the SMU instruments, various techniques must be used to optimize measurement accuracy. These techniques include implementing low current measurement practices and choosing the appropriate settings in the software.

Implementing Low Current Measurement Techniques

Because using the very low frequency impedance measurement method involves measuring picoamp to femtoamp current levels, low current measurement techniques must be implemented. Use the triax cables that come with the 4200A-SCS, which are shielded and will allow making a guarded measurement, if necessary. To reduce the noise due to electrostatic interference, make sure the device is shielded by placing it in a metal enclosure with the shield connected to the Force LO terminal of the 4200A-SCS. Detailed information on low current measurement techniques can be found in Keithley's Low Level Measurements Handbook. Also, ensure that the triax cable is directly connected to the DUT or probe pins; do not use any switching matrix or 4225-RPM in the SMU instrument signal path.

Choosing the Correct "expected_C" and "expected_R" Values

In most cases, expected_C should be 0 and the expected_R = 1E12 (both are the default values). When expected_C = 0, the VLF C-V routine will determine estimated values for both C and R of the device under test. The estimated R and C values determine the SMU instrument measurement range. If these values are chosen incorrectly, measurement errors or measurement range overflow may result (see **Table 9**, error code -16010 for more information). However, in some cases, entering a non-zero estimated capacitance for expected_C may provide better results for higher D devices or larger DC bias tests. To calculate a value of expected_C, multiply a non-overflow value from the meas_Cp column by two and enter this value into the test definition expected_C.

To determine if a device is compatible with the present VLF C-V approach, measure the DC resistance of the DUT, performing an I-V test using the *smu-vsweep* test, *R-C Circuit VLF-CV Project*. Use the same test voltages in the I-V sweep that will be used in the impedance measurements. Additionally, performing a single measurement (test *vlf-cap-one-point*) or frequency sweep (test *vlf-cap-freq-sweep*) at a DC bias of 0 V will determine the D of the device. Refer to "Testing a Device with VLF C-V" and **Table 8** for additional information.

Conclusion

The 4200A-SCS contains a tool for performing very low frequency C-V measurements using the SMU instruments and preamps. This method enables the user to perform low capacitance measurements at a precise test frequency in the range of 10 mHz to 10 Hz. The Clarius software included with the system enables the user to execute these low impedance measurements easily and extract important parameters about the DUT. When combined with the 4210-CVU or 4215-CVU Capacitance Voltage Unit, the 4200A-SCS offers the user a single system that can perform both high and low frequency measurements.

Appendix A

Very Low Frequency C-V Typical Specifications

MEASUREMENT FUNCTIONS

Measurement Parameters: Cp+Gp, Cp+D, Cs, Rs+Cs, R+jX, Z, theta, frequency, voltage, time.

Connector Type: Two triax (female) connectors.

TEST SIGNAL

Frequency Range: 10 mHz to 10 Hz.

Minimum Resolution: 10 mHz

Signal Output Level Range: 10 mV rms to 3 V rms.

DC BIAS FUNCTION

DC Voltage Bias:

Range: ±20 V[1].

Resolution: 0.5 mV.

Accuracy: ±(0.02% + 1.5 mV).

Maximum DC Current: 1 µA.

SWEEP CHARACTERISTICS

Available Test Types: Linear bias voltage sweep (up or down), frequency list sweep, sample (time), single point

Maximum Number of Measurement Points: 512.

INCLUDED LIBRARIES

- C-V, C-t and C-f modules
- Includes test and projects for:
  - Capacitor
  - MOSCAP
  - nMOS FET
  - R-C circuit

REQUIRED HARDWARE and SOFTWARE

- 4200A-SCS
- Two SMU instruments, 4200-SMU, 4201-SMU, 4210-SMU or 4211-SMU, with Pre-amplifiers (4200-PA)

TYPICAL MEASUREMENT ACCURACY[2]

Frequency	Measured Capacitance	C Accuracy @ 300 mV rms[1]	C Accuracy @ 30 mV rms[1]
10 Hz	1 pF	10%	13%
	10 pF	10%	10%
	100 pF	5%	5%
	1 nF	5%	9%
	10 nF	5%	5%
1 Hz	1 pF	2%	2%
	10 pF	1%	2%
	100 pF	2%	1%
	1 nF	2%	1%
	10 nF	2%	2%
100 mHz	1 pF	2%	3%
	10 pF	2%	2%
	100 pF	2%	2%
	1 nF	1%	2%
	10 nF	2%	1%
10 mHz	1 pF	5%	10%
	10 pF	1%	2%
	100 pF	1%	1%
	1 nF	1%	1%
	10 nF	2%	2%

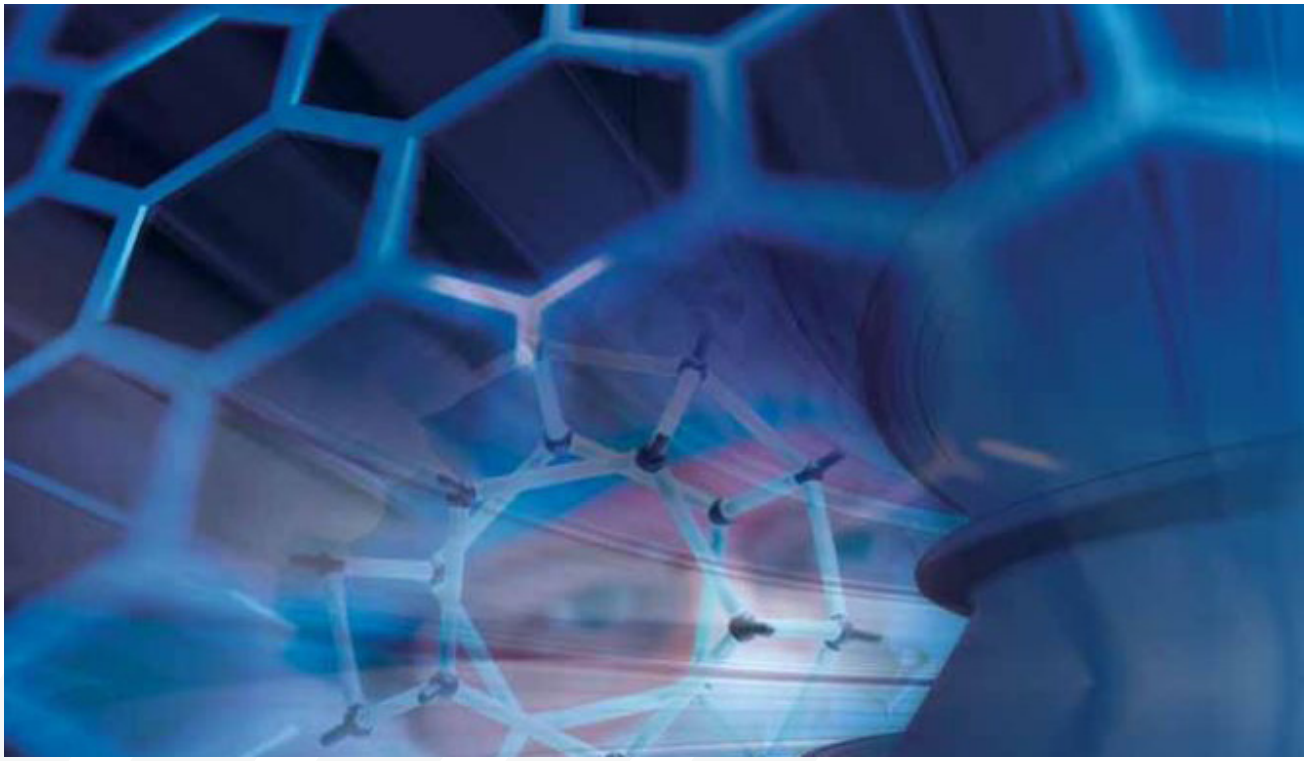
NOTES

1. ±20 V maximum includes the DC Bias and the AC Test Signal peak voltage. Maximum negative bias voltage = –20 + (AC voltage * $\sqrt{2}$). Maximum positive bias voltage = 20 – (AC voltage * $\sqrt{2}$).
2. Test device must have dissipation factor D_X <0.1. All data shown for DC Bias voltage = 0 V.

All specifications apply at 23°C ±5°C, within one year of calibration, RH between 5% and 60%, after 30 minutes of warmup.

Tektronix®

Electrical Characterization of Carbon Nanotube Transistors (CNT FETs) with the 4200A-SCS Parameter Analyzer



Introduction

Carbon nanotubes (CNTs) have been the subject of a lot of scientific research in recent years, due not only to their small size but to their remarkable electronic and mechanical properties and many potential applications. The problems associated with attempting to scale down traditional semiconductor devices have led researchers to look into CNT-based devices, such as carbon nanotube field effect transistors (CNT FETs), as alternatives. Because they are not subject to the same scaling problems as traditional semiconductor devices, CNT FETs are being studied for a wide variety of applications, including logic devices, memory devices, sensors, etc. The research on these devices typically involves determining various electrical parameters, which may include current-voltage (I-V), pulsed I-V, and capacitance (C) measurements. Characterizing the electrical properties of delicate nanoelectronic devices requires instruments and measurement techniques optimized for low power levels and high measurement sensitivity.

The 4200A-SCS Parameter Analyzer offers a variety of advantages for electrical characterization of CNT FETs. This configurable test system can simplify these sensitive electrical measurements because it combines multiple measurement instruments into one integrated system that includes hardware, interactive software, graphics, and analysis capabilities. The system comes with pre-configured tests for performing electrical measurements that have been optimized to ensure accurate results on CNT FETs. This application note explains how to optimize DC, pulsed I-V, and C-V measurements on a CNT FET using the 4200A-SCS Parameter Analyzer. It includes detailed information on proper cabling and connections, guarding, shielding, noise reduction techniques, and other important measurement considerations when testing carbon nanotube transistors.

The Carbon Nanotube Transistor

A single semiconducting CNT can be used as the conducting channel between the source and drain of a FET. **Figure 1** illustrates a back-gated Schottky barrier CNT FET. Two metal contacts are located across both ends of the CNT to form the Source and Drain terminals of the FET. The CNT is placed atop an oxide that sits above a doped silicon substrate, which forms the Gate terminal. Connections are made to the three DUT terminals to perform the electrical measurements.

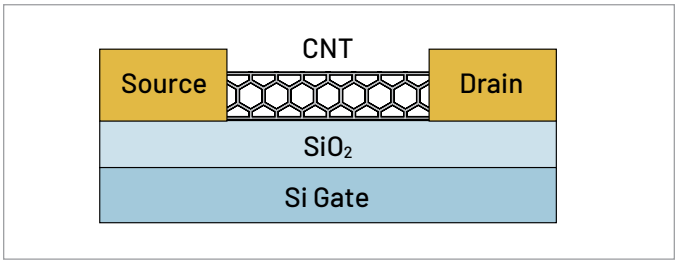


Figure 1. Back-gated carbon nanotube transistor

Making Electrical Measurements with the 4200A-SCS

The 4200A-SCS is supplied with a test project for making some of the most commonly used electrical measurements for CNT FETs. This project, the Carbon Nanotube Transistor Characterization Project (*cntfet*), includes tests for I-V, pulsed I-V, and C-V measurements. The I-V tests are performed using two Source Measure Units (SMUs), 4200-SMU, 4201-SMU, 4210-SMU, or 4211-SMU, both with the 4200-PA Preamp option. The pulsed and transient I-V measurements are made using the 4225-PMU Ultra-Fast I-V Module (PMU) with two 4225-RPM Remote/Preamplifier Switch options. Finally, the C-V measurements are performed using the either the 4210-CVU or 4215-CVU C-V Measurement Module (CVU).

The *cntfet* project is included with all 4200A-SCS systems. **Figure 2** shows the *cntfet* project running in the Clarius application.

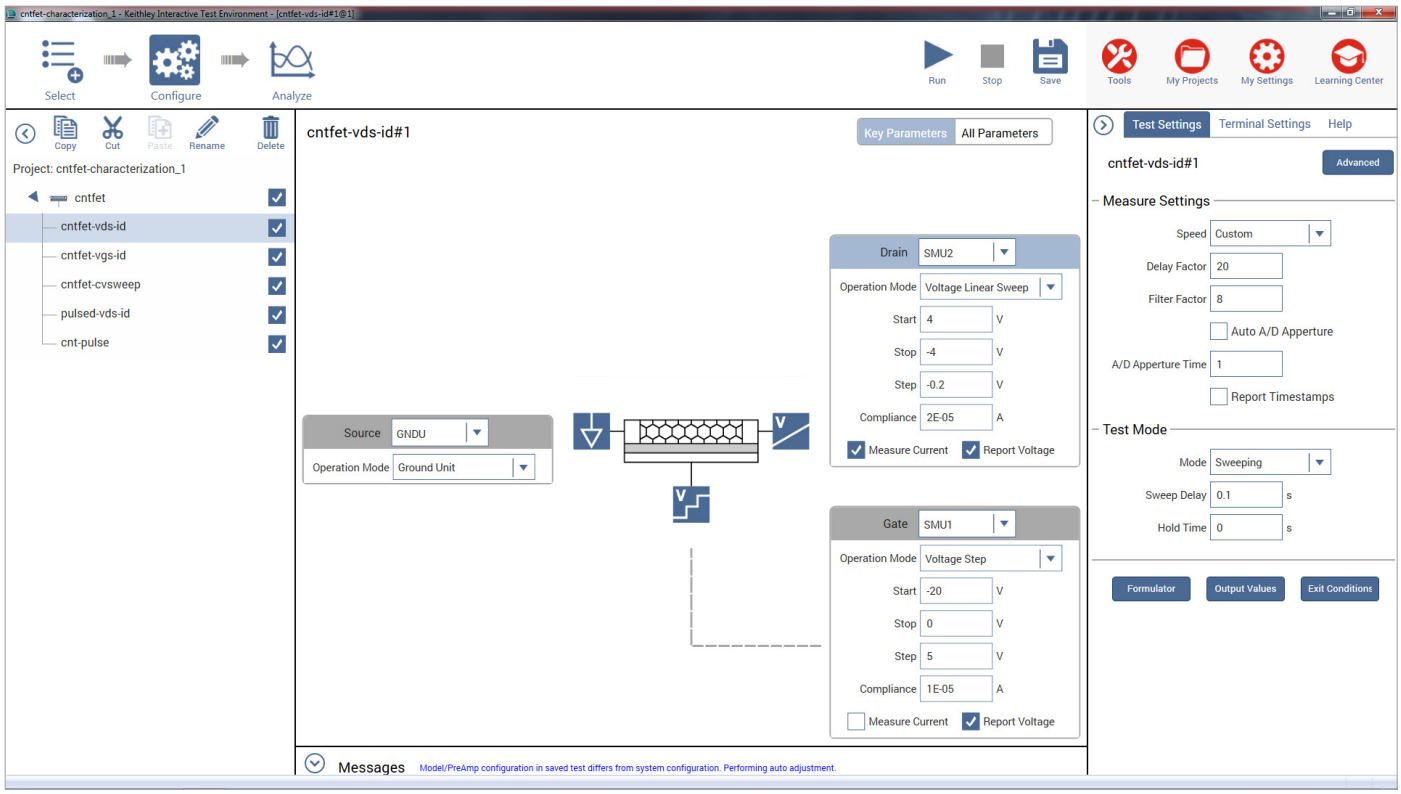


Figure 2. The *cntfet* project for the 4200A-SCS

Current-Voltage Measurements

The I-V characteristics of a CNT transistor can be used to extract many of the device's parameters, study the effects of fabrication technique and process variations, determine the quality of the contacts, etc. **Figure 3** illustrates a DC I-V test configuration that incorporates two SMUs. These SMUs are capable of sourcing and measuring both current and voltage; they have picoamp sensitivity and can be current-limited to prevent damage to the device. In this diagram, SMU1 is connected to the Gate of the CNT FET and SMU2 is connected to the Drain. The Source terminal is connected to the Ground Unit (GNDU) or to a third SMU if it is necessary to source and measure from all three terminals of the FET.

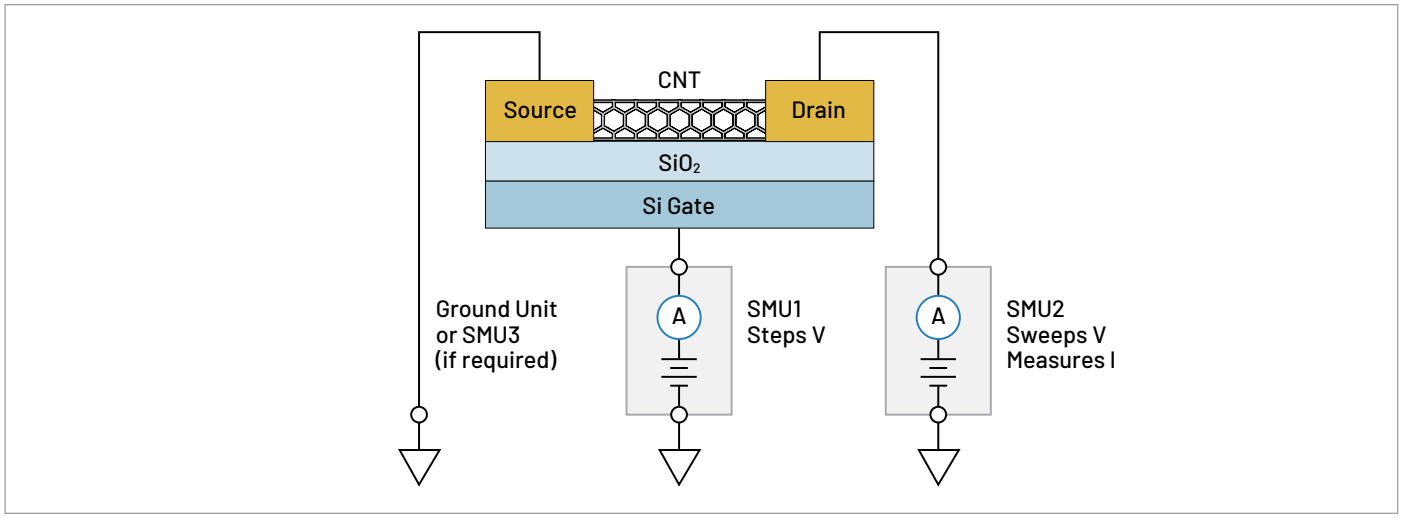


Figure 3. Circuit diagram for measuring the DC I-V characteristics of a CNT FET

In this example, the 4200A-SCS's Clarius software is set up to measure a DC drain family of curves (V_{ds-Id}). As SMU1 steps the gate voltage (V_g), SMU2 sweeps the drain voltage (V_d) and measures the resulting drain current (I_d). **Figure 4** shows the resulting FET characteristics generated using the CNT FET project.

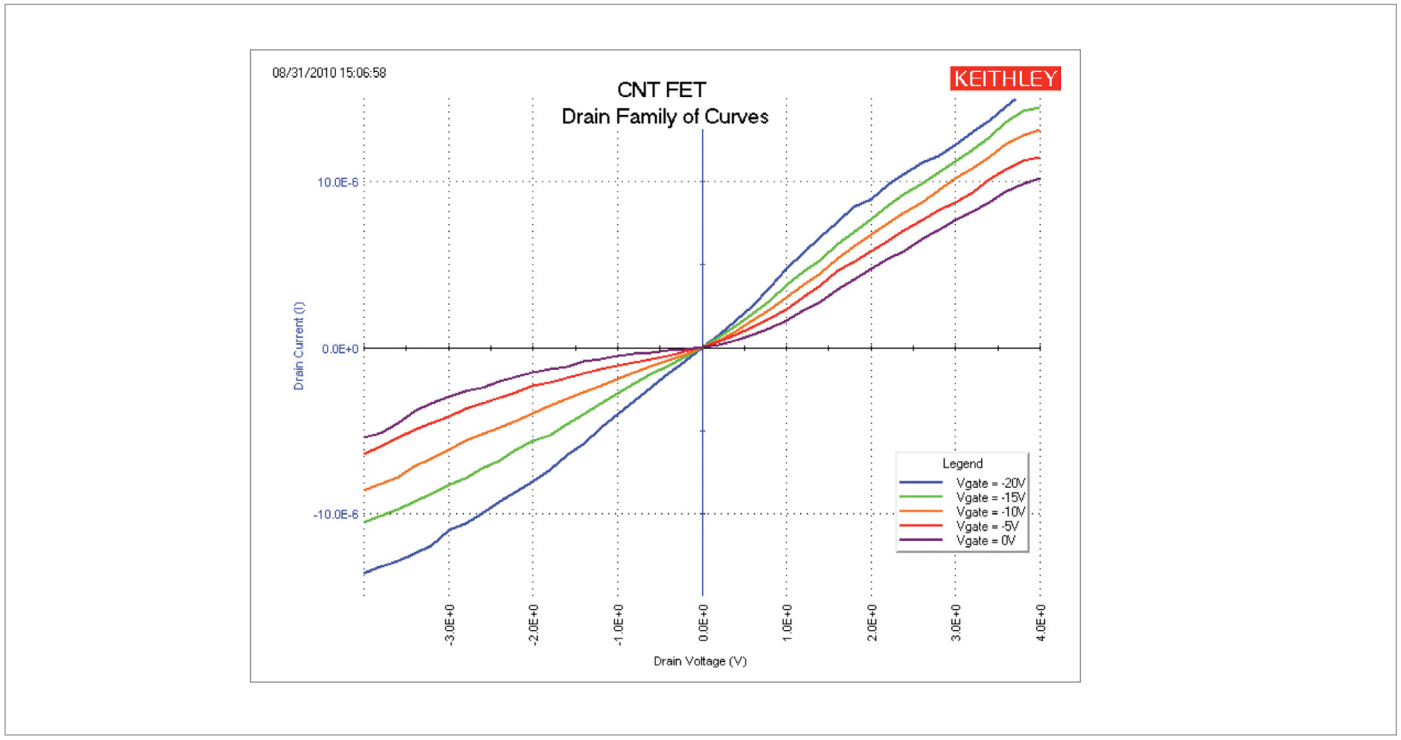


Figure 4. DC I-V drain family of curves measured by the 4200-SMU Source Measure Unit

Without changing connections to the device, 4200A-SCS's interactive Clarius software simplifies performing other common I-V tests such as the drain current (I_d) vs. gate voltage (V_g) curves. For this test, the gate voltage is swept and the resulting drain current is measured at a constant drain voltage. The results of an I_d–V_g curve at a constant drain voltage are shown in **Figure 5**. The drain voltage can also be stepped as the gate voltage is swept.

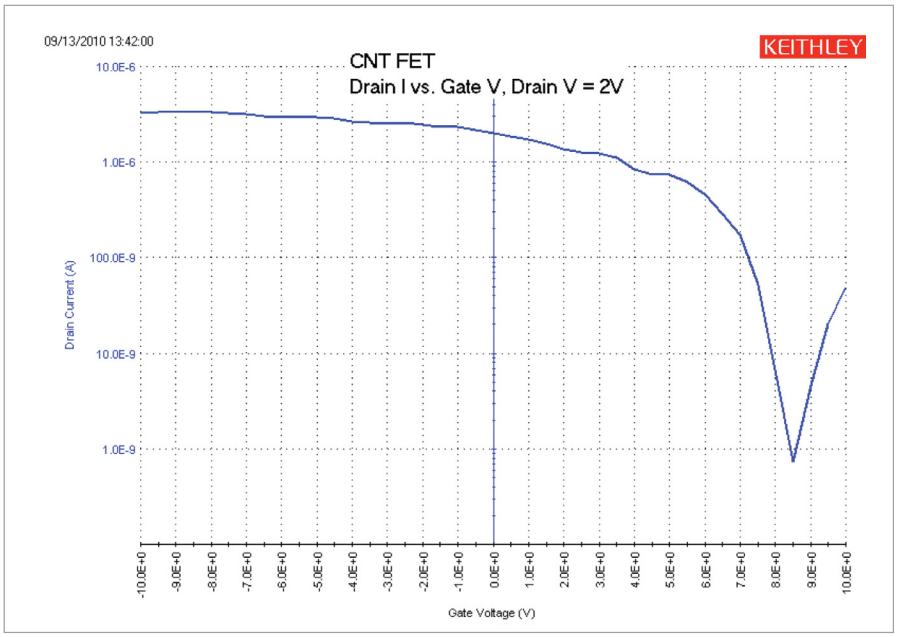


Figure 5. Drain current vs. gate voltage of CNT FET.

Optimizing DC measurements

The following techniques will improve the quality of DC measurements made on CNT FETs with the 4200A-SCS:

- **Limit Current:** To prevent damage to the device while performing I-V characterization, the user should limit the amount of current that can flow through the device. This can be done in the software by setting the Current Compliance of each SMU to a safe level, such as 20 µA. This is a programmed limit to ensure the current doesn't exceed the user-defined compliance.
- **Provide Sufficient Settling Time:** Because CNT FET measurements often involve measuring low current (<1 µA), it is important to allow sufficient settling time to ensure the measurements are stabilized after a current or voltage has been applied. Some of the factors that affect the settling time of the measurement circuit include the cables, test fixtures, switches, probers, the DUT resistance, and the current range of the measurement instrument. To ensure settled readings, additional delay time can be added to the voltage or current step time prior to the measurement. This delay time can be easily adjusted in the Test Settings pane within the Clarius software.
- **Use Proper Speed Modes:** The Test Settings pane also offers Speed Modes, including Delay and Filter Factor settings, which affect the settling time of the reading, as well as the integration time of the measurement. Increasing the Delay Factor, Filter Factor, and the A/D Aperture Time can decrease noisy measurements.
- **Minimize Noisy Measurements:** Noise may be generated from a variety of sources, including particle collisions, defects, AC pick-up, and electrostatic interference. Noisy measurements result when a noise signal is superimposed on the DC signal being measured. This can result in inaccurate or fluctuating measurements.

  The most common form of external noise "pick-up" is 60 Hz (or 50 Hz) line cycle pick-up. This can be a common occurrence near fluorescent lights. Millivolts of noise are not uncommon. Keithley uses a technique called Line-Cycle Integration to minimize the effects of 60 Hz (or 50 Hz) line pick-up. Line-cycle noise will "average out" when the integration time is equal to an integral number of power line cycles. The number of power line cycles can be adjusted in the Clarius software in the Advanced Test Settings dialog box on the right side of the screen.

Electrostatic interference is another cause of noisy measurements when measuring low currents. This coupling occurs when an electrically charged object approaches the circuit under test. In high impedance circuits, this charge doesn't decay rapidly and can result in unstable measurements. The erroneous readings may be due to either DC or AC electrostatic fields, so electrostatic shielding will help minimize the effects of these fields.

The electrostatic shield can be just a simple metal box that encloses the test circuit. Probe stations often include an electrostatic/EMI shield or optional dark box. The shield should be connected to the measurement circuit LO, which is the Force LO terminal of the SMU. The Force LO terminal is the outside shield of the triax cable of the SMU or is located on the GNDU. All cables need to be of a low-noise design and shielded. Each SMU comes with two low-noise triax cables.

Keep Probes Up: Make sure the probes are in the up position (not contacted to the device) when connecting and disconnecting instruments from the terminals of the device. The process of moving cables has the potential to inject charge into the device and cause damage. This is due to both triboelectric and piezoelectric effects.

Pulsed I-V Measurements

In addition to making traditional DC I-V measurements, it may be desirable to perform ultra-fast pulsed I-V measurements for various reasons. First, it may be important to observe the high speed response of the CNT device. In some cases, nanostructures can be destroyed by the heat generated when making traditional DC measurements. Pulsed I-V measurements can reduce the total energy dissipated in a device, and therefore reduce the potential for damage. Finally, pulsed electrical testing can prevent current drifting in measurements that can occur during DC measurements.

The pulsed I-V measurements on the CNT FET can be easily made using the 4225-PMU Ultra-Fast I-V Module. The PMU provides two channels of high speed, multi-level voltage pulse output while simultaneously measuring current and voltage. This module replaces traditional pulse/measure test configurations, which consisted of a pulse generator, digital oscilloscope, interconnect hardware, and software.

The PMU has two modes of ultra-fast I-V source with measure: pulsed I-V and transient I-V. These two modes are illustrated in **Figure 6.**

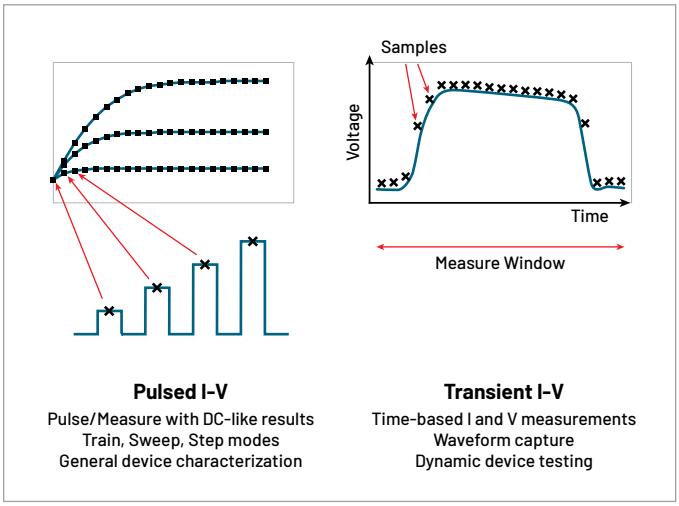


Figure 6. Two modes of ultra-fast I-V source with measure: Pulsed I-V and Transient I-V.

Pulsed I-V refers to any test with a pulsed source and a corresponding high speed, time-based measurement that provides DC-like results. The current and/or voltage measurement is an average of readings taken in a predefined measurement window on the pulse. This average of readings is called the "spot mean." The user defines the parameters of the pulse, including the pulse width, duty cycle, rise/fall times, amplitude, etc.

Transient I-V, or waveform capture, is a time-based current and/or voltage measurement that is typically the capture of a pulsed waveform. A transient test is typically a single pulse waveform that is used to study time-varying parameters, such as the drain current degradation versus time due to charge trapping or self-heating. Transient I-V measurements can be used to test a dynamic test circuit or as a diagnostic tool for choosing the appropriate pulse settings in the pulsed I-V mode.

Given that the 4225-PMU has two channels, only one module is needed to test a three-terminal CNT FET. A typical test configuration for connecting the PMU module to a CNT FET is shown in **Figure 7.** In this diagram, Ch 1 of the PMU is connected to the Gate terminal and Ch 2 is connected to the Drain terminal. The Source terminal is connected to the PMU Common, which is the outside shield of the PMU coax connector. To connect this Common terminal to the probe tip, use a BNC or triax shorting plug that will connect the

outside of the coax to the manipulator probe. To generate a V_{ds}–I_d curve, Ch 1 steps the gate voltage and Ch 2 sweeps the drain voltage and measures the resulting drain current.

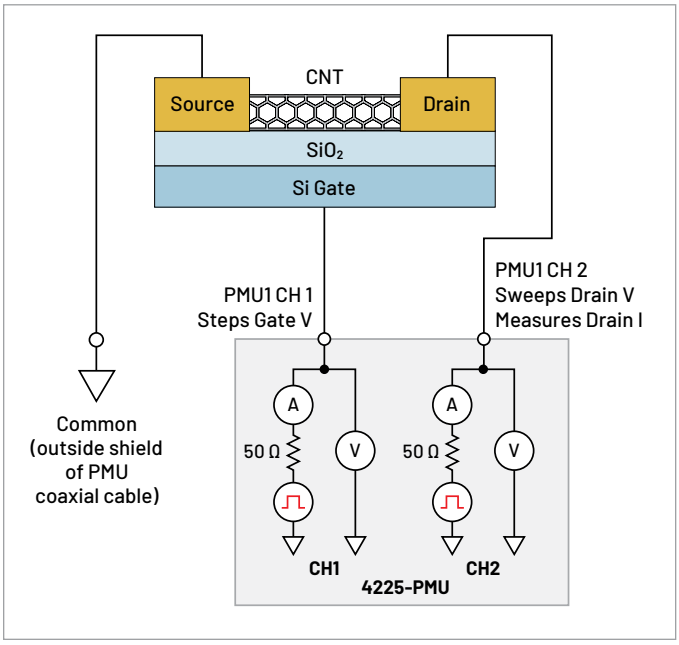


Figure 7. Circuit diagram for measuring the pulsed I-V characteristics of a CNT FET.

Figure 8 illustrates a pulsed I-V drain family of curves taken with the PMU. For this measurement, a pulse width of 500 µs was used to generate the curves. However, each PMU channel has the ability to output voltage pulses as short as 70 ns with a rise time as short as 20 ns. The minimum duration of the pulse width will depend on several factors, including the test circuit RC time constant and the magnitude of the test current. Each dot on the curves represents a "spot mean" measurement on the pulsed waveform.

The PMU has five ranges full scale from 800 mA down to 100 µA. To measure lower currents, using the 4225-RPM optional Remote Amplifier/Switch is recommended because it adds six measurement ranges, down to 100 nA full scale. The pulsed I-V curves shown in **Figure 8** were taken on the 100 µA range. The threshold current was set to 20 µA so that the test will stop if the threshold current level is reached.

For some applications, it may be necessary to study the transient response of a CNT FET. If this is the case, the waveform capture mode (transient I-V) can be used to capture the current and voltage time-based response to the device. **Figure 9** shows the transient response of the CNT FET. The blue curve is the pulsed drain voltage and the red curve is the resulting current response as a function of time.

The blue voltage output curve looks close to the defined rise and fall times of 10µs with a pulse width of 50 µs. Note that the pulse width is measured at one-half of the input amplitude of 1 V. Therefore, the pulse width is measured at 500 mV. The sample period in this example is 25 ns (40 MHz rate). With proper cabling and connections, the voltage shape should be output as defined by the user with minimal deviation.

The red curve shows the drain current and is plotted on the right Y-axis. The drain current is measured at constant drain and gate voltages. The peaks in the curve are caused by charging and discharging of the cabling, as well as the current flow through the device. Note that these peaks occur during the pulse transitions. Reducing the pulse amplitude or increasing the pulse transition time reduces the dV/dt, which reduces the peak height.

Optimizing Pulsed I-V Measurements

To improve the quality of pulsed I-V measurements made with the 4200A-SCS, follow these guidelines:

- **Use the Right Cables and Connections:** Using proper cabling and connections is important for ultra-fast I-V applications in order to achieve the highest frequency output and to avoid signal distortions and capacitive charging effects.
  - Use cabling and connections optimized for high frequency (at least 150 MHz).
  - Use a signal path that matches the impedance of the instrument (50 ohms).
  - Tie the low side of the DUT to the shield of the PMU coax cable.
  - Connect the shields from each PMU channel together as close as possible to the DUT.
  - Minimize the loop area once the center conductor and shield are separate in the test circuit.
  - Minimize the cable length.

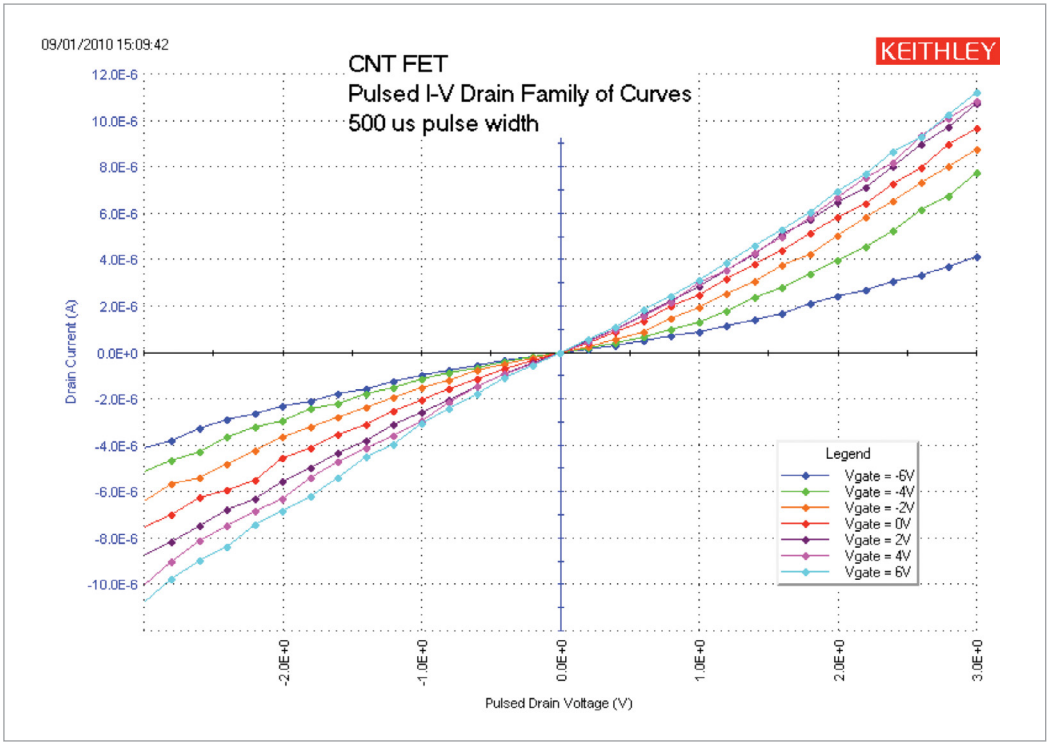


Figure 8. Pulsed I-V drain family of curves of CNT FET.

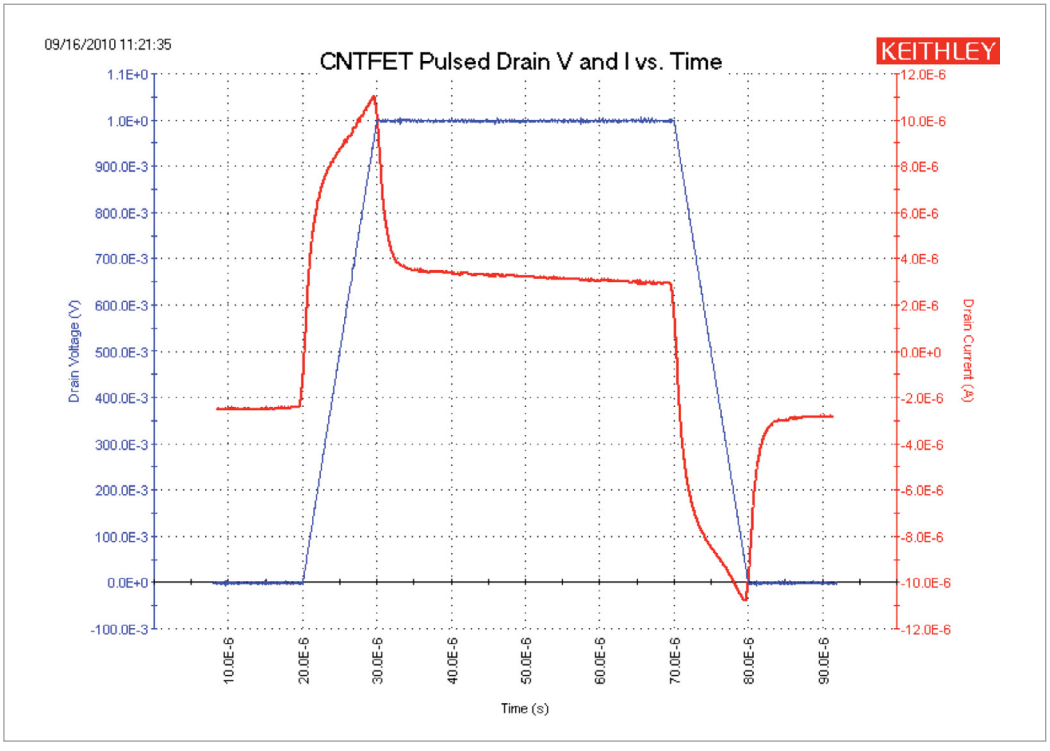


Figure 9. Waveform of single drain voltage pulse and resulting drain current of CNT FET.

- **Make the Right Chuck Connections:** CNT FETs and other nanotransistors may be either back-gated or top-gated. For back-gated devices, one of the PMU channels needs to be connected to the chuck of the prober. When making PMU connections to the chuck, the user will give up some functionality of the PMU: fast transitions, high frequency, low current, etc. This is because the output of the high frequency PMU channel is connected to the chuck capacitance and the chuck cabling, which slows down the source response and couples noise into the measurement. If possible, it is better to use a third manipulator and probe directly to the chuck. For high speed sourcing and measuring, it is best to use all top-side connections and avoid connecting the PMU to the chuck.
- **Verify Pulse Width:** Ensure the pulse width is long enough to ensure a settled reading. Verify the resulting current measurement is settled by outputting a single pulse using the Waveform Capture mode. Both the current and voltage can be plotted as a function of time in the Graph.
- **Minimize Noise:** To minimize noisy results, multiple waveforms can be averaged or a moving average function can be created in the built-in Formulator to smooth out the measurements further.

Capacitance-Voltage Measurements

In addition to performing DC and pulsed I-V measurements on CNT FETs, measuring the capacitance of the FET can also provide information about the device, including the mobility, timing effects, and gate dielectrics. **Figure 10** outlines the connections of the 4210-CVU or 4215-CVU to the CNT FET. In this configuration, the gate-to-drain capacitance is measured as a function of the gate voltage.

The HCUR/HPOT terminals that connect the high of the voltage source to the gate should be connected to the chuck. The LCUR/LPOT terminals that measure the capacitance should be connected to the drain terminal of the DUT. For best results, the measurement terminals should never be connected to the chuck. For top-gated CNT FETs, both the measure and voltage source can be output to the gate of the FET from the same terminals (either HCUR/HPOT or LPOT/LCUR) of the CVU. The HI and LO terminals of the CVU are interchangeable in the Terminal Settings window of the CVU in the Clarius software. The results of generating a C-V sweep between the gate and drain of the CNT FET are shown in **Figure 11.**

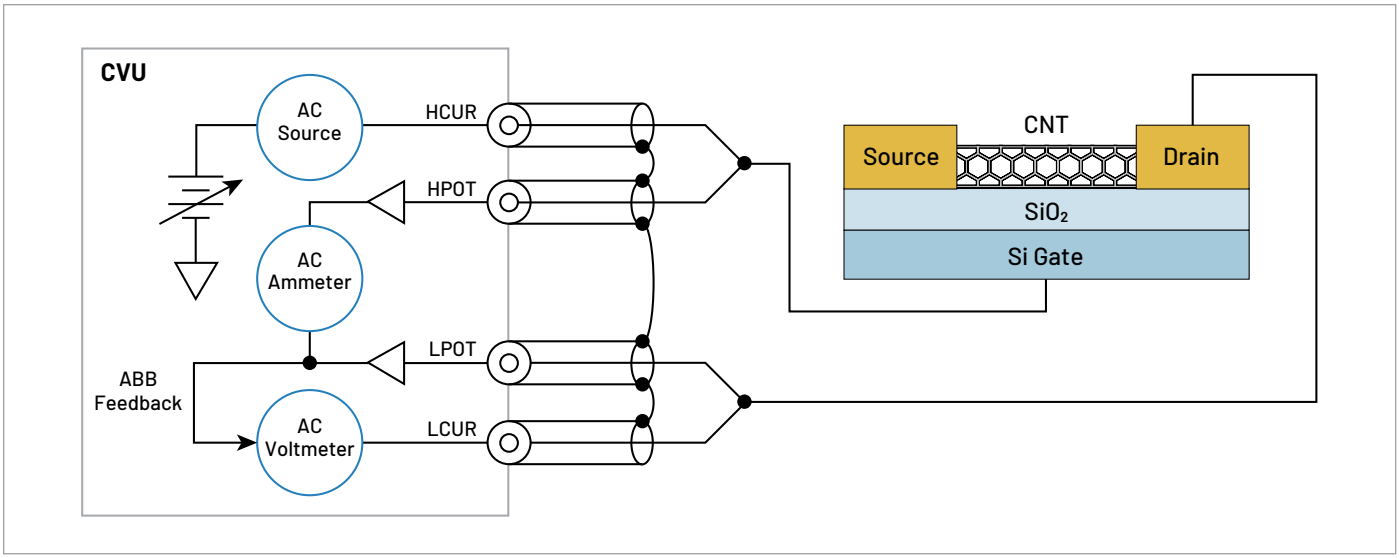


Figure 10. Connections of the CVU to a CNT FET.

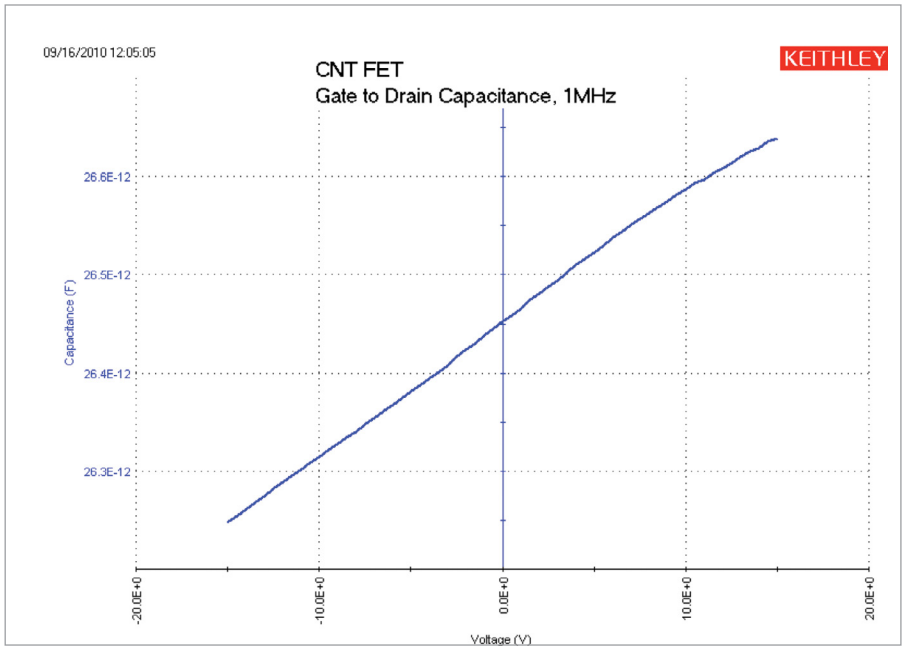


Figure 11. C-V sweep of gate-to-drain capacitance.

Optimizing Capacitance Measurements

To improve the quality of capacitance measurements made with the CVU, follow these guidelines:

- **Perform Open Compensation (for Measurements <10 pF):** The open correction feature compensates for capacitance offsets in the cabling and connections. Performing the correction is a two-part process. The corrections are performed, and then they are enabled within a test module.

  To perform the corrections, select Tools at the top of the screen and select CVU Connection Compensation. For an Open correction, select Measure Open. Probes must be up or the DUT removed from the test fixture. Enable the correction by selecting Open Compensation button in the Terminal Settings pane.
- **Use Proper Shield Connections:** Connect the shields of the coax cables together as close as possible to the DUT. This reduces the loop area of the shields, which minimizes the inductance. This also helps to maintain the transmission line effects. If the shields are not connected together, offsets may occur. The higher the frequency, the more important this becomes.
- **Choose Appropriate Hold and Sweep Delay Times:** The condition of a device when all internal capacitances are fully charged after an applied voltage step is referred to as "equilibrium." If capacitance measurements are made before the device is in equilibrium, inaccurate results may occur.

  To choose the delay times for a C-V sweep, step an applied voltage using the Sampling Mode, and plot the capacitance as a function of time. Observe the settling time from the graph. Use this time for the Hold Time for the initial applied voltage or for the Sweep Delay Time applied at each step in the sweep. The Sweep Delay Time may not need to be as long as the first step. The user will need to experiment to verify the appropriate time.
- **Choose Appropriate Speed Mode in the Test Settings window:** The Speed mode function enables the user to adjust the time for settling and integration of the measurement. For small capacitances (pico-Farads or less) use the Quiet or Custom Speed modes for best results.

- **Use Guarding:** When making very small capacitance measurements, guarding will help prevent stray capacitance from unused terminals of the device from affecting measurement accuracy. For example, if measuring the capacitance between only the gate and drain terminals, the source terminal of the FET can be connected to the guard. The guard terminal of the CVU is the outside shield of the coax cable.

Conclusion

When using the appropriate instrumentation and measurement techniques, optimal electrical characterization of CNT FETs can be achieved. The 4200A-SCS is an ideal tool for performing electrical characterization of CNT FETs and other nanostructures because of its integrated hardware, software, and analysis tools. The SMUs can be used to determine V_{ds}–I_d, V_{GS}–I_d, resistance, and other I-V measurements on the CNT FET. The PMU can be used to make pulsed I-V measurements or observe the transient response of a pulsed waveform applied to the DUT. The CVU can be used to generate C-V, C-f, or C-t curves. Using the Carbon Nanotube Transistor Characterization (*cntfet*) project that comes with the 4200A-SCS can further simplify measurement setup and execution.

Acknowledgement

The author appreciates the assistance provided by Sandia National Labs, Livermore, California, who supplied the CNT FETs used in the device testing process during the development of this application note.

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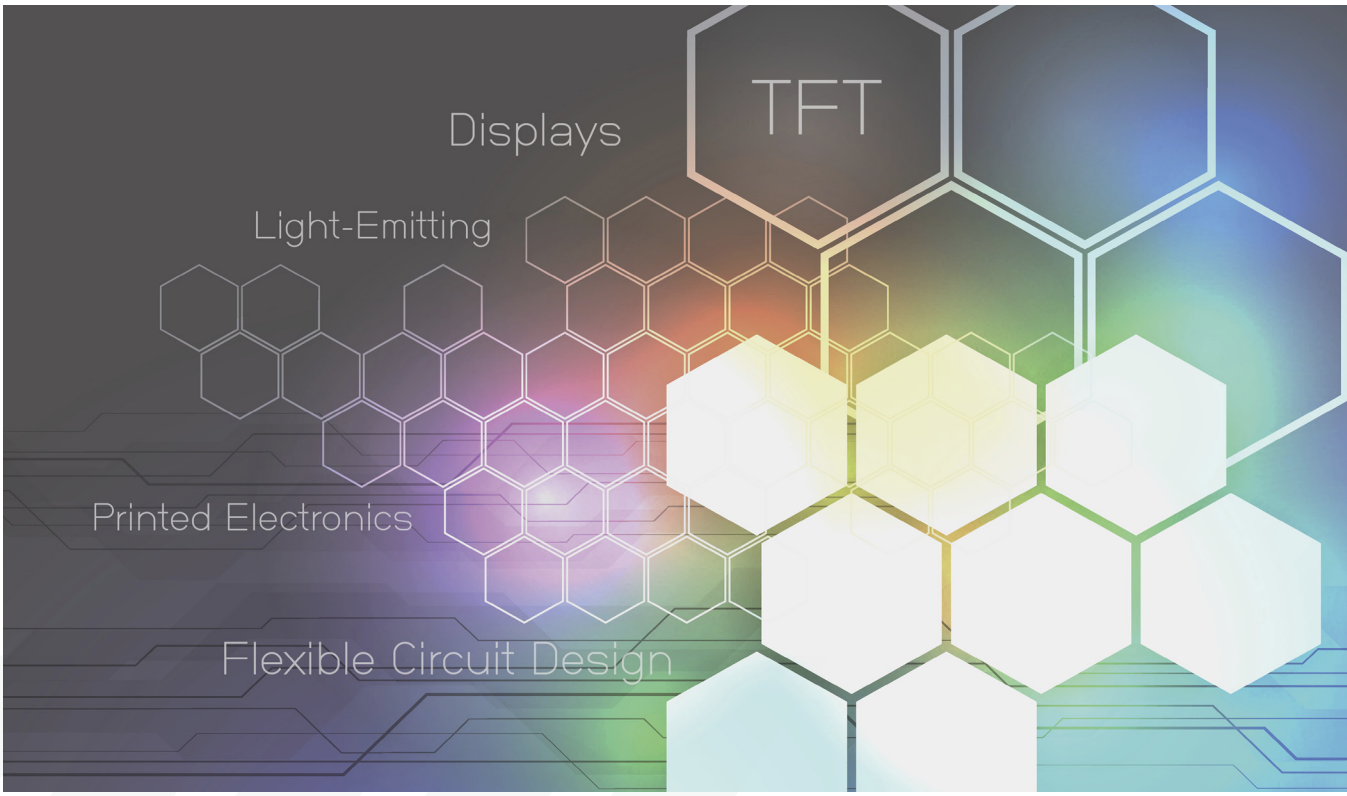
DC I-V and AC Impedance Testing of Organic FETs



Introduction

Organic semiconductor devices have been developed as replacements for traditional semiconductor devices because they use lower cost materials, are less expensive to manufacture, can be printed onto surfaces such as paper and glass, and can be used in flexible circuit designs. These devices are used in a range of applications that includes displays, medical devices, lighting, sensors, memory devices, batteries, and solar cells. One of the most common organic semiconductor devices is the Organic Field Effect Transistor (OFET).

OFET research generally seeks to optimize the performance of the device, such as its carrier mobility and on/off current ratio. DC I-V techniques are used to determine the output and transfer characteristics, hysteresis effects, bias stressing, gate leakage current, etc. AC impedance techniques can reveal critical information about the device, like its carrier mobility, threshold voltage, flat band voltage, and charge effects.

This application note outlines how to optimize DC I-V and AC impedance measurements on OFETs using the 4200A-SCS Parameter Analyzer. Timing parameters, noise reduction, shielding, proper cabling, and other important measurement considerations for achieving the best results will be discussed.

The Organic Field Effect Transistor (OFET)

The OFET is a type of field effect transistor that uses an organic semiconductor material as the channel between the source and drain terminals of the device. The organic thin film transistor (OTFT) is a type of OFET; for this application note, these two FETs will be used synonymously. **Figure 1** illustrates a bottom-gated OFET. The organic semiconductor is placed above a dielectric that sits above the gate terminal. Two metal contacts are located across the top of the organic semiconductor for the source and drain terminals. Connections are made to the three device terminals to perform the electrical measurements.

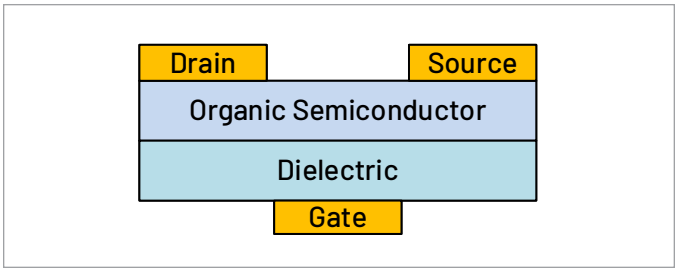


Figure 1. Bottom-gated organic field effect transistor.

Making Electrical Measurements with the 4200A-SCS

The 4200A-SCS system includes tests for making some of the most commonly used electrical measurements on organic FETs. These tests for making DC I-V, very low frequency C-V, and high frequency C-V measurements can be found in the Test Library by searching on the keyword "ofet" or "organic" while in the Select view of the Clarius software. All these tests can also be found in the Organic FET Characterization Project (***ofet***) in the Project Library using the keyword, "ofet" or "organic" in the Search field. **Figure 2** shows a screen capture of this project. In addition to the provided tests, the user can also easily create their own tests and projects based on their application and measurement requirements.

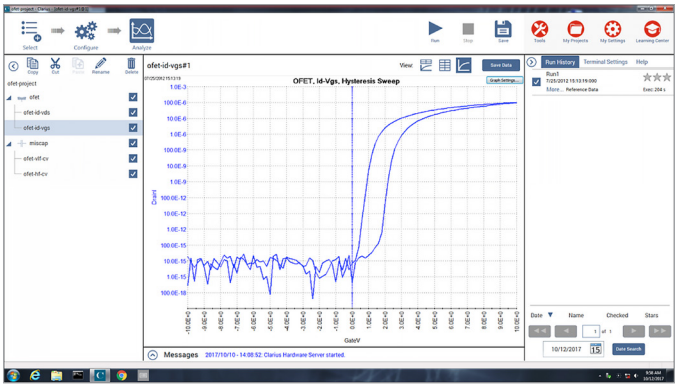


Figure 2. Screen capture of Organic FET Characterization Project.

Current-Voltage Measurements

The I-V characteristics of an organic device can be used to extract many of the device's parameters, study the effects of fabrication processes, and determine the quality of the contacts. The Test Library and Organic FET Characterization project includes tests to measure the output characteristics (I_D-V_{DS}) and transfer characteristics (I_D-V_{GS}) of an OFET.

Figure 3 illustrates a DC I-V test configuration for measuring the transfer characteristics of an OFET using two SMUs (4200-SMU, 4201-SMU, 4210-SMU or 4211-SMU) with optional 4200-PA preamps. These SMUs are capable of sourcing and measuring both current and voltage. They have pico-amp sensitivity and can be current-limited to prevent damage to the device. In this diagram, SMU1 is connected to the gate of the OFET and SMU2 is connected to the drain terminal. The source terminal is connected to the ground unit (GNDU) or it can be connected to a third SMU if it is necessary to source and measure from all three terminals of the OFET.

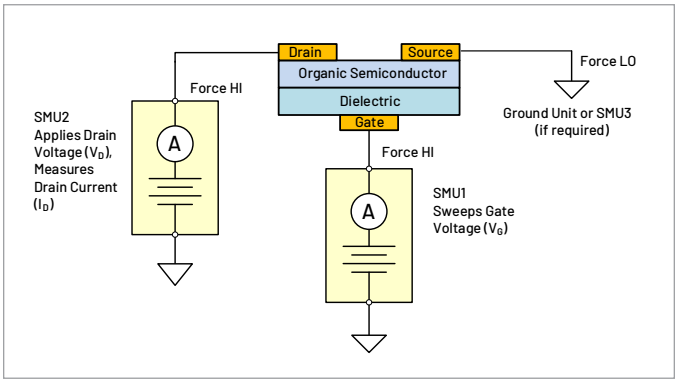


Figure 3. Circuit diagram for measuring the DC I-V characteristics of an OFET.

Once the SMUs are connected to the OFET, the transfer characteristics can be generated using the Organic FET Drain Current vs. Gate Voltage (***ofet-id-vgs***) test in the Test Library. In this test, SMU2 applies a constant drain voltage (V_D) and measures the drain current (I_D) while SMU1 sweeps the gate voltage (V_G). **Figure 4** shows the results of measuring the drain current as a function of the gate voltage of an OFET. The hysteresis sweep is performed using the Dual Sweep function in the software. Notice the many decades of current—from femto-amps to milli-amps—that the SMUs with preamps can measure.

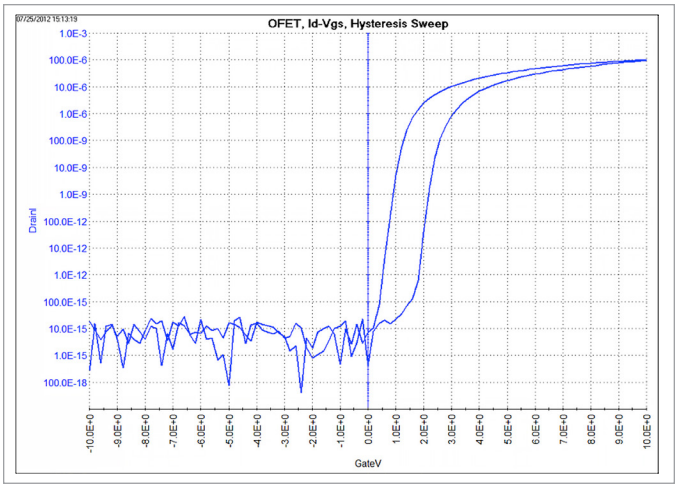


Figure 4. ID-VGS curve of an OFET.

The SMUs connected to each terminal of the OFET can be easily reconfigured in the Clarius software to perform other tests. The output characteristics, I_D vs. V_D, can also be measured by changing the SMU parameters in the software. It's also possible to use the preconfigured Organic FET Output Characteristics (***ofet-id-vds***) test in the Test Library. By stepping the gate voltage and measuring the drain current as a function of drain voltage, a drain family of curves can be generated. **Figure 5** shows the results of measuring I_D-V_{DS} curves of a p-type OFET using the ***ofet-id-vd***s test.

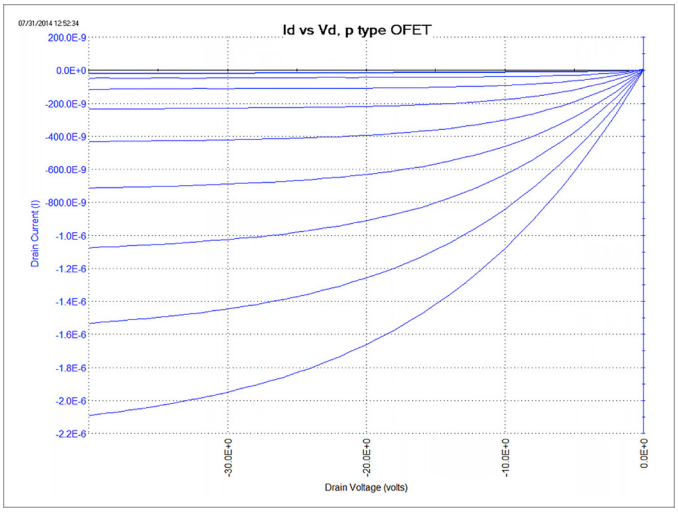


Figure 5. Output Characteristics of a p-type OFET.

Optimizing DC I-V Measurements

The following techniques will improve the quality of DC measurements made on organic FETs with the 4200A-SCS:

Eliminate Lead and Contact Resistance: The series resistance of the cables used to connect the SMU to the device can cause measurement errors. The effects of the cable resistance are particularly detrimental when using long connecting cables and high currents because the voltage drop is significant compared to the measured voltage.

As shown in **Figure 6**, the voltage drop due to the cable resistance is added to the voltage measurement of a DUT when making 2-wire, or local sense, connections. In this case, the current flows across both cables, as well as the DUT, causing three voltage drops that all are measured by the SMU voltmeter. To eliminate the cable resistance from the measurement, a 4-wire or remote sense connection is made to the device, as shown in the right half of **Figure 6**. In this case, only the voltage drop across the DUT is measured by the SMU voltmeter.

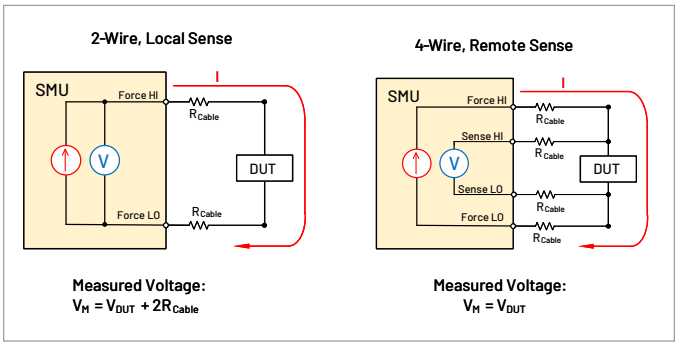


Figure 6. Local vs. Remote Sense.

Minimize Noise in Measurements: Noise may be generated from a variety of sources, including AC pickup and electrostatic interference. Noisy measurements result when a noise source is superimposed on the DC signal being measured. This can result in inaccurate or fluctuating measurements.

The most common form of external noise pickup is 60 Hz (or 50 Hz) line cycle pickup. This can be a common occurrence near fluorescent lights. Millivolts of noise are not uncommon. Keithley uses a technique called Line-Cycle Integration to minimize the effects of 60 Hz (or 50 Hz) line pickup. Line-cycle noise will average out when the integration time, or measurement window, is equal to an integral number of power line cycles. This A/D aperture time (measurement window) can be adjusted using the Speed setting in the Test Settings pane.

Electrostatic interference is another cause of noisy measurements when measuring low currents. This coupling occurs when an electrically charged object approaches the circuit under test. In high impedance circuits, this charge doesn't decay rapidly and can result in unstable measurements. The erroneous readings may be due to either DC or AC electrostatic fields, so electrostatic shielding will help minimize the effects of these fields.

An electrostatic shield can be just a simple metal box that encloses the test circuit. However, this can be difficult when working within a laboratory glove box, which is often used with organic devices. Probe stations often include an electrostatic/EMI shield or optional dark box. As shown in **Figure 7**, the shield surrounds the device and is connected to the measurement circuit LO, which is the Force LO terminal of the SMU. The Force LO terminal is the outside shield of the triax cable of the SMU and is also located on the rear panel of the 4200A-SCS in the ground unit (GNDU). All cables need to be low noise and shielded. Each SMU comes with two low noise triax cables.

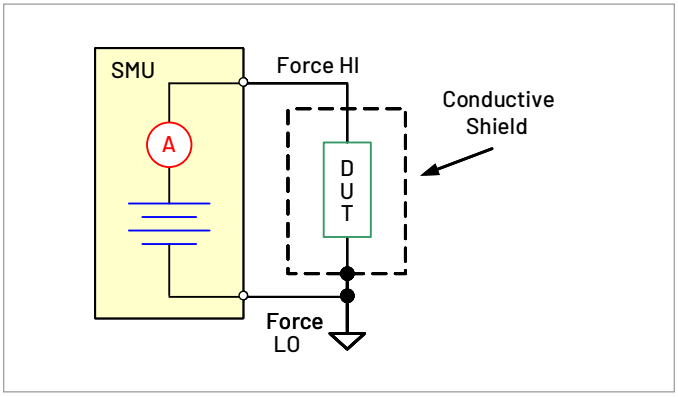


Figure 7. Conductive Shield Surrounds Device Under Test.

Provide Sufficient Settling Time: Because device leakage current usually involves measuring very low current (<1 nA), it is important to allow sufficient settling time to ensure the measurements are stabilized after a voltage bias has been applied. Some of the factors that affect the settling time of the measurement circuit include the cables, test fixtures, switches, probers, the DUT resistance and capacitance, and the current range of the SMU. To ensure settled readings,

additional delay time can be added to the voltage step prior to the measurement. This delay time can be easily adjusted in the Test Settings pane in the Clarius software.

Very Low Frequency Capacitance-Voltage Technique

In addition to measuring very small currents, two SMUs with preamps can be used to measure Very Low Frequency C-V (VLF C-V). C-V sweeps and C-t measurements can be made with test frequencies from 10 mHz to 10 Hz. **Figure 8** is a simplified diagram of the two-SMU configuration used to generate low frequency impedance measurements. This configuration requires a 4200A-SCS Parameter Analyzer with two SMUs and two 4200-PA preamps with one connected to either side of the device under test. SMU1 outputs the DC bias with a superimposed AC signal and measures the voltage. SMU2 measures the resulting AC current while sourcing 0V DC.

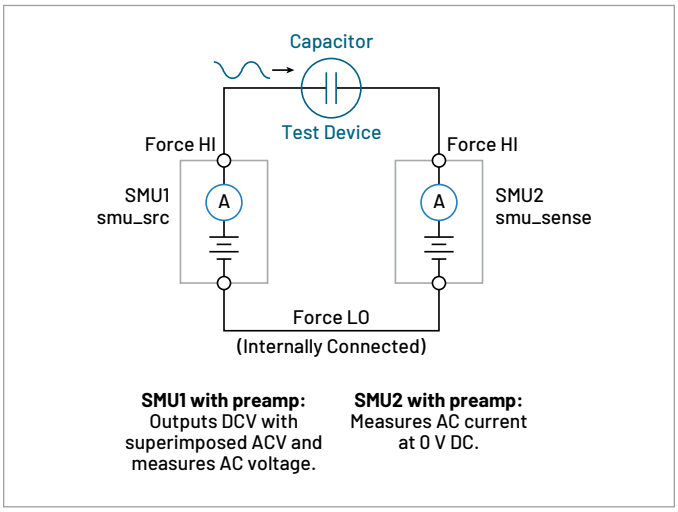


Figure 8. Connections for Very Low Frequency C-V measurements.

While the voltage is forced, voltage and current measurements are obtained simultaneously over several cycles. The magnitude and phase of the DUT impedance is extracted from the discrete Fourier transform (DFT) of a ratio of the resultant voltage and current sinusoids. The narrow-band information can be collected at varying frequencies (10 mHz to 10 Hz) to measure the complex impedance of the DUT. The resulting output parameters include the impedance (Z), phase angle (θ), capacitance (C), conductance (G), resistance (R), reactance (X), and the dissipation factor (D).

Because the very low frequency method works only over a limited frequency range, the capacitance of the device under test (DUT) should be in the range of 1 pF to 10 nF. **Table 1** summarizes the VLF C-V specifications. Complete specifications and more detailed information about this technique can be found in a Keithley application note, "Performing Very Low Frequency Capacitance-Voltage Measurements of High Impedance Devices Using the 4200A-SCS Parameter Analyzer."

Table 1. Typical Measurement Accuracy[2]

Frequency	Measured Capacitance	C Accuracy @ 300 mV rms[1]	C Accuracy @ 30 mV rms[1]
10 Hz	1 pF	10%	13%
	10 pF	10%	10%
	100 pF	5%	5%
	1 nF	5%	9%
	10 nF	5%	5%
1 Hz	1 pF	2%	2%
	10 pF	1%	2%
	100 pF	2%	1%
	1 nF	2%	1%
	10 nF	2%	2%
100 mHz	1 pF	2%	3%
	10 pF	2%	2%
	100 pF	2%	2%
	1 nF	1%	2%
	10 nF	2%	1%
10 mHz	1 pF	5%	10%
	10 pF	1%	2%
	100 pF	1%	1%
	1 nF	1%	1%
	10 nF	2%	2%

NOTES

1. ±20V maximum includes the DC Bias and the AC Test Signal peak voltage. Maximum negative bias voltage = –20 + (AC voltage * $\sqrt{2}$). Maximum positive bias voltage = 20 – (AC voltage * $\sqrt{2}$).
2. Test device must have dissipation factor D_X <0.1. All data shown for DC Bias voltage = 0V.

All specifications apply at 23°C ±5°C, within one year of calibration, RH between 5% and 60%, after 30 minutes of warmup.

VLF C-V Characterization of Organic FETs

The built-in software for performing VLF C-V measurements can be used on different types of devices, including organic FETs and MIS capacitor devices. **Figure 9** shows the results of performing a C-V sweep with a test frequency of 0.25 Hz on an OFET between the gate and drain terminals using the Organic FET Very Low Frequency C-V Sweep (***ofet-vlf-cv***) test in the Test Library.

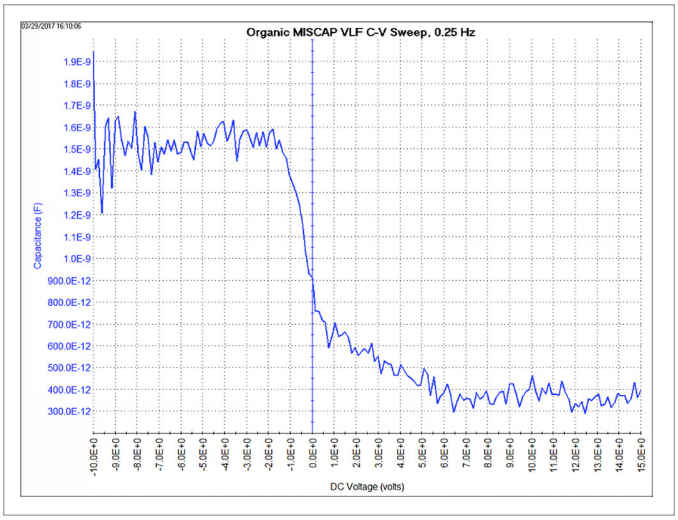


Figure 9. A Very Low Frequency C-V Sweep of an OFET at a Test Frequency of 0.25 Hz.

High Frequency Capacitance-Voltage Measurements

In addition to DC I-V and VLF C-V measurements, measuring the capacitance of an OFET can provide information about the device, including the gate capacitance and the carrier mobility. **Figure 10** shows the connections of the 4210-CVU or 4215-CVU Capacitance Voltage Unit to an OFET. In this configuration, the gate-to-drain capacitance is measured as a function of the gate voltage.

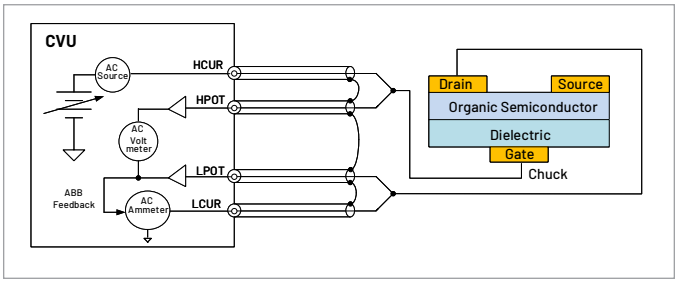


Figure 10. Connections from the CVU to an OFET.

Using the Organic FET C-V Sweep (***ofet-hf-cv***) test in the Test Library, a C-V sweep from –10 V to 10 V at 50 kHz was generated on an OFET between the gate and drain terminals. The results of the C-V sweep are shown in **Figure 11**.

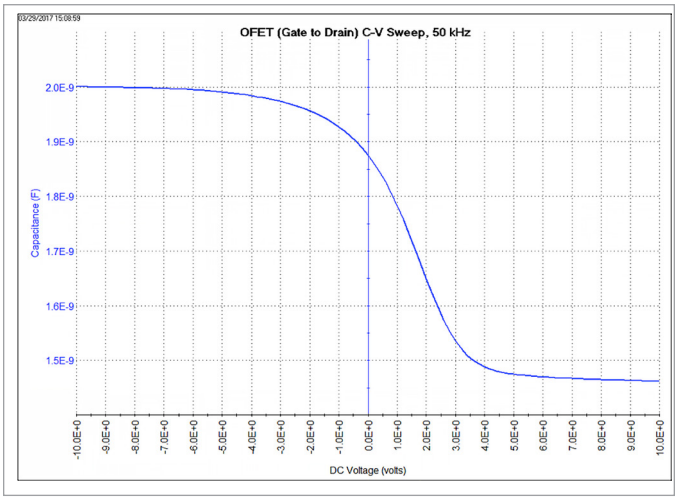


Figure 11. High Frequency C-V Sweep of an OFET.

Optimizing Capacitance Measurements

To improve the quality of capacitance measurements made with the 4200A-SCS, follow these guidelines:

Perform Open Compensation (for measurements <10 pF): The open correction feature compensates for capacitance offsets in the cabling and connections. Performing the correction is a two-part process. The corrections are performed, and then they are enabled within a test.

To perform the corrections in the Clarius software, select ***Tools*** at the top of the screen and select ***CVU Connection Compensation***. For an Open correction, select ***Measure Open***. Probes must be up or the DUT removed from the test fixture. Once the correction data is acquired from the Tools menu, the correction is enabled within a test by selecting ***Open Compensation*** in the Terminal Settings pane.

Choose Appropriate Hold and Sweep Delay Times: The condition of a device when all internal capacitances are fully charged after an applied voltage step is referred to as "equilibrium." If capacitance measurements are made before the device is in equilibrium, the results of these measurements may be inaccurate.

To choose the appropriate delay times, apply DC voltage to the device using the Sampling Test Mode, and plot the capacitance as a function of time. Observe the settling time from the graph. This observed equilibrium time can be used as the Hold Time, which is the time the Presoak Voltage is output prior to the beginning of the Sweep or Sampling Operation Mode. The observed time can also be used for the Sweep Delay time applied for each step in the sweep. The Sweep Delay time may not need to be as long as the Hold Time. The user will need to experiment to verify the appropriate times to use in the Test Settings pane for a particular test.

Use Proper Shield Connections: When measuring AC impedance at test frequencies greater than 1 MHz, connect the shields of the coax cables together as close as possible to the device. This reduces the loop area of the shields, which minimizes the inductance. This also helps to maintain the transmission line effects. If the shields are not connected together, offsets may occur.

Choose the Appropriate Speed Mode in the Test Settings Window: The Speed Mode function allows adjusting the settling time and measure window (A/D aperture) of the measurements. For small capacitances, use the Quiet or Custom Speed modes for best results.

Conclusion

Appropriate instrumentation and measurement techniques make it possible to achieve optimal electrical characterization of organic FETs. The 4200A-SCS is an ideal tool for performing electrical characterization of OFETs because of its integrated hardware, interactive software, and analysis capabilities. The test system includes built-in tools, such as open correction, informational videos, the Help function, and timing controls to help researchers minimize set-up time and achieve the best measurement results as quickly as possible.

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Electrical Characterization of Photovoltaic Materials and Solar Cells with the 4200A-SCS Parameter Analyzer

I-V, C-V, C-f, DLCP, Pulsed I-V, Resistivity, and Hall Voltage Measurements

Introduction

The increasing demand for clean energy and the largely untapped potential of the sun as an energy source is making solar energy conversion technology increasingly important. As a result, the demand for solar cells, which convert sunlight directly into electricity, is growing. Solar or photovoltaic (PV) cells are made up of semiconductor materials that absorb photons from sunlight and then release electrons, causing an electric current to flow when the cell is connected to a load. A variety of measurements are used to characterize a solar cell's performance, including its output and its efficiency. This electrical characterization is performed as part of research and development of photovoltaic cells and materials, as well as during the manufacturing process.

Some of the electrical tests commonly performed on solar cells involve measuring current and capacitance as a function of an applied DC voltage. Capacitance measurements are sometimes made as a function of frequency or AC voltage. Some tests require pulsed current-voltage measurements. These measurements are usually performed at different light intensities and under different temperature conditions. A variety of important device parameters can be extracted from the DC and pulsed current-voltage (I-V) and capacitance-voltage (C-V) measurements, including output current, conversion efficiency, maximum power output, doping density, resistivity, etc. Electrical characterization is important in determining how to make the cells as efficient as possible with minimal losses.

Instrumentation such as the 4200A-SCS Parameter Analyzer can simplify testing and analysis when making these critical electrical measurements. The 4200A-SCS is an integrated system that includes instruments for making DC and ultra fast I-V and C-V measurements, as well as control software, graphics, and mathematical analysis capability. The 4200A-SCS is well-suited for performing a wide range of measurements, including DC and pulsed current-voltage (I-V), capacitance-voltage (C-V), capacitance-frequency (C-f), drive level capacitance profiling (DLCP), four-probe resistivity (ρ, σ), and Hall voltage (V_H) measurements. This application note describes how to use the 4200A-SCS to make these electrical measurements on PV cells.

Making Electrical Measurements with the 4200A-SCS

To simplify testing photovoltaic materials and cells, the 4200A-SCS is supported with tests and a project for making many of the mostly commonly used measurements easily. These tests, which include I-V, capacitance, and resistivity measurements, also include formulas for extracting common parameters such as the maximum power, short circuit current, defect density, etc. The *SolarCell* project (**Figure 1**) is included with all 4200A-SCS systems and can be found in the Project Library if you use the PV cell filter. Most of the tests in this project can also be found in the Test Library.

Table 1. Tests in the *SolarCell* project

Measurement	Name	Description
DC I-V	*fwd-ivsweep*	Performs I-V sweep and calculates I_{sc}, V_{oc}, P_{max}, I_{max}, V_{max}, FF
	rev-ivsweep	Performs reversed bias I-V sweep
Capacitance	*solarcell-cvsweep*	Generates C-V sweep
	solarcell-c-2vsv	Generates C-V sweep and calculates $1/C^2$
	cfsweep	Sweeps the frequency and measures capacitance
	dlcp	Measures capacitance as AC voltage is swept. DC voltage is applied so as to keep the total applied voltage constant. The defect density is calculated.
Pulse-IV	*solarcell-pulse-iv-sweep*	Performs pulse I-V sweep using one channel of PMU
4-Probe Resistivity	*hir*	Uses 3 or 4 SMUs to source current and measure voltage difference for high resistance semiconductor materials. Calculates sheet resistivity.
	lor	Uses 1 or 2 SMUs to source current and measure voltage using remote sense. Calculates sheet resistivity. Uses current reversal method to compensate for thermoelectric voltage offsets.
vdp Resistivity	*i1-v23*	First of 4 tests that are used to measure the van der Pauw resistivity. This test sources current between terminals 1 and 4 and measures the voltage difference between terminals 2 and 3.
	i2-v34	Sources current between terminals 2 and 1 and measures the voltage difference between terminals 3 and 4.
	i3-v41	Sources current between terminals 3 and 2 and measures the voltage difference between terminals 4 and 1.
	i4-v12	Sources current between terminals 4 and 1 and measures the voltage difference between terminals 1 and 2.

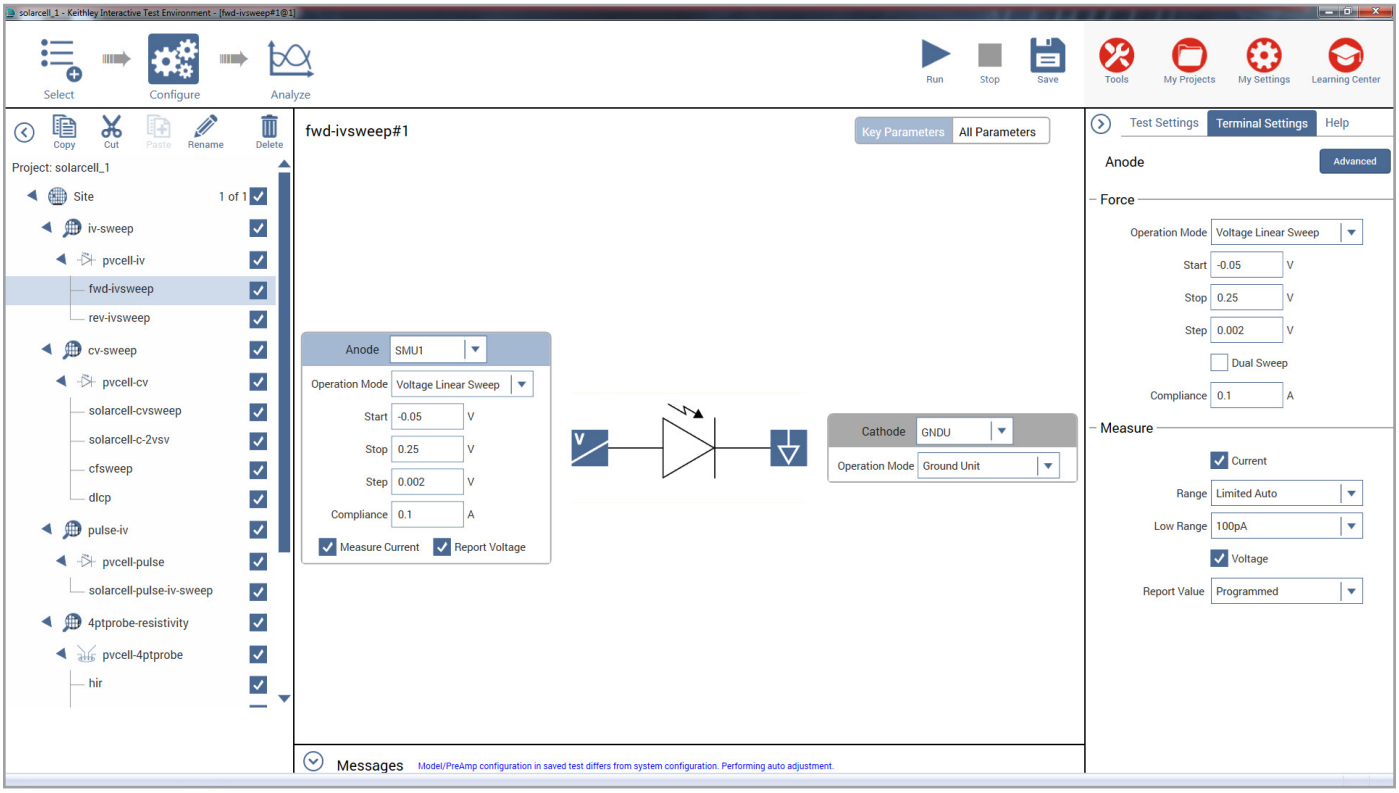


Figure 1. Screenshot of *Solar Cell* project for the 4200A-SCS

DC Current-Voltage (I-V) Measurements

As described previously, many solar cell parameters can be derived from current-voltage (I-V) measurements of the cell. These I-V characteristics can be measured using the 4200A-SCS's Source-Measure Units (SMUs), which can source and measure both current and voltage. Because these SMUs have four-quadrant source capability, they can sink the cell current as a function of the applied voltage. Four types of SMUs are available for the 4200A-SCS: the 4200-SMU or 4201-SMU, which can source/sink up to 100 mA, and the 4210-SMU or 4211-SMU, which can source/sink up to 1 A. If the output current of the cell exceeds these current levels, it may be necessary to reduce it, possibly by reducing the area of the cell itself. However, if this is not possible, Keithley's SourceMeter® instruments, which are capable of sourcing/sinking higher currents, offer possible alternative solutions.

Parameters Derived from I-V Measurements

A solar cell may be represented by the equivalent circuit model shown in **Figure 2**, which consists of a light-induced current source (I_L), a diode that generates a saturation current [$I_S(e^{qV/kT}-1)$], series resistance (r_s), and shunt resistance (r_{sh}). The series resistance is due to the resistance of the metal contacts, ohmic losses in the front surface of the cell, impurity concentrations, and junction depth. The series resistance is an important parameter because it reduces both the cell's short-circuit current and its maximum power output. Ideally, the series resistance should be 0 Ω ($r_s = 0$). The shunt resistance represents the loss due to surface leakage along the edge of the cell or to crystal defects. Ideally, the shunt resistance should be infinite ($r_{sh} = \infty$).

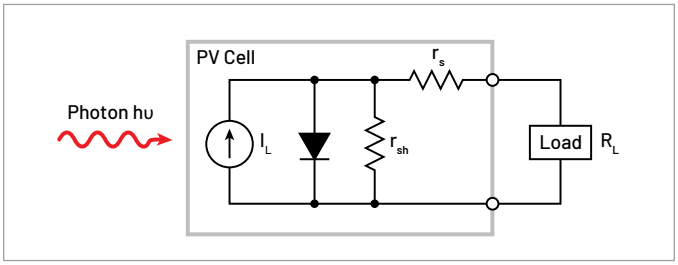


Figure 2. Idealized equivalent circuit of a photovoltaic cell

If a load resistor (R_L) is connected to an illuminated solar cell, then the total current becomes:

$$I = I_S(e^{qV/kT} - 1) - I_L$$

where:

I_S = current due to diode saturation

I_L = current due to optical generation

Several parameters are used to characterize the efficiency of the solar cell, including the maximum power point (P_{max}), the energy conversion efficiency (η), and the fill factor (FF). These points are illustrated in **Figure 3**, which shows a typical forward bias I-V curve of an illuminated PV cell. The maximum power point (P_{max}) is the product of the maximum cell current (I_{max}) and the voltage (V_{max}) where the power output of the cell is greatest. This point is located at the "knee" of the curve.

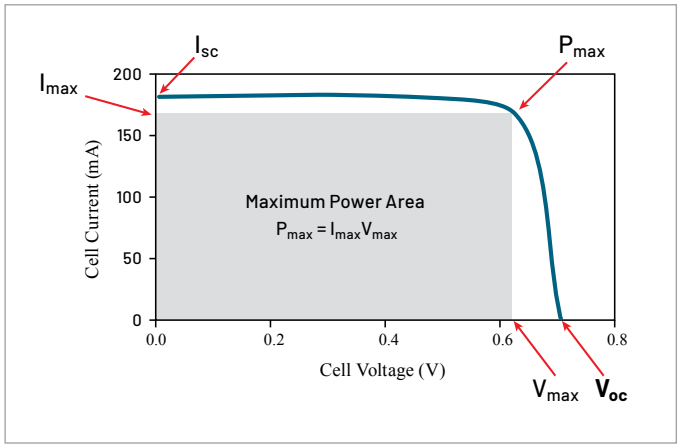


Figure 3. Typical forward bias I-V characteristics of a PV cell

The fill factor (FF) is a measure of how far the I-V characteristics of an actual PV cell differ from those of an ideal cell. The fill factor is defined as:

$$FF = \frac{I_{max}V_{max}}{I_{sc}V_{oc}}$$

where:

I_{max} = the current at the maximum power output (A)

V_{max} = the voltage at the maximum power output (V)

I_{sc} = the short-circuit current (A)

V_{oc} = the open-circuit voltage (V)

As defined, the fill factor is the ratio of the maximum power ($P_{max} = I_{max}V_{max}$) to the product of the short circuit current (I_{sc}) and the open circuit voltage (V_{oc}). The ideal solar cell has a fill factor equal to one (1) but losses from series and shunt resistance decrease the efficiency.

Another important parameter is the conversion efficiency (η), which is defined as the ratio of the maximum power output to the power input to the cell:

$$\eta = \frac{P_{max}}{P_{in}}$$

where:

P_{max} = the maximum power output (W)

P_{in} = the power input to the cell defined as the total radiant energy incident on the surface of the cell (W)

Making Connections to the Solar Cell for I-V Measurements

Figure 4 illustrates a solar cell connected to the 4200A-SCS for I-V measurements. One side of the solar cell is connected to the Force and Sense terminals of SMU1; the other side is connected to the Force and Sense terminals of either SMU2 or the ground unit (GNDU) as shown.

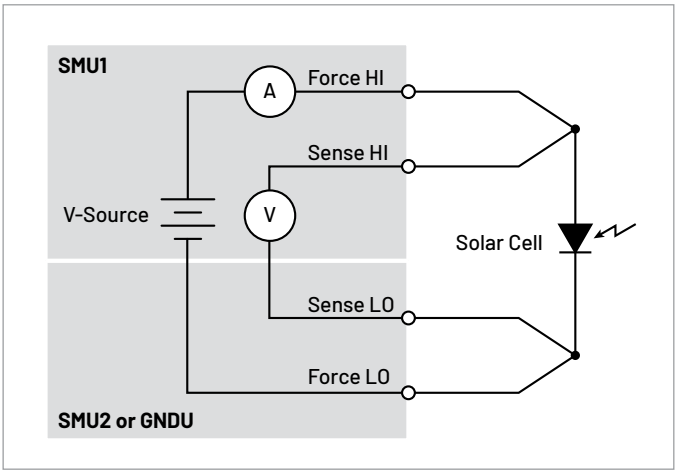


Figure 4. Connection of 4200A-SCS to a solar cell for I-V measurements

Using a four-wire connection eliminates the lead resistance that would otherwise affect this measurement's accuracy. With the four-wire method, a voltage is sourced across the solar cell using one pair of test leads (between Force HI and Force LO), and the voltage drop across the cell is measured across a second set of leads (across Sense HI

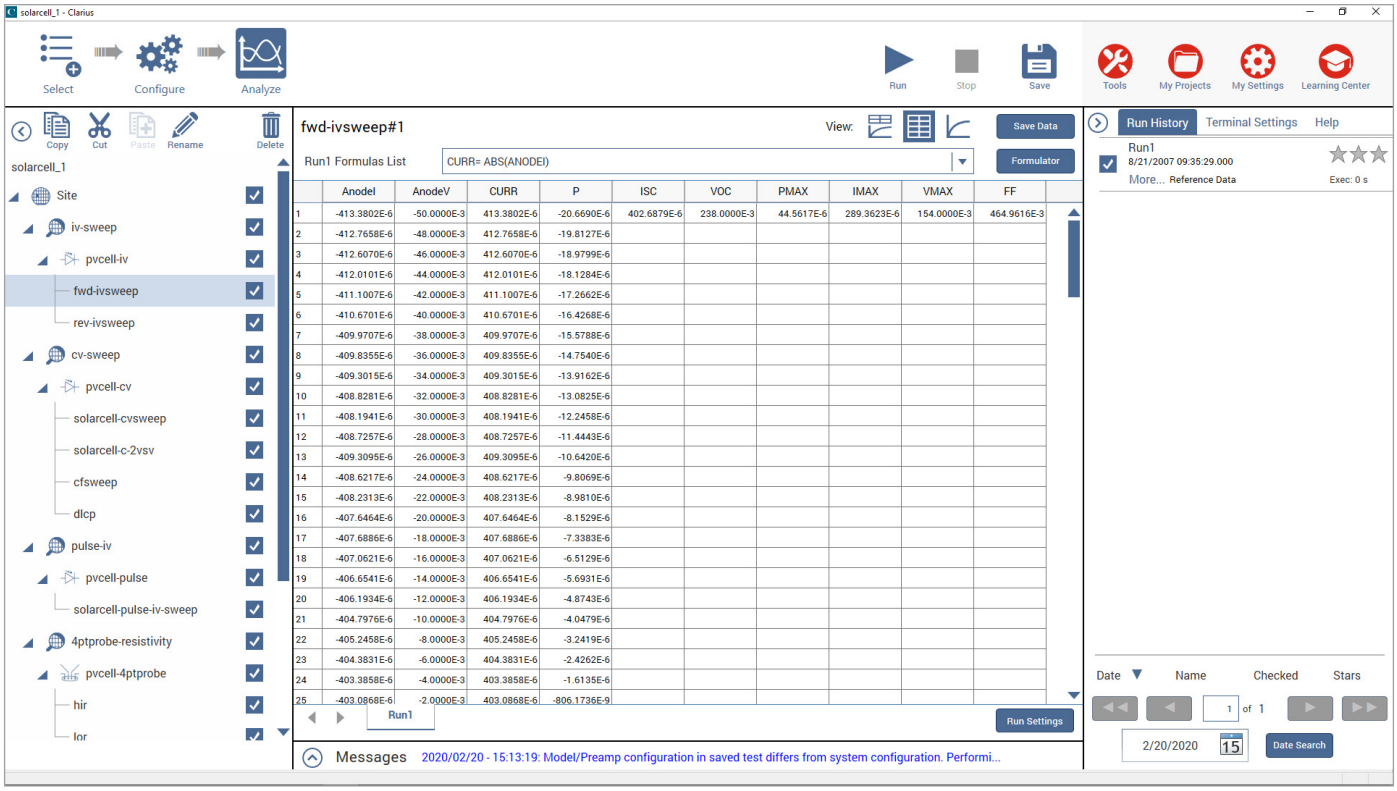


Figure 5. Results of calculated parameters shown in the Sheet in the Analyze pane.

and Sense LO). The sense leads ensure that the voltage developed across the cell is the programmed output value and compensate for the lead resistance.

Forward-Biased I-V Measurements

Forward-biased I-V measurements of the solar cell are made under controlled illumination. The SMU is set up to output a voltage sweep and measure the resulting current. This forward bias sweep can be performed using the *Solar Cell Forward I-V Sweep* or "*fwd-ivsweep*" test, which allows adjusting the sweep voltage to the desired values. As previously illustrated in **Figure 3**, the voltage source is swept from $V_1 = 0$ to $V_2 = V_{OC}$. When the voltage source is 0 ($V_1 = 0$), the current is equal to the source-circuit current ($I_1 = I_{SC}$). When the voltage source is an open circuit ($V_2 = V_{OC}$) then the current is equal to zero ($I_2 = 0$). The parameters, V_{OC} and I_{SC} can be derived easily from the sweep data using the 4200A-SCS's built-in mathematical analysis tool, the Formulator. For convenience, the *Solar Cell Forward I-V Sweep* test has the commonly derived parameters already calculated, so the values automatically appear in the Sheet in the Analyze pane every time the test is executed. **Figure 5** shows some of the derived parameters in the Sheet. These parameters include the short-circuit current (I_{SC}), the open circuit voltage (V_{OC}), the maximum power point (P_{max}), the maximum cell current (I_{max}), the maximum cell voltage (V_{max}), and the fill factor (FF).

The user can easily add other formulas depending on the required parameters that need to be determined.

Using the Formulator, the conversion efficiency (η) can also be calculated if the user knows the power input to the cell and inputs the formula. The current density (J) can also be derived by using the Formulator and inputting the area of the cell.

Figure 6 shows an actual I-V sweep of an illuminated silicon PV cell generated with the 4200A-SCS using the "*fwd-ivsweep*" test. Because the system's SMUs can sink current, the curve passes through the fourth quadrant and allows power to be extracted from the device (I–, V+). If the current output spans several decades as a function of the applied voltage, it may be desirable to generate a semilog plot of I vs. V. The Graph supports an easy transition between displaying data graphically on either a linear or a log scale.

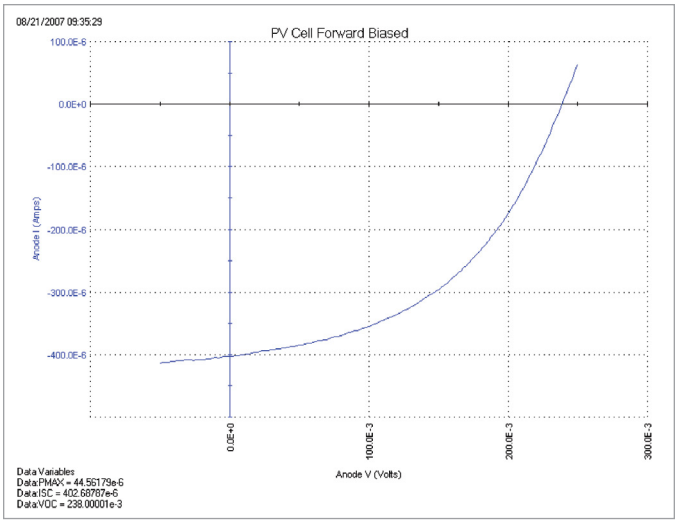


Figure 6. I-V sweep of silicon PV cell generated with the 4200-SMU

If desired, the graph settings functions make it easy to create an inverted version of the graph about the voltage axis. Simply go to the Graph Settings tab, select Axis Properties, select the Y1 Axis tab, and click on the Invert checkbox. The inverse of the graph will appear as shown in **Figure 7**.

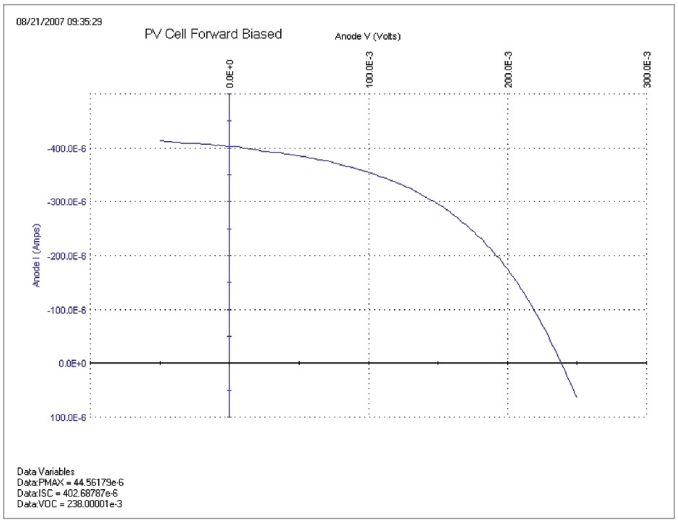


Figure 7. Inversion of the forward-biased I-V curve about the voltage axis

The series resistance (r_s) can be determined from the forward I-V sweep at two or more light intensities. First, make I-V curves at two different intensities (the magnitudes of the intensities are not important). Measure the slope of this curve from the far forward characteristics where the curve becomes linear. The inverse of this slope yields the series resistance:

$$r_s = \frac{\Delta V}{\Delta I}$$

By using additional light intensities, this technique can be extended using multiple points located near the knee of the curves. As illustrated in **Figure 8**, a line is generated from which the series resistance can be calculated from the slope.

When considered as ammeters, one important feature of the SMUs is their very low voltage burden. The voltage burden is the voltage drop across the ammeter during the measurement. Most conventional digital multimeters (DMMs) will have a voltage burden of at least 200 mV at full scale. Given that only millivolts may be sourced to the sample in solar cell testing, this can cause large errors. The 4200A-SCS's SMUs don't produce more than a few hundred microvolts of voltage burden, or voltage drop, in the measurement circuit.

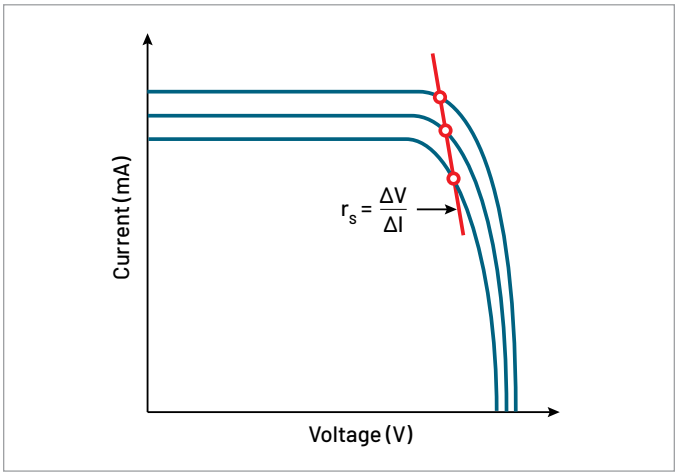


Figure 8. Slope method used to calculate the series resistance

Reverse-Biased I-V Measurements

The leakage current and shunt resistance (r_{sh}) can be derived from the reverse-biased I-V data. Typically, the test is performed in the dark. The voltage is sourced from 0V to a voltage level where the device begins to break down. The resulting current is measured and plotted as a function of the voltage. Depending on the size of the cell, the leakage current can be as small as picoamps. The SMUs have a preamp option that allows making accurate measurements well below a picoamp. When making very sensitive low current measurements (nanoamps or less), use low noise cables and place the device in a shielded enclosure to shield it electrostatically. This conductive shield is connected to the Force LO terminal of the 4200A-SCS. The Force LO terminal connection can be made from the outside shell of the triax connectors, the black binding post on the

ground unit (GNDU), or from the Force LO triax connector on the GNDU.

One method for determining the shunt resistance of the PV cell is from the slope of the reverse-biased I-V curve, as shown in **Figure 9**. From the linear region of this curve, the shunt resistance can be calculated as:

$$r_{sh} = \frac{\Delta V_{Reverse\ Bias}}{\Delta I_{Reverse\ Bias}}$$

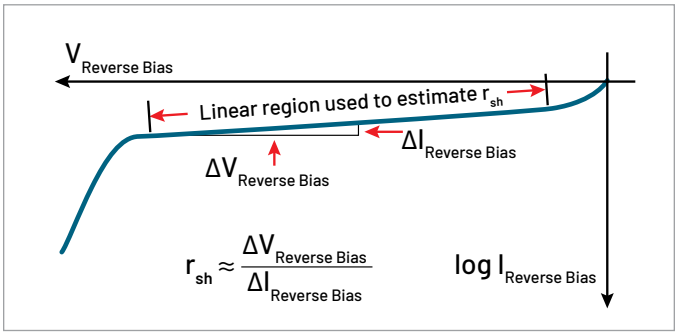


Figure 9. Typical reverse-biased characteristics of a PV cell

Figure 10 shows an actual curve of a reverse-biased solar cell, generated using the *Solar Cell Reverse I-V Sweep* or "*rev-ivsweep*" test. In this semi-log graph, the absolute value of the current is plotted as a function of the reverse-biased voltage that is on an inverted x-axis.

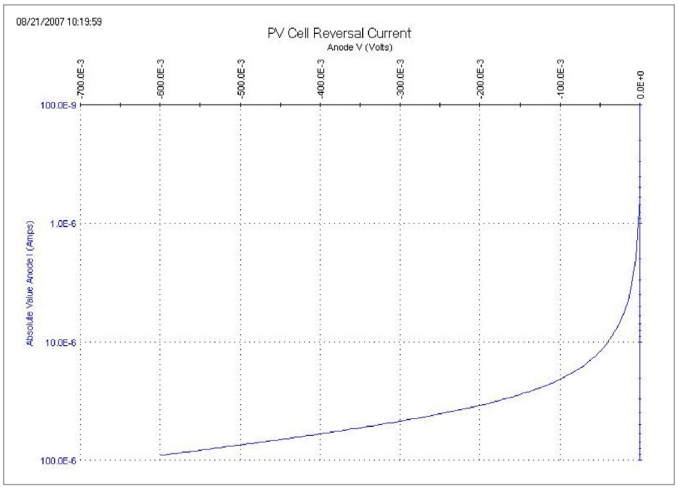


Figure 10. Reverse-biased I-V measurement of silicon solar cell using the SMU

Capacitance Measurements

Capacitance-voltage measurements are useful in deriving particular parameters about PV devices. Depending on the type of solar cell, capacitance-voltage (C-V) measurements can be used to derive parameters such as the doping concentration and the built-in voltage of the junction. A capacitance-frequency (C-f) sweep can be used to provide information on the existence of traps in the depletion region. The 4210-CVU or 4215-CVU, the 4200A-SCS's optional capacitance meter, can measure the capacitance as a function of an applied DC voltage (C-V), a function of frequency (C-f), a function of time (C-t), or a function of the AC voltage. The CVU can also measure conductance and impedance.

To make capacitance measurements, a solar cell is connected to the CVU as shown in **Figure 11**. Like I-V measurements made with the SMU, the capacitance measurements also involve a four-wire connection to compensate for lead resistance. The HPOT/HCUR terminals are connected to the anode and the LPOT/LCUR terminals are connected to the cathode. This connects the high DC voltage source terminal of the CVU to the anode.

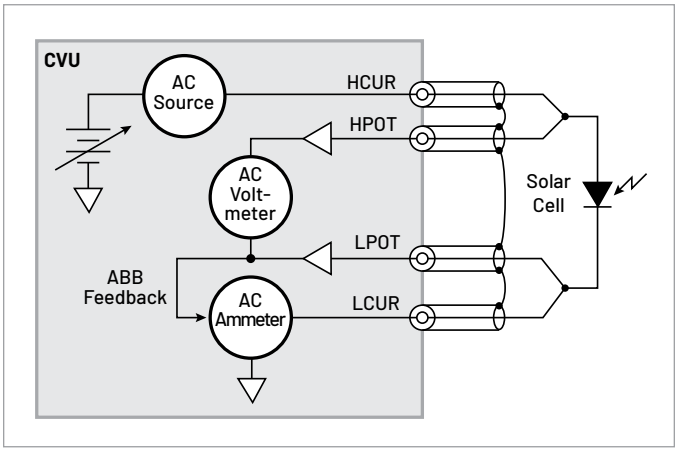


Figure 11. Connecting the solar cell to the CVU capacitance meter

Figure 11 shows the shields of the four coax cables coming from the four terminals of the capacitance meter. The shields from the coax cables must be connected together as close as possible to the solar cell to obtain the highest accuracy because this reduces the effects of the inductance in the measure circuit. This is especially important for capacitance measurements made at higher test frequencies.

Performing an Open and Short Connection Compensation will reduce the effects of cable capacitance on measurement accuracy. This simple procedure is described in the 4200A-SCS Reference Manual.

Given that the capacitance of the cell is directly related to the area of the device, it may be necessary to reduce the area of the cell itself, if possible, to avoid capacitances that may be too high to measure. Also, setting the CVU to measure capacitance at a lower test frequency and/or lower AC drive voltage will allow measuring higher capacitances.

C-V Sweep

C-V measurements can be made either forward-biased or reverse-biased. However, when the cell is forward-biased, the applied DC voltage must be limited; otherwise, the conductance may get too high for the capacitance meter to measure. The maximum DC current cannot be greater than 10 mA; otherwise, the instrument's DC voltage source will go into compliance and the DC voltage output will not be at the desired level.

Figure 12 illustrates a C-V curve of a silicon solar cell generated by the CVU using the *Solar Cell C-V Sweep* or "*solarcell-cvsweep*" test. This test was performed in the dark while the cell was reversed-biased.

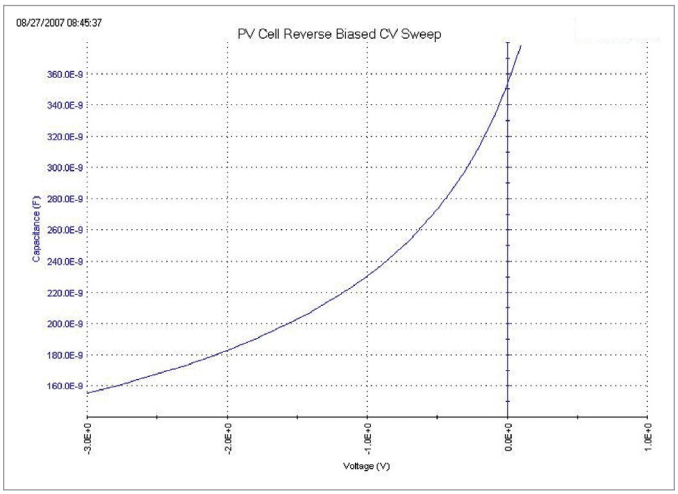


Figure 12. C-V sweep of a silicon solar cell

Rather than plotting dC/dV, it is sometimes desirable to view the data as $1/C^2$ vs. voltage because some parameters are related to the $1/C^2$ data. For example, the doping density (N) can be derived from the slope of this curve because N is related to the capacitance by:

$$N(a) = \frac{2}{qE_S A^2 [d(1/C^2)/dV]}$$

where:

N(a) = the doping density ($1/cm^3$)

q = the electron charge ($1.60219 \times 10^{-19}C$)

E_S = semiconductor permittivity ($1.034 \times 10^{-12}F/cm$ for silicon)

A = area (cm^2)

C = measured capacitance (F)

V = applied DC voltage (V)

The built-in voltage of the cell junction can be derived from the intersection of the $1/C^2$ curve and the horizontal axis. This plot should be a fairly straight line. An actual curve taken with the CVU, generated using the *Solar Cell I/C² C-V Sweep* or "*solarcell-c-2vsv*" test, is shown in **Figure 13**. The Formulator function is used to derive both the doping density (N) and the built-in voltage on the x-axis (x-intercept). The doping density is calculated as a function of voltage in the Formulator and appears in the Sheet in the Analyze pane. The user must input the area of the cell in the Constants area of the Formulator. The built-in voltage source value is derived both in the Formulator and by using a Linear Line Fit option in the Graph settings. Notice the value of the x-intercept appears in the lower left corner of the graph.

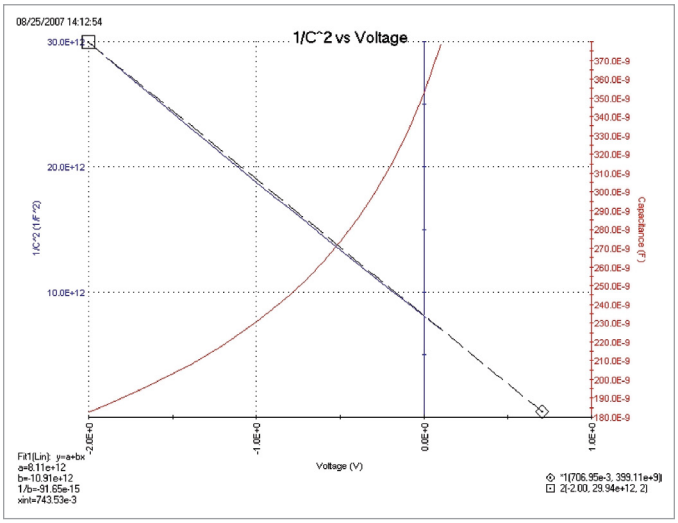


Figure 13. $1/C^2$ vs. voltage of a silicon solar cell

C-f Sweep

The CVU option can also measure capacitance, conductance, or impedance as a function of the test frequency. The range of frequency is from 1 kHz to 10 MHz. The curve in **Figure 14** was generated by using the Solar Cell C-f Sweep or "*cfsweep*" test. Both the range of sweep frequency and the bias voltage can be adjusted. The desired parameters, such as the trap densities, can be extracted from the capacitance vs. frequency data. The measurements can be repeated at various temperatures.

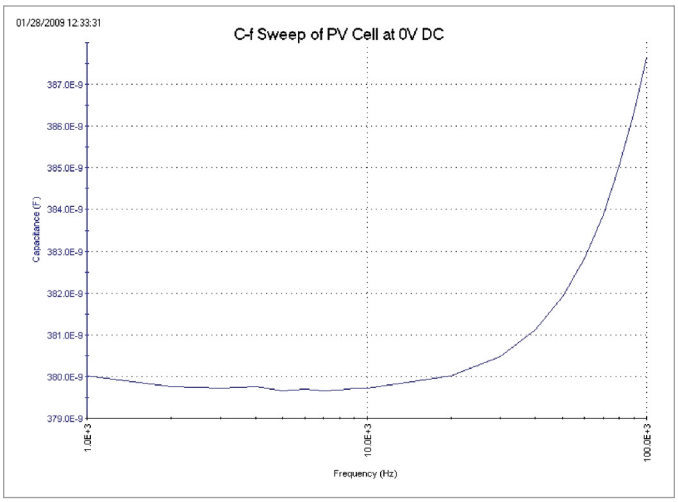


Figure 14. C-f Sweep of Solar Cell

Drive Level Capacitance Profiling (DLCP)

Drive Level Capacitance Profiling (DLCP) is a technique for determining the defect density (N_{DL}) as a function of depth of a photovoltaic cell[1]. During the DLCP measurement, the applied AC voltage (peak-to-peak) is swept and the DC voltage is varied while the capacitance is measured. This is in contrast to the conventional C-V profiling technique, in which the AC rms voltage is fixed and the DC voltage is swept.

In DLCP, the DC voltage is automatically adjusted to keep the total applied voltage (AC + DC) constant while the AC voltage is swept. By maintaining a constant total bias, the exposed charge density (ρ_e) inside the material stays constant up to a fixed location (x_e), which is defined as the distance from the interface where $E_F - E_v = E_e$. This is also in contrast to conventional C-V profiling, the analysis of which assumes that the only charge density changes occur at the end of the depletion region.[1]

Thus, in DLCP, the position (x_e) can be varied by adjusting the DC voltage bias to the sample. This also allows determining the defect density as a function of the distance, or special profiling. The test frequency and temperature of the measurement can also be varied to show a profile that is energy dependent.

Once the measurements are taken, a quadratic fit of the C-V data is related to the impurity density at a given depletion depth as follows for a p-type semiconductor:

$$N_{DL} \equiv \frac{C_0^3}{2q\varepsilon A^2 C_1} = \frac{|\rho_e|}{q} = p + \int_{E_F^0}^{E_V + E_e} g(E, x_e)\,dE$$

where:

N_{DL} = defect density (cm^{-3})

C_1, C_0 = coefficients of quadratic fit of C-V data

q = electron charge (1.60×10^{-19}C)

ε = permittivity (F/cm)

A = area of solar cell (cm^2)

ρ_e = charge density (C/cm^3)

p = hole density (cm^{-3})

x_e = distance from interface where $E_F - E_v = E_e$

The coefficients C_0 and C_1 are determined via a full least-squares best fit of the data to a quadratic equation:

$$dQ/dV = C_2(dV)^2 + C_1*(dV) + C_0$$

However, only the C_0 and C_1 coefficients are used in the analysis.

The *Solar Cell DLCP* or "*dlcp*" test allows making C-V measurements for drive level capacitance profiling. During these measurements, the total applied voltage remains constant as the DC voltage bias is automatically adjusted as the AC voltage drive level amplitude varies. The AC amplitude can be adjusted from 10 mVrms to 100 mVrms (14.14 mV to 141.4 mVp-p). The range of frequency can also be set from 1 kHz to 10 MHz. The capacitance is measured as the AC voltage is sweeping.

1 J. T. Heath, J. D. Cohen, W. N. Shafarman, "Bulk and metastable defects in CuIn1–xGaxSe2 thin films using drive-level capacitance profiling", Journal of Applied Physics, vol. 95, no. 3, p. 1000, 2004

Table 2 lists the input parameters used in the test, the allowed range of input values, and descriptions. This test was created from the DLCP User Library and the ACSweep User Module. The user inputs the total applied voltage (VmaxTotal), the AC start, stop, and step voltages (VacppStart, VacppStop, and VacppStep), the time between voltage steps (SweepDelay), the test frequency (Frequency), the measurement speed (Speed), the measurement range (CVRange), and offset compensation (OpenComp, ShortComp, LoadComp, and LoadVal).

Table 2. Adjustable parameters for the *dlcp* test (ACSweep User Module)

Parameter	Range	Description
VmaxTotal	-10 to 10 volts	Applied DC Volts and ½ AC Volts p-p
VacppStart	.01414 to .1414	Start Vac p-p
VacppStop	.02828 to .1414	Stop Vac p-p
VacppStep	.0007070 to .1414	Step Vac p-p
SweepDelay	0 to 100	Sweep delay time in seconds
Frequency	1E+3 to 10E+6	Test Frequency in Hertz
Speed	0, 1, 2	0=Fast, 1=Normal, 2=Quiet
CVRange	0, 1E-6, 30E-6, 1E-3	0=autorange, 1 µA, 30 µA, 1 mA
OpenComp	1, 0	Enables/disables open compensation for CVU
ShortComp	1, 0	Enables/disables short compensation for CVU
LoadComp	1, 0	Enables/disables load compensation for CVU
LoadVal	1 to 1E+9	Load value

Once the test is executed, the capacitance, AC voltage, DC voltage, time stamp, frequency, and the defect density (N_{DL}) are determined and their values are listed in the Sheet. The defect density is calculated in the Formulator using a quadratic line fit of the C-V data. The coefficients (C_0 and C_1) of the quadratic equation are also listed in the Sheet. The user inputs the area and permittivity of the solar cell to be tested into the Constants/Values/Units area of the Formulator.

Figure 15 shows the measurement results in the graph of capacitance vs. AC voltage p-p. Notice the coefficients of the derived quadratic line fit and the defect density are displayed on the graph.

The capacitance measurements can be repeated at various applied total voltages in order to vary the position of x_e. The energy (E_e) can be varied by changing the test frequency (1 kHz to 10 MHz) or the temperature. To change the temperature of the measurement, the user can add an Action to the project to control a temperature controller via the 4200A-SCS's GPIB interface. The 4200A-SCS is provided with user libraries for operating the Temptronics, Lakeshore, and Triotek temperature controllers.

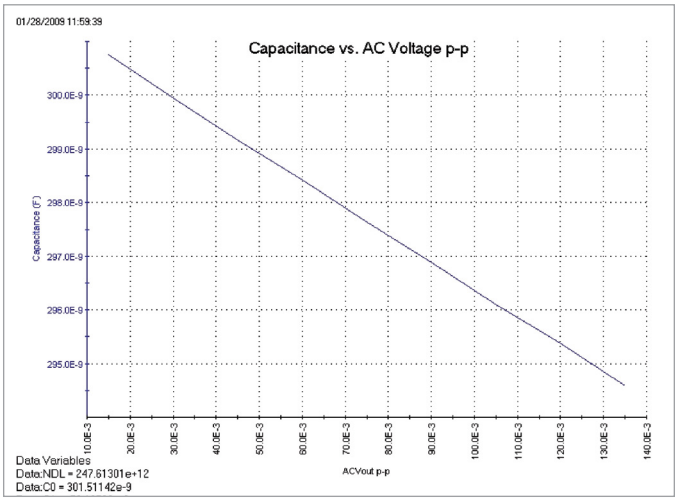


Figure 15. Capacitance vs. AC voltage p-p of a solar cell

Pulsed I-V Measurements

Pulsed I-V measurements can be useful for studying parameters of solar cells. In particular, pulsed I-V measurements have been used to determine the conversion efficiency, minimum carrier lifetime, and the effects of cell capacitance. The 4225-PMU, the 4200A-SCS's optional Ultra-Fast I-V Module, can output pulsed voltage and measure current, and can capture ultra-high-speed current or voltage waveforms in the time domain. In addition to sourcing a pulsed voltage, the PMU can sink current so it can measure a solar cell's current output.

To make pulsed I-V measurements on a solar cell, the 4225-PMU is connected to the cell as shown in **Figure 16**. Each PMU has two channels so the solar cell can be connected using either one or two channels. In the one-channel case shown, one end of the cell is connected to the HI terminal of PMU CH1 and the other side of the cell is connected to the shield of the coax cable, which is the LO terminal of the PMU.

Unlike the DC I-V and C-V measurements, the 4225-PMU uses a two-wire technique. The Short Compensation feature can be used to "zero out" the voltage drops due to the cables so that a 4-wire measurement technique isn't necessary.

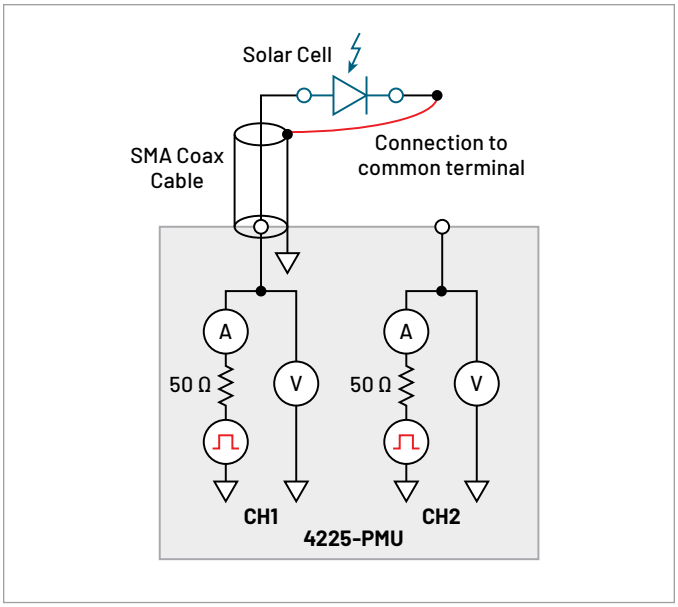


Figure 16. Connecting the solar cell to the 4225-PMU Ultra-Fast I-V Module

Because solar cells are fairly capacitive, it is important to ensure the pulse width is long enough for the pulsed I-V sweep. The waveform capture mode should be used to verify the pulse width prior to generating the pulsed I-V sweep. The waveform capture mode enables a time-based current and/or voltage measurement that is typically the capture of a pulsed waveform. This can be used to perform a dynamic test on the cell or used as a diagnostic tool for choosing the appropriate pulse settings in the pulsed I-V mode. Given that larger solar cells have larger capacitances, it may be necessary to reduce the area of the cell itself to avoid a long settling time in the measurement.

The results of generating a pulsed I-V measurement sweep on a silicon solar cell are shown in **Figure 17**. Note that the current is in the fourth quadrant of the curve. This indicates that the PMU is sinking current; in other words, the current is flowing out of the solar cell and into the PMU.

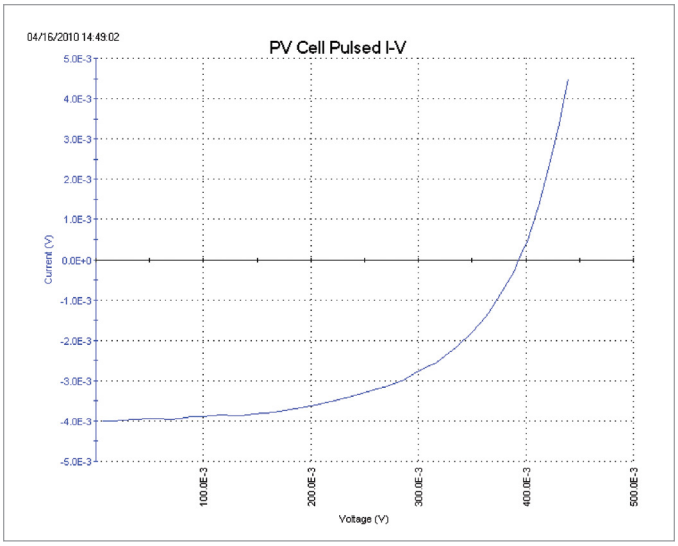


Figure 17. Pulsed I-V measurement on solar cell using 4225-PMU

Resistivity and Hall Voltage Measurements

Determining the resistivity of a solar cell material is a common electrical measurement given that the magnitude of the resistivity directly affects the cell's performance. Resistivity measurements of semiconductor materials are usually performed using a four-terminal technique. Using four probes eliminates errors due to the probe resistance, spreading resistance under each probe, and the contact resistance between each metal contact and the semiconductor material. Two common techniques for determining the resistivity of a solar cell material are the four-point collinear probe method and the van der Pauw method. The *SolarCell* project contains several tests for making both types of measurements, which are described in the next few paragraphs.However, the Test Library also contains individual tests for making both van der Pauw and Hall coefficient measurements. These tests can be found by typing in the name of these tests in the search bar in the Select view: vdp-surface-resistivity, vdp-volume-resistsivity, or hall-coefficient. These tests are described in the Keithley application note, "Making van der Pauw Resistivity and Hall Voltage Measurements Using the 4200A-SCS Parameter Analyzer".

Four-Point Collinear Probe Measurement Method

The four-point collinear probe technique involves bringing four equally spaced probes in contact with a material of unknown resistance. The probe array is placed in the center of the material as shown in **Figure 18**. The two outer probes are used to source current and the two inner probes are used to measure the resulting voltage difference across the surface of the material.

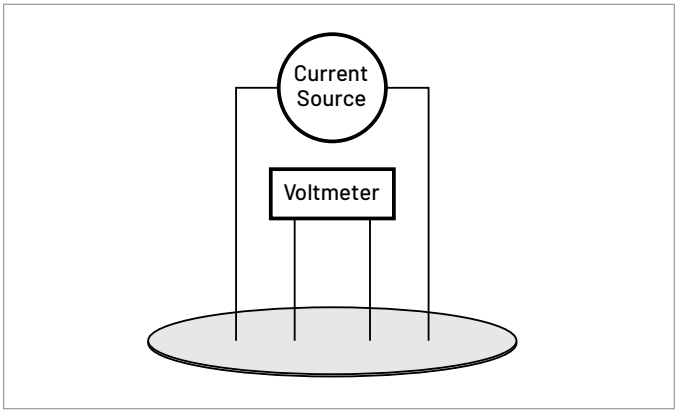


Figure 18. Four-point collinear probe resistivity configuration

From the sourced current and the measured voltage, the surface or sheet resistivity is calculated by:

$$\sigma = \frac{\pi}{\ln 2} \times \frac{V}{I}$$

where:

σ = surface resistivity (Ω/□)

V = the measured voltage (V)

I = the source current (A)

Note that the units for sheet resistivity are expressed as ohms per square (Ω/□) in order to distinguish this number from the measured resistance (V/I), which is simply expressed in ohms. Correction factors to the resistivity calculation may be required for extremely thin or thick samples or if the diameter of the sample is small relative to the probe spacing.

If the thickness of the sample is known, the volume resistivity can be calculated as follows:

$$\rho = \frac{\pi}{\ln 2} \times \frac{V}{I} \times t \times k$$

where:

ρ = volume resistivity (Ω-cm)

t = the sample thickness (cm)

k = a correction factor* based on the ratio of the probe spacing to wafer diameter and on the ratio of wafer thickness to probe spacing

* The correction factors can be found in a standard four-point probe resistivity test procedure such as *Semi MF84: Standard Test Method for Measuring Resistivity of Silicon Wafers With an In-Line Four-Point Probe.* This standard was originally published by ASTM International as ASTM F 84.

Using the Four-Point Probe Tests

The *Solar Cell High Resistance* or "*hir*" test or the *Solar Cell Low Resistance* or "*lor*" tests are both used for making four-point collinear probe measurements. The "*hir*" test can be used for materials over a wide resistance range, ~1 mΩ to 1 TΩ. The 4200-PA preamps are required for making high resistance measurements (>1MΩ). The "*lor*" test is intended for measurements of lower resistance materials (~1 mΩ–1 kΩ).

A screenshot of the "*hir*" test for measuring four-probe resistivity is shown in **Figure 19**.

The *Solar Cell High Resistance* test (*hir*) uses either three or four SMUs to make the resistivity measurements. One SMU (SMU1) and the ground unit (GNDU) are used to source current between the outer two probes. Two other SMUs (SMU2 and SMU3) are used to measure the voltage drop between the two inner probes. The Force HI terminal of each SMU is connected to each of the four probes. The SMU designation for this configuration is shown in **Figure 20**.

In the Formulator, the voltage difference between SMU2 and SMU3 is calculated and the resistance and sheet resistivity are derived from the voltage difference. The results appear in the Sheet in the Analyze pane of the test.

When making high resistance measurements, potential sources of error need to be considered in order to make optimal measurements. Use a probe head that has a level of insulation resistance between the probes that is sufficiently higher than the resistance of the material to be measured. This will help prevent errors due to leakage current through the probe head. Ensure that the measurement circuit is electrostatically shielded by enclosing the circuit in a metal shield. The shield is connected to the LO terminal of the 4200A. The LO terminal is located on the GNDU or on the outside shell of the triax connectors. Use triax cables to produce a guarded measurement circuit. This will prevent errors due to leakage current and significantly reduce the test time. Finally, the 4200-PA preamp option is required to

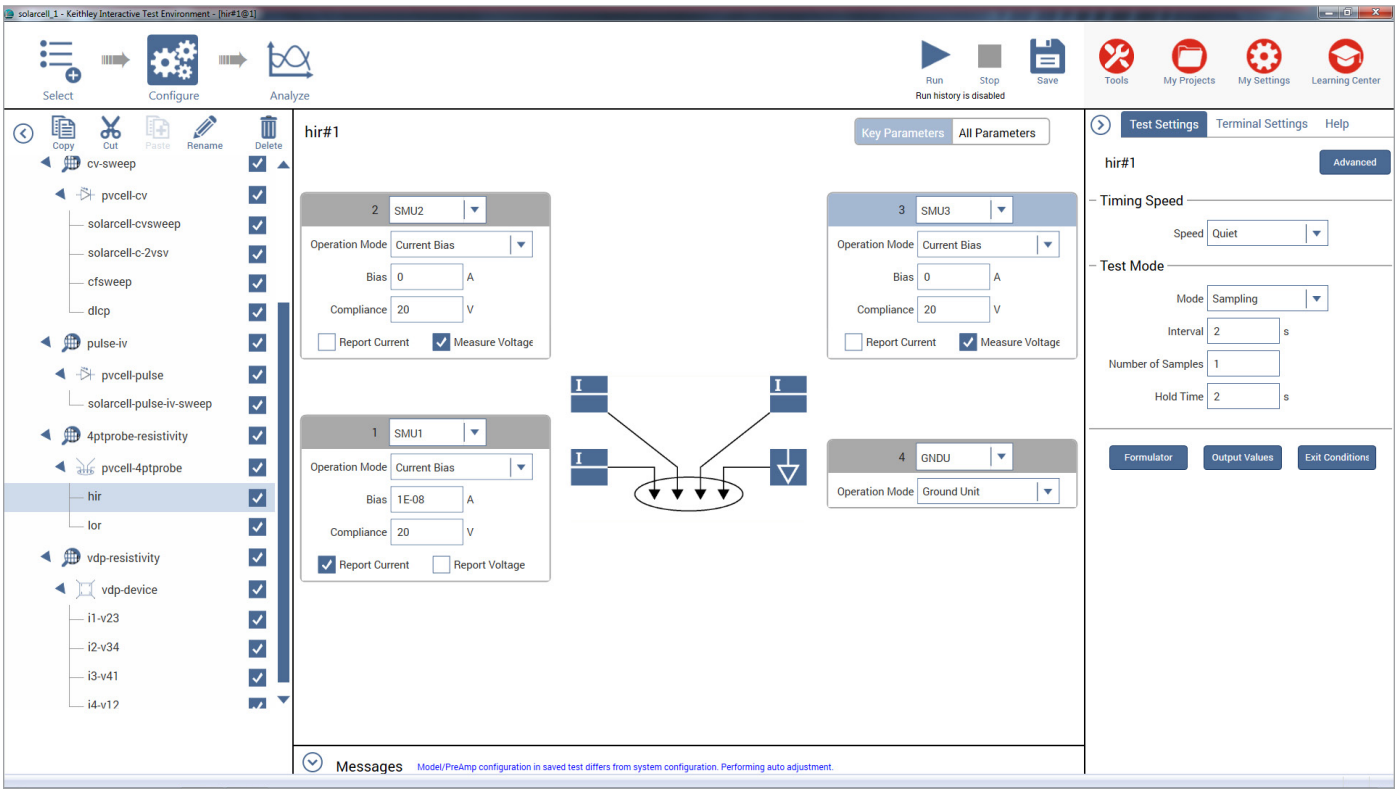


Figure 19. "hir" test module for measuring resistivity

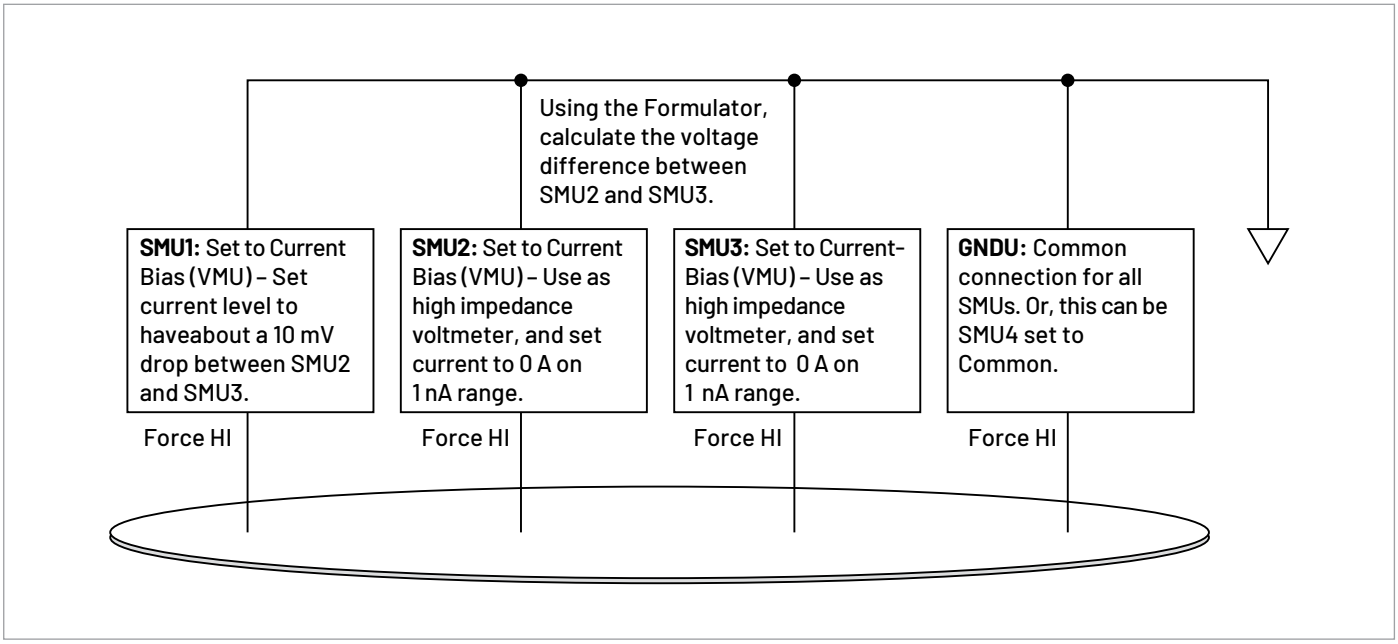


Figure 20. SMU designation for four-point collinear probe measurements

source very small currents (nanoamp and picoamp range) and to provide high input impedance (>1E16 ohms) to avoid loading errors when measuring the voltage difference.

The *Solar Cell Low Resistance* (*Ior*) test is only used for lower resistance materials and requires only one or two SMUs. In this case, the Force and Sense terminals of the SMUs are connected to the four-point probe as shown in **Figure 20**.

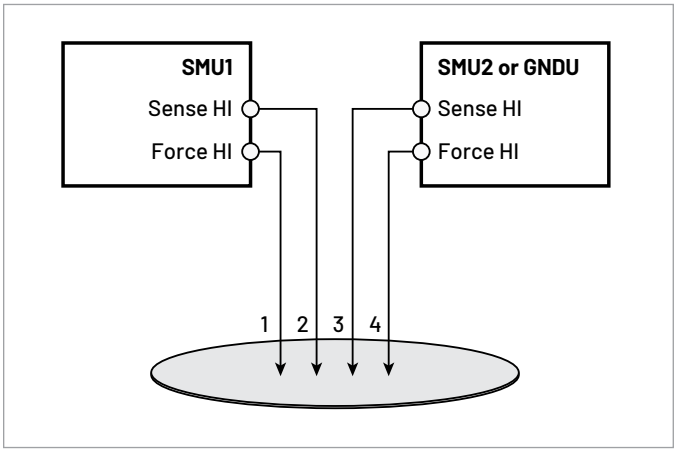


Figure 21. Connecting two SMUs for four-point probe measurements

In the configuration shown in **Figure 21**, the Force HI terminal SMU1 sources the current through Probe 1. The voltage difference between Probes 2 and 3 is measured through the Sense terminals of the two SMUs.

To compensate for thermoelectric offset voltages, two voltage measurements are made with currents of opposite polarity. The two measurements are combined and averaged to cancel the thermoelectric EMFs. The *Solar Cell Low Resistance* (*Ior*) test performs this offset correction automatically by sourcing the two current values in the List Sweep and then mathematically correcting for the offsets in the Formulator. The corrected resistance and sheet resistivity are displayed in the Sheet.

Measuring Resistivity with the van der Pauw Method

The van der Pauw (vdp) technique for measuring resistivity uses four isolated contacts on the boundary of a flat, arbitrarily shaped sample. The resistivity is derived from eight measurements made around the sample as shown in **Figure 22**.

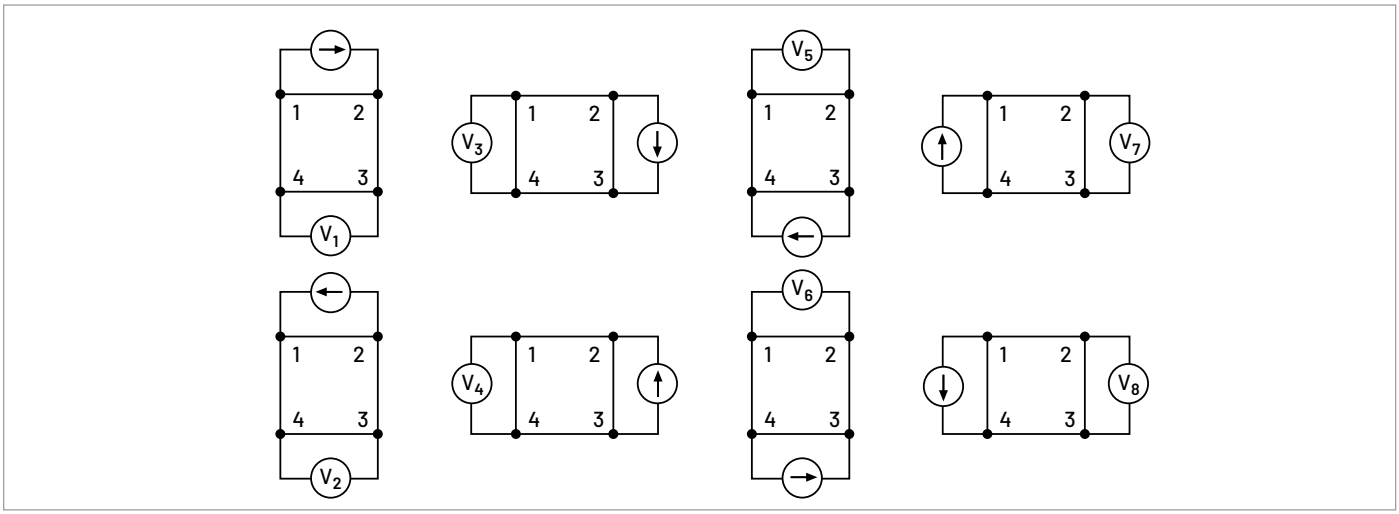


Figure 22. van der Pauw resistivity measurement conventions

Once all the voltage measurements have been taken, two values of resistivity, ρ_A and ρ_B, are derived as follows:

$$\rho_A = \frac{p}{\ln^2} f_A t_s \frac{(V_2 + V_4 - V_1 - V_3)}{4I}$$

$$\rho_B = \frac{p}{\ln^2} f_B t_s \frac{(V_6 + V_8 - V_5 - V_7)}{4I}$$

where:

ρ_A and ρ_B are volume resistivities in ohm-cm;

t_s is the sample thickness in cm;

V_1–V_8 represent the voltages measured by the voltmeter;

I is the current through the sample in amperes;

f_A and f_B are geometrical factors based on sample symmetry, and are related to the two resistance ratios Q_A and Q_B as shown in the following equations ($f_A = f_B = 1$ for perfect symmetry).

Q_A and Q_B are calculated using the measured voltages as follows:

$$Q_A = \frac{V_2 - V_1}{V_4 - V_3}$$

$$Q_B = \frac{V_6 - V_5}{V_8 - V_7}$$

Also, Q and f are related as follows:

$$\frac{Q-1}{Q+1} = \frac{f}{0.693} \operatorname{arc\,cosh}\left(\frac{e^{0.693/f}}{2}\right)$$

A plot of this function is shown in **Figure 23**. The value of "f" can be found from this plot once Q has been calculated.

Once ρ_A and ρ_B are known, the average resistivity (ρ_{AVG}) can be determined as follows:

$$\rho_{AVG} = \frac{\rho_A + \rho_B}{2}$$

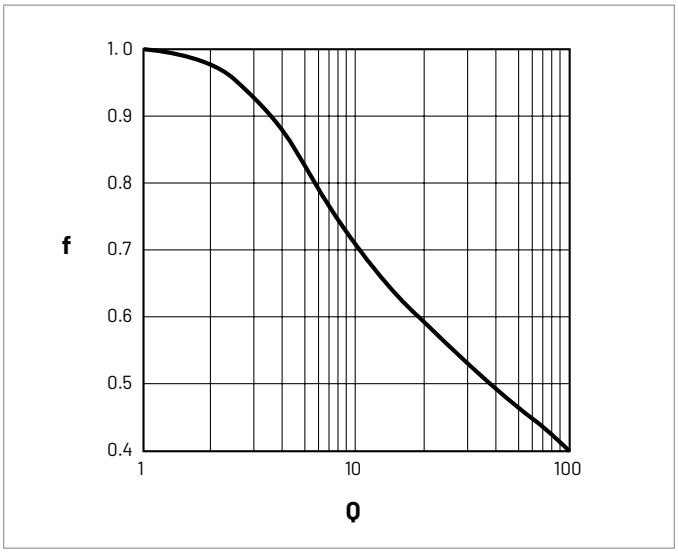


Figure 23. Plot of f vs. Q

Using the *vdp-resistivity* subsite and vdp method tests

To automate the vdp resistivity measurements, the *solarcell* project has a *vdp-resistivity* subsite with four tests: "*i1-v23*", "*i2-v34*", "*i3-v41*", and "*i4-v12*." A screenshot of the test is shown in **Figure 24**.

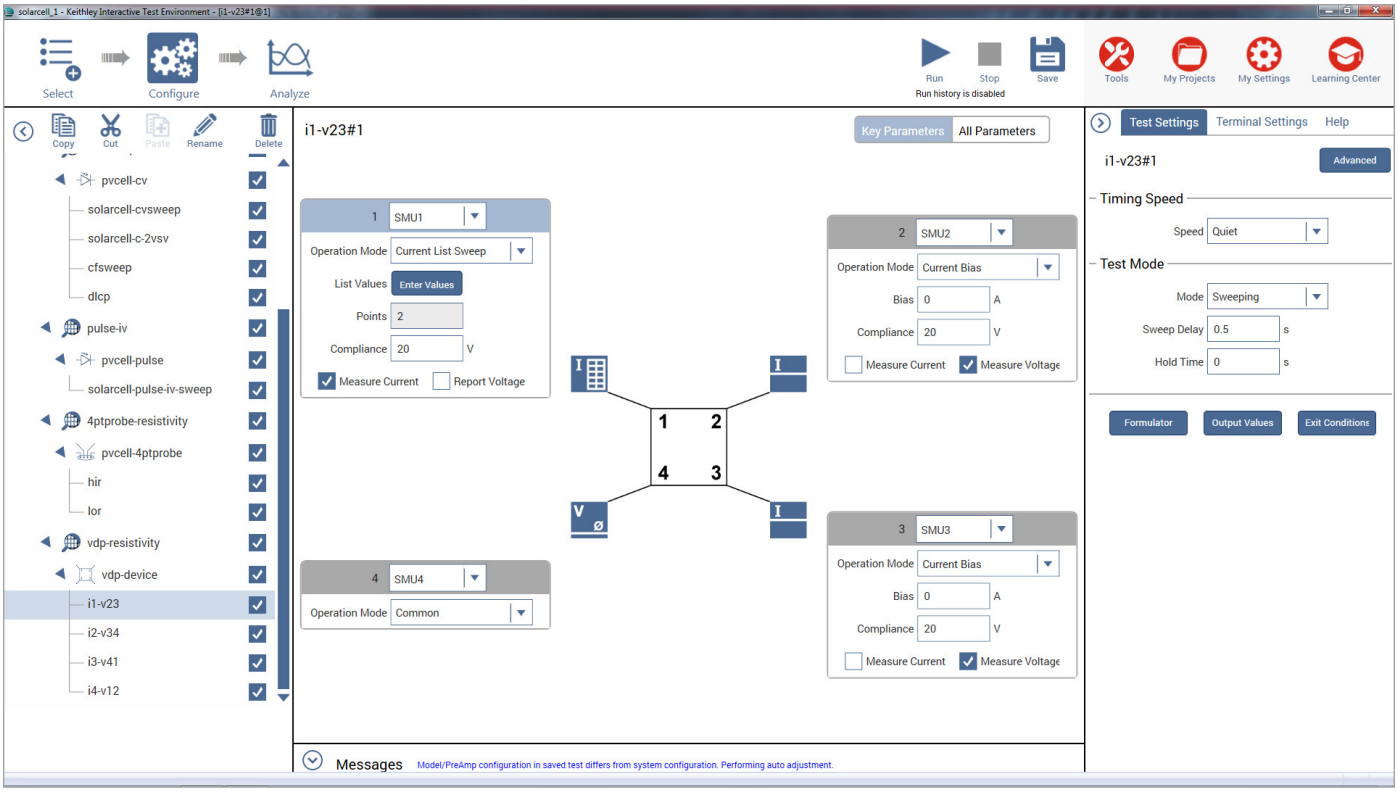


Figure 24. Screenshot of van der Pauw test

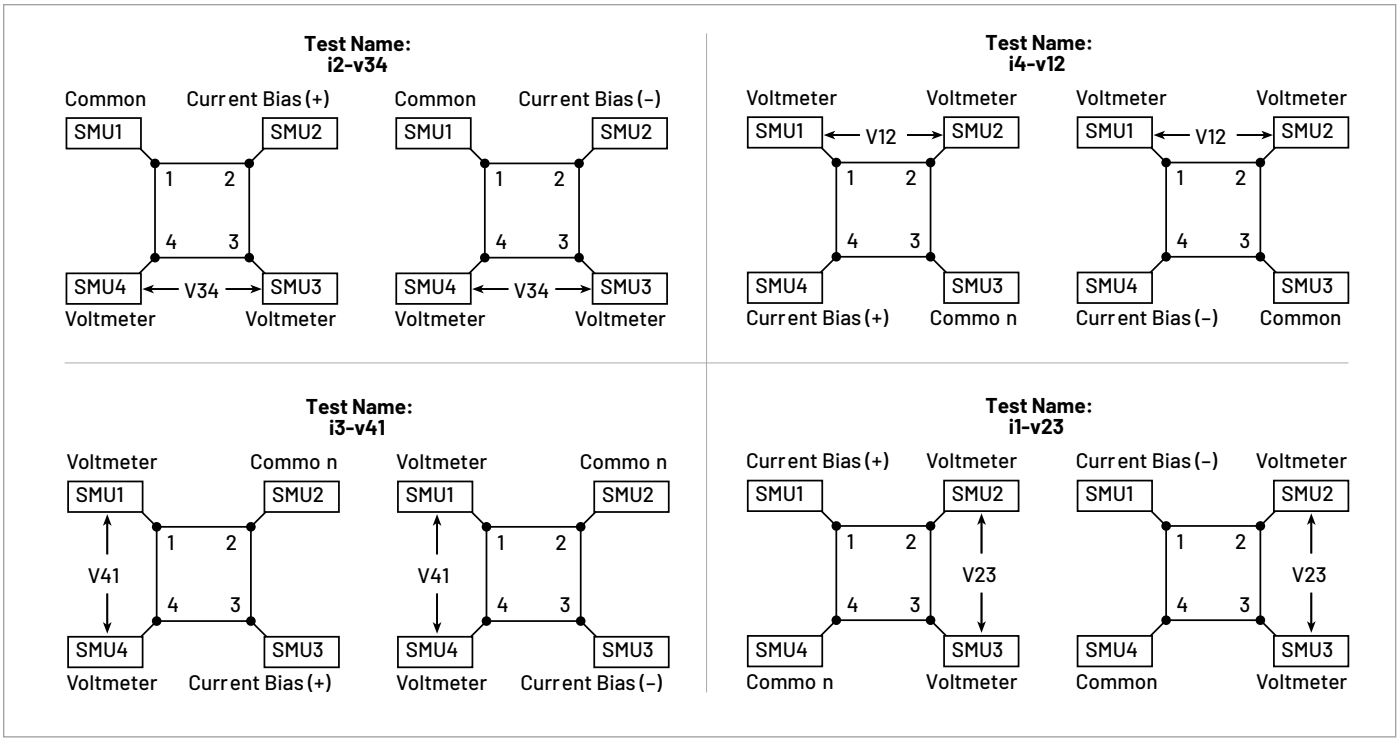


Figure 25. SMU configurations for van der Pauw measurements

Each terminal of the sample is connected to the Force HI terminal of an SMU, so a 4200A-SCS with four SMUs is required. The four SMUs are configured differently in each of the four tests – one SMU supplies the test current, two are configured as voltmeters, and one is set to common. This measurement setup is repeated around the sample, with each of the four SMUs serving a different function in each of the four tests. A diagram of the function of each SMU in each test is shown in **Figure 25**.

Adjusting the Test Parameters

Before executing the test, some of the test parameters must be adjusted based on the sample to be tested. In particular, it's necessary to specify the source current, the settling time, and the thickness of the material.

Input Source Current: Before running the project, input the current source values based on the expected sample resistance. Adjust the current so that the voltage difference will not exceed approximately 25 mV to keep the sample in thermal equilibrium. In each of the four tests, enter both polarities of the test current. The same magnitude must be used for each test.

Input the Settling Time: For high resistance samples, it will be necessary to determine the settling time of the measurements. This can be accomplished by creating a test that sources current into two terminals of the samples and measures the voltage drop on the adjacent two terminals. The settling time can be determined by taking multiple voltage readings and then graphing the voltage difference as a function of time.

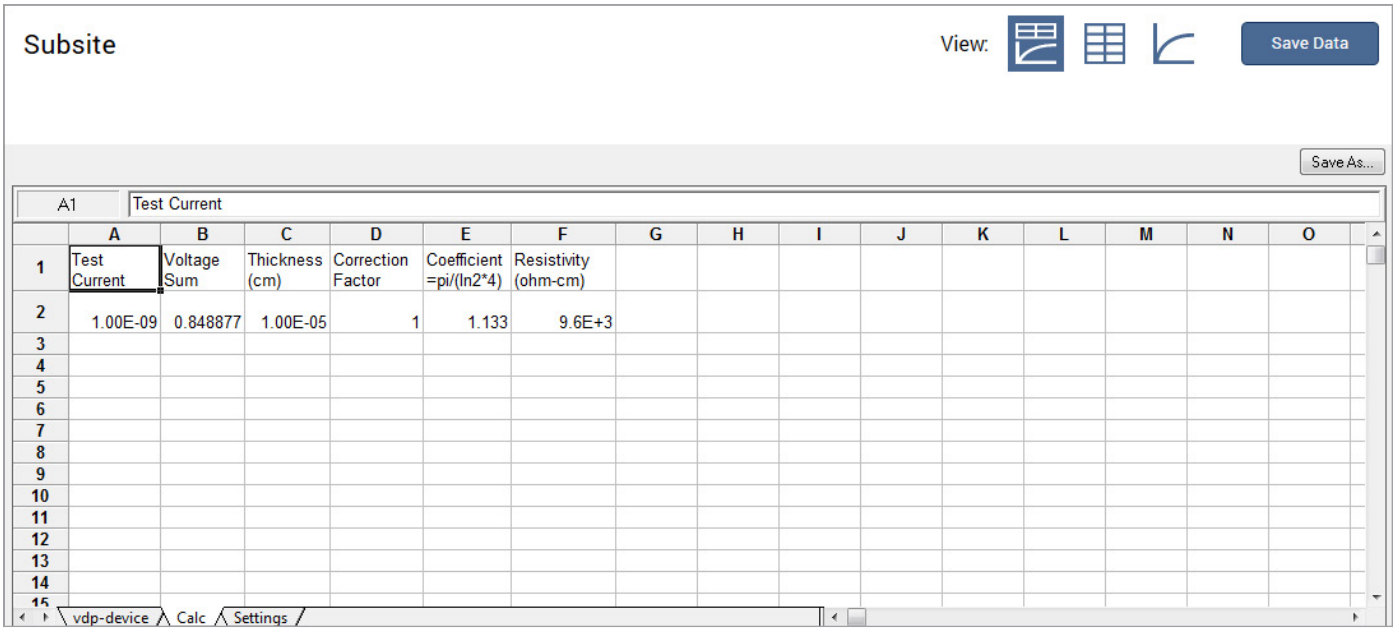
This settling time test can be generated by copying and then modifying one of the existing vdp tests. Switch the source function from the sweep mode to the sampling mode. Then, in the Test Settings pane, take a few hundred or so readings with a delay time of one second. Make sure that the "Report Timestamps" box is selected. After the readings are done, plot the voltage difference vs. time on the graph. The settling time is determined by observing the graph and finding the time when the reading is within the desired percentage of the final value.

Input the Thickness of the Sample: Enter the thickness of the sample into the Calc sheet at the subsite level. Select the subsite vdp_resistivity. Go to the Subsite Data vdp-device tab. It contains the output values of the voltage differences and test current. From the Calc tab, the thickness can be adjusted. The default thickness is 1 cm.

Input Correction Factor: The resistivity formula found in the Calc sheet at the subsite level also allows inputting a correction factor, if necessary. The resistivity is multiplied by this number, which may be based on the geometry or uniformity of the sample. By default, the correction factor is 1.

Running the Project

The van der Pauw resistivity measurements must be run at the subsite level. Make sure that all four checkboxes to the right of the vdp tests (*"i1-v23," "i2-v34," "i3-v41,"* and *"i4-v12"*) are selected and then select *vdp_resistivity*. Execute the project by using the Run button. Each time the test is run, the subsite data is updated. The voltage differences from each of the four tests will appear in the Subsite Data vdp-device Sheet tab. The resistivity will appear in the Subsite Data Calc sheet as shown in **Figure 26**.



	A	B	C	D	E	F
1	Test Current	Voltage Sum	Thickness (cm)	Correction Factor	Coefficient =pi/(ln2*4)	Resistivity (ohm-cm)
2	1.00E-09	0.848877	1.00E-05	1	1.133	9.6E+3

Figure 26. vdp resistivity calculation

Hall Voltage Measurements

Hall effect measurements are important to semiconductor material characterization because the conductivity type, carrier density, and Hall mobility can be derived from the Hall voltage. With an applied magnetic field, the Hall voltage can be measured using the configuration shown in **Figure 27**.

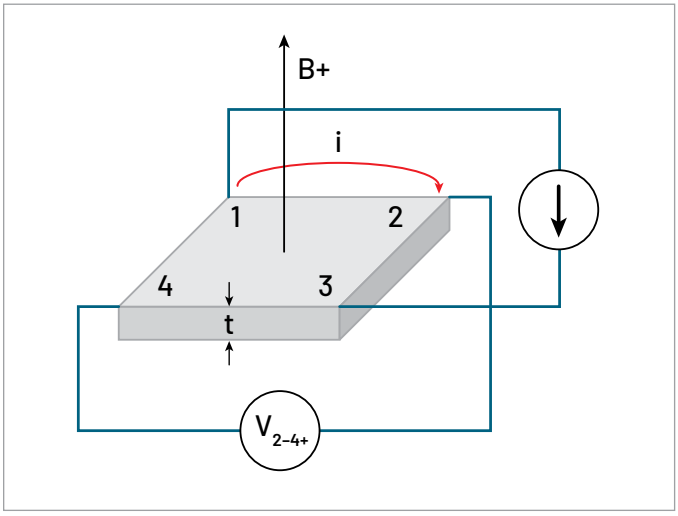


Figure 27. Hall voltage measurement

With a positive magnetic field (B+), apply a current between Terminals 1 and 3 of the sample, and measure the voltage drop (V_{2-4+}) between Terminals 2 and 4. Reverse the current and measure the voltage drop (V_{4-2+}). Next, apply current between Terminals 2 and 4, and measure the voltage drop (V_{1-3+}) between Terminals 1 and 3. Reverse the current and measure the voltage drop ($V_{3-1}+$) again.

Reverse the magnetic field (B–) and repeat the procedure, measuring the four voltages: (V_{2-4-}), (V_{4-2-}), (V_{1-3-}), and (V_{3-1-}). **Table 3** summarizes the Hall voltage measurements.

Table 3. Summary of Hall Voltage Measurements

Voltage Designation	Magnetic Flux	Current Forced Between Terminals	Voltage Measured Between Terminals
V2–4+	B+	1–3	2–4
V4–2+	B+	3–1	4–2
V1–3+	B+	2–4	1–3
V3–1+	B+	4–2	3–1
V2–4–	B–	1–3	2–4
V4–2–	B–	3–1	4–2
V1–3–	B–	2–4	1–3
V3–1–	B–	4–2	3–1

From the eight Hall voltage measurements, the average Hall coefficient can be calculated as follows:

$$R_{HC} = \frac{t(V_{4-2+} - V_{2-4+} + V_{2-4-} - V_{4-2-})}{4BI}$$

$$R_{HD} = \frac{t(V_{3-1+} - V_{1-3+} + V_{1-3-} - V_{3-1-})}{4BI}$$

where:

R_{HC} and R_{HD} are Hall coefficients in cm^3/C;

t is the sample thickness in cm;

V represents the voltages measured in V;

I is the current through the sample in A;

B is the magnetic flux in Vs/cm^2

Once R_{HC} and R_{HD} have been calculated, the average Hall coefficient (R_{HAVG}) can be determined as follows:

$$R_{HAVG} = \frac{R_{HC} + R_{HD}}{2}$$

From the resistivity (ρ_{AVG}) and the Hall coefficient (R_H), the Hall mobility (μ_H) can be calculated:

$$\mu_H = \frac{|R_H|}{\rho_{AVG}}$$

Using the 4200A-SCS to Measure the Hall Voltage

The *SolarCell* project does not include a specific test to measure the Hall voltage; however, four tests can be added to the subsite for determining the Hall coefficient and mobility. Given that the configuration for the Hall measurements is very similar to the van der Pauw resistivity measurements, the vdp tests can be copied and modified for making the Hall voltage measurements. The modifications involve changing the functions of the SMUs. **Figure 28** illustrates how to configure the four SMUs in the tests to measure the Hall voltage. Use the Output Value checkboxes on the Test Settings pane of each test to return the Hall voltages to the subsite-level Calc sheet.

A custom test must be added to control the magnet. For a GPIB-controlled electromagnet, users can write a user module using KULT (the Keithley User Library Tool) to control the magnitude and polarity of the electromagnet. The code can be opened up in a custom test within the project. Information on writing code using KULT is provided in the 4200A-SCS Reference Manual.

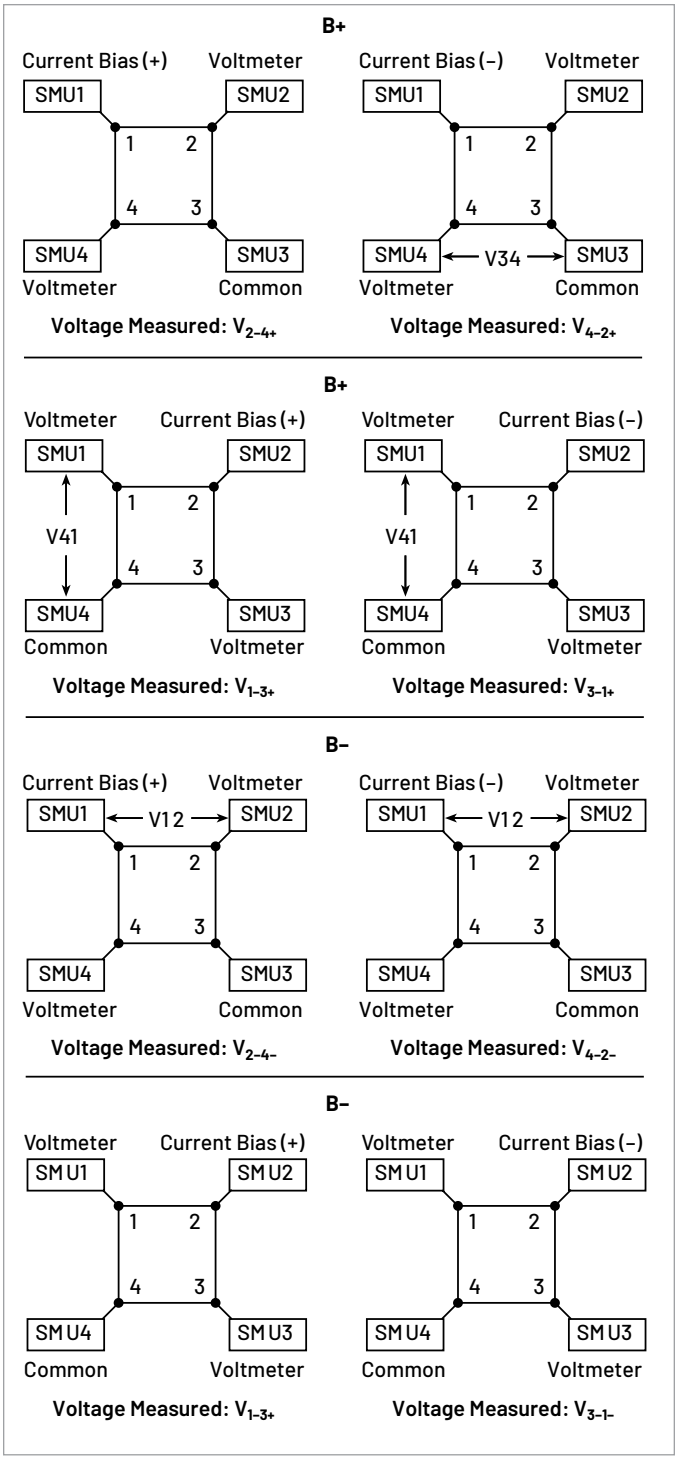


Figure 28. SMU configurations for Hall voltage measurements

If a permanent magnet is used, an Action from the Actions Library can be used to create a dialog box Project Prompt that will stop the test sequence in the project tree and instruct the user to change the polarity of the magnetic field applied to the sample. A Project Prompt is a dialog window that pauses the project test sequence and prompts the user to perform some action. See the 4200A-SCS Reference Manual for a description of how to use Dialog Box Actions.

Finally, the Hall coefficient and mobility can be derived in the subsite-level Calc sheet. These math functions can be added to the other equations for determining resistivity.

Instead of using four separate tests and the subsite-level Calc Sheet for making Hall voltage measurements, add the hall-coefficient test from the Library, which combines all the measurements and parameter extractions into one test.

Conclusion

Measuring the electrical characteristics of a solar cell is critical for determining the device's output performance and efficiency. The 4200A-SCS simplifies cell testing by automating the I-V, C-V, pulsed I-V, and resistivity measurements and provides graphics and analysis capability. For measurements of currents greater than 1 A, Keithley offers SourceMeter instruments that can be used for solar cell testing. Information on these models and further information on making solar cell measurements can be found on Keithley's website: www.keithley.com.

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